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TP6740

Qi Compliant Wireless Power Receiver

Application Note

Rev 1.2

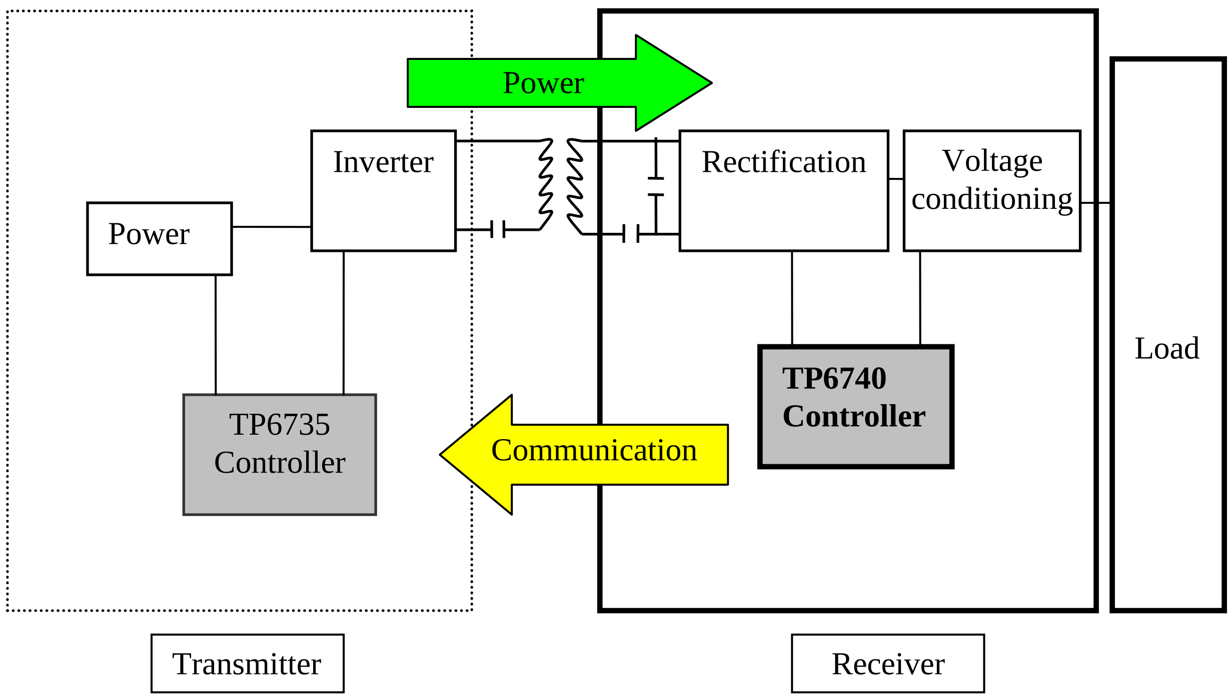
AMENDMENT HISTORY

Version	Date	Description
V1.0	Jan, 2015	New release.
V1.1	Jun, 2015	P12 edit figure 6-1
V1.2	Jan, 2017	1. P.5: Edit description in chapter 1 feature"2.5W(5v/500mA) " change to "5W(5V/1A)". 2. P.5: Replace pin description figure 3. P.6: Replace Figure3-1. 4. P.7: Replace Figure 4-1. 5. P.12: Replace Figure 6-1.

CONTENTS

Description

The TP6740 is a high efficiency, wireless power receiver for portable applications. The TP6740 device integrates digital controller required to comply with Qi v1.1 communication protocol and all necessary control algorithms needed for efficient. Together with TP6735 transmitter-side controller, the TP6740 enables a complete wireless power transfer system for Qi solution. By utilizing near-field inductive power transfer, the receiver coil embedded in the portable device can pick up the power transmitted by transmitter coil. Global feedback is established from the receiver to the transmitter in order to stabilize the power transfer process. This feedback is established by utilizing the Qi v1.2 communication protocol.



PRODUCT NAME

TP6740

TITLE

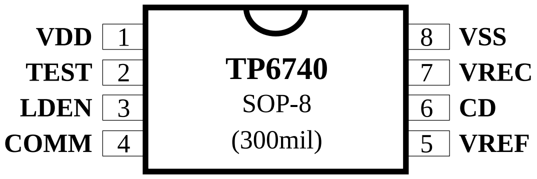
Qi Compliant Wireless Power Receiver

APPLICATION NOTE

1. Feature

- Signal modulation for Qi communication protocol
- 5v Output .
- Supports up to 5W(5v/1A) power output.
- Active adjust rectifier voltage to fit loading change.

2. Pin Descriptions



Pin	Pin Name	Pin Description
1	VDD	TP6740 Power 2.5V.
2	TEST	TEST/ Reserve.
3	LDEN	Enable/Disable output control. When voltage received from second coil is high enough to loading, LDEN pin will output low level.
4	COMM	Qi protocol signal output.
5	VREF	5V output monitor
6	CD	Current Detect.
7	VREC	Voltage divider input of rectifier.
8	VSS	GND.

3. Communication Modulator

The TP6740 provides Qi communication protocol which are output to the pins COMM. The COMM Pin must connected two NFETs. These NFETs are used for modulating the secondary load current which allows TP6740 to communicate error control and configuration information to the transmitter. Figure ?? shows how the COMM pins can be used for capacitive load modulation. A capacitor is connected from NFET Drain to AC1 and from NFET Drain to AC2. When the COMM switches are closed there is effectively a 22nF capacitor connected between AC1 and AC2. Connecting a capacitor in between AC1 and AC2 modulates the impedance seen by the coil, which will be reflected in the primary as a change in current.

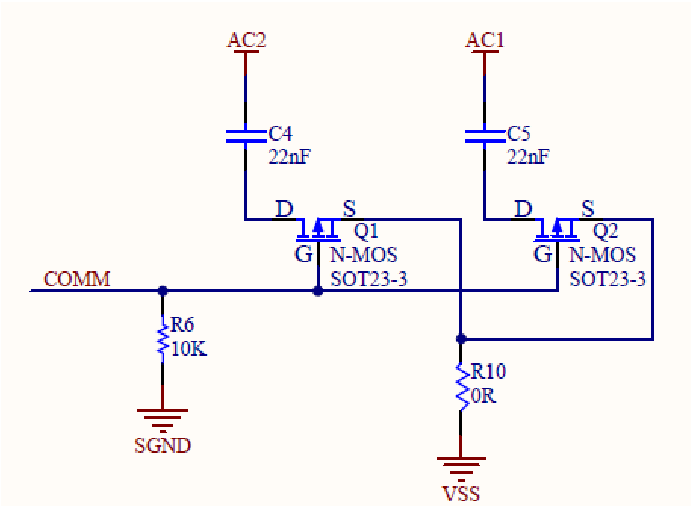


Figure 3-1 Capacitive Load Modulation

4. Rectifier Voltage Modify

TP6740 monitor rectifier voltage via VREC pin. In according to the amount of loading current adjusts the rectified voltage. If rectified voltage is too high, TP6740 will send negative control error value to transmitter. The transmitter modifies power to comply with the receiver. Hence, TP6740 can avoid the system voltage too low or low efficient situation.

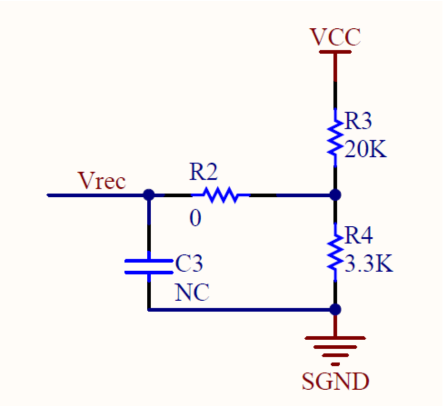


Figure 4-1 Rectified voltage divider

5. Power Receiver design requirements

5.1 Interface Surface

The distance from the Secondary Coil to the Interface Surface of the Mobile Device shall not exceed dz=2.5mm, across the bottom face of the Secondary Coil. See Figure 5-1.

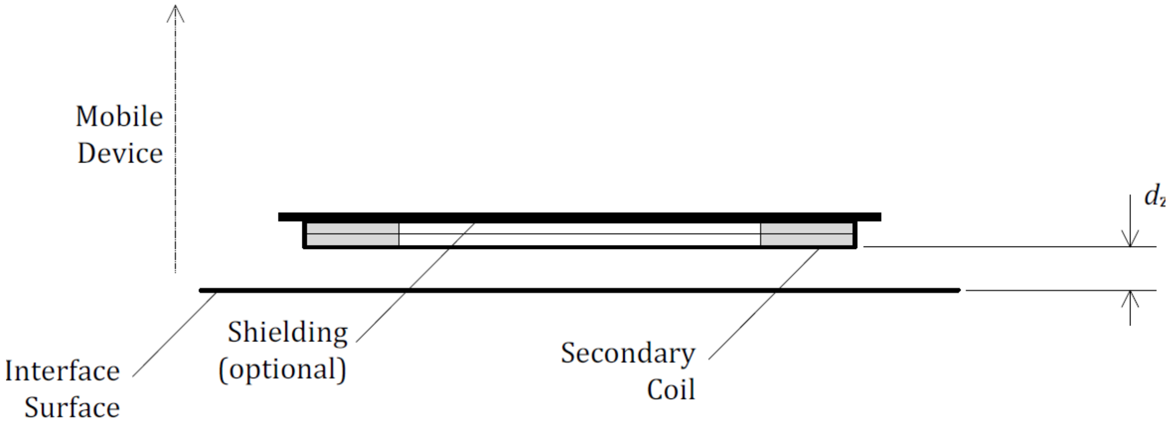


Figure 5-1 Secondary Coil assembly

5.2 Alignment aid

The design of a Mobile Device shall include means that helps a user to properly align the Secondary Coil of its Power Receiver to the Primary Coil of a Power Transmitter that enables Guided Positioning. This means shall provide the user with directional guidance—i.e. where to the user should move the Mobile Device—as well as alignment indication—i.e. feedback that the user has reached a properly aligned position.

5.3 Shielding

An important consideration for a Power Receiver designer is the impact of the Power Transmitter's magnetic field on the Mobile Device. Stray magnetic fields could interact with the Mobile Device and potentially cause its intended functionality to deteriorate, or cause its temperature to increase due to the power dissipation of generated eddy currents.

It is recommended to limit the impact of magnetic fields by means of Shielding on the top face of the Secondary Coil. See also Figure5-1. This Shielding should consist of material that has parameters similar to the materials listed.

- Material 44 — Fair Rite Corporation.
- Material 28 — Steward, Inc.
- CMG22G — Ceramic Magnetics, Inc.
- Material 78 — Fair Rite Corporation.
- 3C94 — Ferroxcube.
- N87 — Epcos AG.
- PC44 —TDK Corp.
- Kolektor 22G — Kolektor.
- LeaderTech SB28B2100-1 — LeaderTech Inc.
- TopFlux "A "— TopFlux.
- TopFlux "B "— TopFlux.
- ACME K081 — Acme Electronics.
- L7H — TDK Corporation.
- PE22 — TDK Corporation.
- FK2 — TDK Corporation.

The Shielding should cover the Secondary Coil completely. Additional Shielding beyond the outer diameter of the Secondary Coil might be necessary depending upon the impact of stray magnetic fields.

5.4 Dual resonant circuit

The dual resonant circuit of the Power Receiver comprises the Secondary Coil and two resonant capacitances. The purpose of the first resonant capacitance C_s is to enhance the power transfer efficiency. The purpose of the second resonant capacitance $C_d$is to enable a resonant detection method. Figure 5-2 illustrates the dual resonant circuit. The switch in the dual resonant circuit is optional. If the switch is not present, the capacitance C_d shall have a fixed connection to the Secondary Coil L_s. If the switch is present, it shall remain closed until the Power Receiver transmits its first Packet.

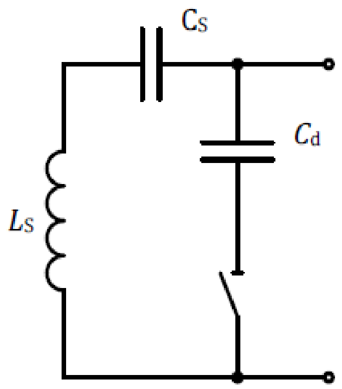


Fig 5-2 Dual resonant circuit of a Power Receiver

The dual resonant circuit shall have the following resonant frequencies:

$$fs = \frac{1}{2\pi \cdot \sqrt{Ls' \cdot Cs}} = 100^{+x}_{-y}\,kHz$$

$$fd = \frac{1}{2\pi \cdot \sqrt{Ls \cdot (\frac{1}{Cs} + \frac{1}{Cd})^{-1}}} = 1000^{\pm 10\%}\,kHz$$

In these equations, Ls' is the self inductance of the Secondary Coil when placed on the Interface Surface of a Power Transmitter and—if necessary—aligned to the Primary Cell; and Ls is the self inductance of the Secondary Coil without magnetically active material that is not part of the Power Receiver design close to the Secondary Coil (e.g. away from the Interface Surface of a Power Transmitter). Moreover, the tolerances x and y on the resonant frequency fs are x = y = 5% for Power Receivers that specify a Maximum Power value in the Configuration Packet of 3 W and above, and x = 5% and y = 10% for all other Power Receivers. The quality factor Q of the loop consisting of the Secondary Coil, switch (if present), resonant capacitance Cs and resonant capacitance Cd, shall exceed the value 77. Here the quality factor Q is defined as:

$$Q = \frac{2\pi \cdot fd \cdot Ls}{R}$$

with the DC resistance of the loop with the capacitances and short-circuited.

Figure 5-3 shows the environment that is used to determine the self-inductance Ls'of the Secondary Coil. The primary Shielding shown in Figure 5-3 consists of material PC44 from TDK Corp. The primary Shielding has a square shape with a side of 50 mm and a thickness of 1 mm. The center of the Secondary Coil and the center of the primary Shielding shall be aligned. The distance from the Receiver Interface Surface to the primary Shielding is dz = 3.4mm. Shielding on top of the Secondary Coil is present only if the Receiver design includes such Shielding. Other Mobile Device components that influence the inductance of the Secondary Coil shall be present as well when determining the resonant frequencies—the magnetic attractor shown in Figure 4-4 is example of such a component. The excitation signal that is used to determine Ls and Ls' shall have an amplitude of 1 V RMS and a frequency of 100 kHz.

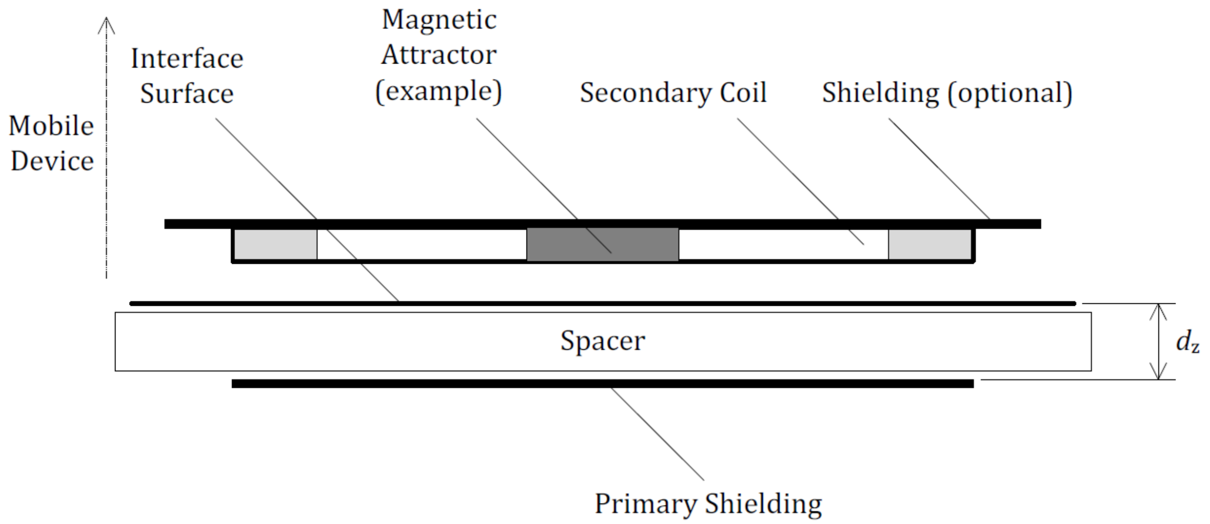


Fig 5-3 Characterization of resonant frequencies

6. Application Diagram

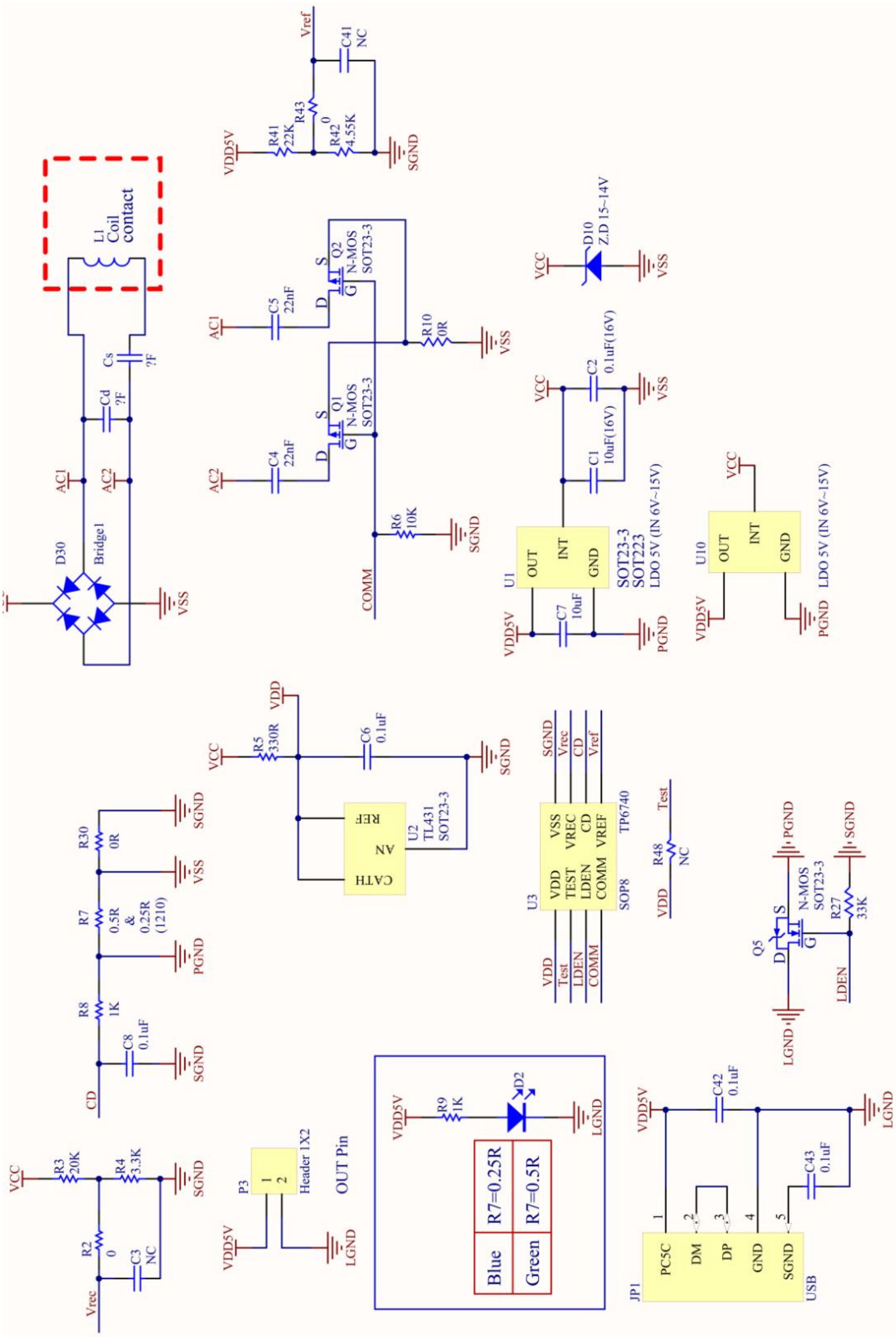


Figure 6-1 TP6740 Schemtic

7. Wireless charging demo

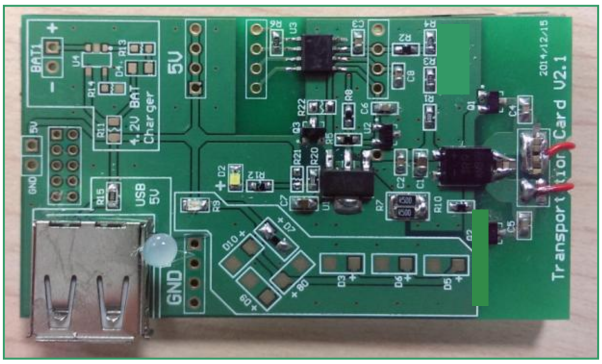


Figure 5-1 TP6740 Demo board

Figure 5-2 iPhone5s

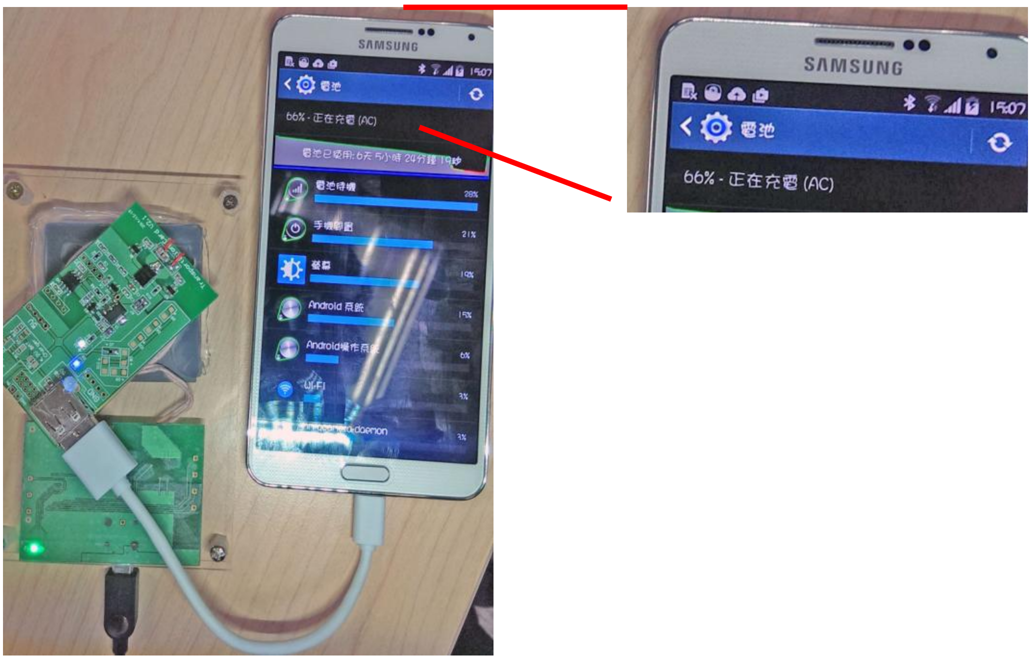


Figure 5-3 SAMSUNG Note3

8. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T_A = 25℃)

Parameter	Rating	Unit
Supply voltage	V_{SS} -0.3 to V_{SS} +6.5	V
Input voltage	V_{SS} -0.3 to V_{DD} +0.3	
Output voltage	V_{SS} -0.3 to V_{DD} +0.3	
Output current high per 1 PIN	-25	mA
Output current high per all PIN	-80	
Output current low per 1 PIN	+30	
Output current low per all PIN	+150	
Maximum operating voltage	5.5	V
Operating temperature	-40 to +85	°C
Storage temperature	-65 to +150	

DC Characteristics (T_A = 25℃, V_{DD} = 1.9V to 5.5V)

Parameter	Sym	Conditions		Min	Typ	Max	Unit
Operating Voltage	V_{DD}	25℃		1.9	5.0	5.5	V
COMM Source Current	I_{OH}	All Output	V_{DD} = 5V, V_{OH} = 0.9 V_{DD}	4	8	–	mA
			V_{DD} = 3V, V_{OH} = 0.9 V_{DD}	1.5	3	–	
COMM Sink Current	I_{OL}	All Output	V_{DD} = 5V, V_{OL} = 0.1 V_{DD}	10	20	–	mA
			V_{DD} = 3V, V_{OL} = 0.1 V_{DD}	5	10	–	
Input Leakage Current (pin high)	I_{ILH}	All Input	V_{IN} = V_{DD}	–	–	1	μA
Input Leakage Current (pin low)	I_{ILL}	All Input	V_{IN} = 0V	–	–	-1	μA
Power Supply Current	I_{DD}	Run 4 MHz, LVR enable	V_{DD} = 5V	–	1.4	–	mA
			V_{DD} = 3V	–	0.6	–	
LVR Reference Voltage	V_{LVR}	T_A = 25℃		–	2.2	–	V
				–	3.1	–	V
LVR Hysteresis Voltage	V_{HYST}	T_A = 25℃		–	±0.1	–	V
Low Voltage Detection time	t_{LVR}	T_A = 25℃		100	–	–	μs

Reset Timing Characteristics (T_A = -40℃ to +85℃)

Parameter	Conditions	Min	Typ	Max	Unit
TP6740 start up time	V_{DD} = 5V	–	22.5	–	ms
	V_{DD} = 3V	–	30.5	–	