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# TM87M23

## *DATA SHEET*

### *Rev 1.0*

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## AMENDMENT HISTORY

<b>Version</b>	<b>Date</b>	<b>Description</b>
1.0	Feb, 2019	New release.

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## GENERAL DESCRIPTION

The TM87M23 is a Multiple Time Programmed ROM embedded high-performance 4-bit microcomputer with LCD driver. It contains all the necessary functions, such as 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock operation, Resistance to Frequency Converter (RFC), EL panel driver, LCD driver, look-up table, watchdog timer and key matrix scanning circuitry in a signal chip.

## FEATURE

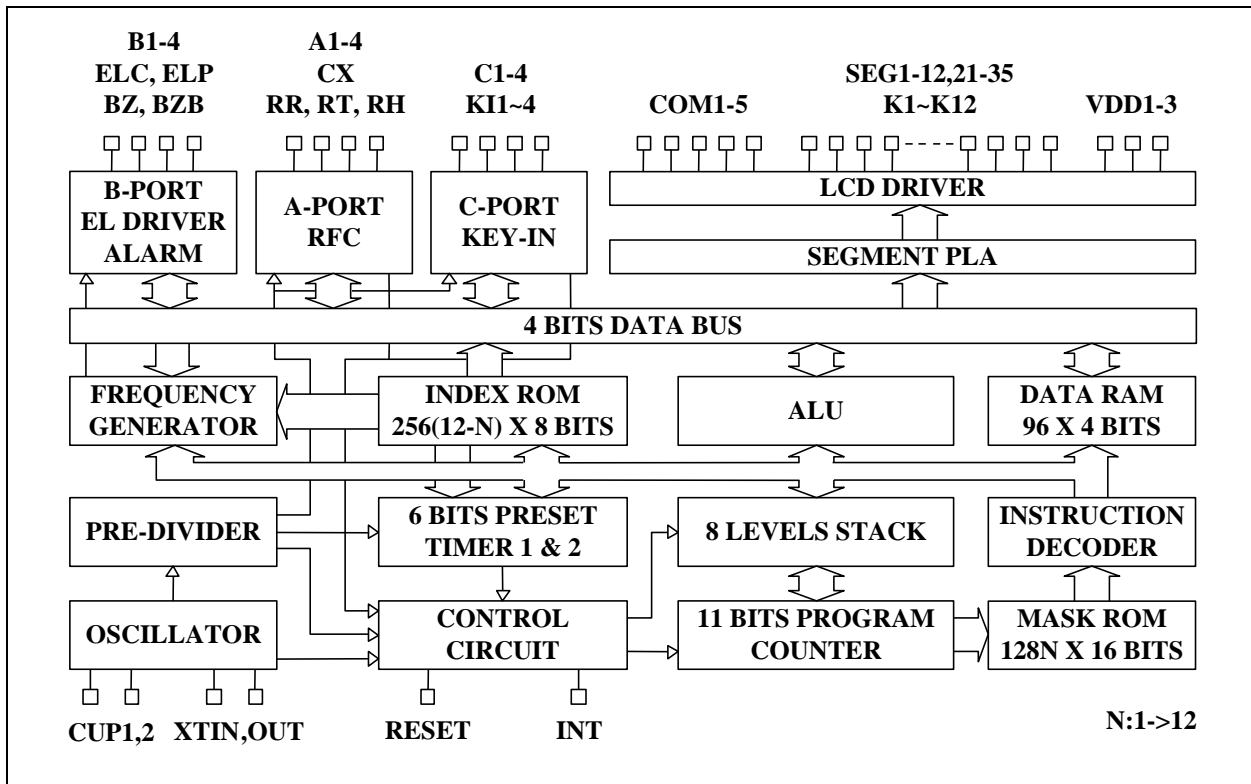
1. Low power dissipation.
  - 1.5V/3V operating voltage range.
2. Powerful instruction set.
  - Binary addition, subtraction, BCD. BCD can be executed directly in addition, subtraction.
  - Single-bit manipulation (set, reset, decision for branch).
  - Various conditional branches.
  - 16 initial working registers and manipulators.
  - Table look-up.
  - LCD driver data transfer.
3. ROM(MTP) capacity. 1.5K x 16 bits.
  - Instruction ROM Max. capacity 1.5K x 16 bits.
  - Table ROM Max. capacity 2816 x 8 bits.
  - Endurance: 1000 cycles (min.)
4. RAM capacity. 96 x 4bits (Address 50h ~ 6Fh is no use).
5. With direct/index addressing mode in data RAM access.
6. LCD driver output.
  - Max 135 LCD dots by 5 common outputs and 27 segment outputs.
  - SEG24~35 can be defined as IOA1~4/CX, RR, RT, RH, IOB1~4/ELC, ELP, BZB, BZ, IOC/KI1~4 by option.
  - 1/1~1/5 Duty can be selected by option.
  - 1/2 ~1/3 Bias can be selected by option.
  - Single instruction to turn off all segments.
  - COM1~5, SEG1~12,21~35 can be defined as CMOS or P\_open drain type output by option(COM1 & SEG35 force same PSTB & DBUS option for CMOS or P\_open drain type output).
7. Input/output ports.

- Port IOA4 pins (with internal pull-low), and can be defined as SEG24~27/CX,RR,RT,RH by option.
  - Port IOB4 pins (with internal pull-low), and can be defined as SEG28~31/ELC, ELP, BZB, BZ by option.
  - Port IOC4 pins (with internal pull-low, low-level-hold, input signal chattering prevention circuitry), and can be defined as SEG32~35/KI1~4 by option.
- 8. Interrupt function.**
- External factors     3 (INT pin, Port IOC & KI input).
  - Internal factors     4 (Pre-Divider, Timer1, Timer2 & RFC).
- 9. Built-in EL-light driver.**
- ELC, ELP. Can be defined as SEG28, 29/IOB1, 2 by option.
- 10. Built-in Alarm, clock or single tone melody generator.**
- BZB, BZ. Can be defined as SEG30, 31/IOB3, 4 by option.
- 11. Built-in resistance to frequency converter.**
- CX, RR, RT, RH. Can be defined as SEG24~27/IOA1~4 by option.
- 12. Built-in key matrix scanning function.**
- KO1~KO16 (Shared with SEG1~16)
  - KI1~KI4. Can be defined as SEG32~35/IOC1~4 by option.
- 13. Two 6-bit programmable timers with programmable clock source.**
- Read out the content in anytime
- 14. Watchdog timer.**
- 15. Built-in voltage charge halver & pump circuit.**
- 16. Dual clock operation**
- slow clock oscillation can be defined as X'tal or external RC type oscillator by option.
  - fast clock oscillation can be defined as internal R or external R(Fast Only) type oscillator by option.
- 17. HALT function.**
- 18. STOP function.**
- 19. Built-in Low Voltage Reset.**

## APPLICATION

- Timer/Calendar/Calculator/Thermometer

## BLOCK DIAGRAM



**PAD ASSIGNMENT**

No	Name	No	Name
1	BAK	27	SEG21
2	XIN	28	SEG22
3	XOUT	29	SEG23
4	GND	30	SEG24/IOA1/CX
5	VL1<VDD1>	31	SEG25/IOA2/RR
6	VL2<VDD2>	32	SEG26/IOA3/RT
7	VL3<VDD3>	33	SEG27/IOA4/RH
8	CUP1	34	SEG28/IOB1/ELC
9	CUP2	35	SEG29/IOB2/ELP
10	COM1	36	SEG30/IOB3/BZB
11	COM2	37	SEG31/IOB4/BZ
12	COM3	38	SEG32/IOC1/KI1
13	COM4	39	SEG33/IOC2/KI2
14	COM5	40	SEG34/IOC3/KI3
15	SEG1 (K1)	41	SEG35/IOC4/KI4
16	SEG2 (K2)	42	RESET (VPP)
17	SEG3 (K3)	43	INT
18	SEG4 (K4)	44	VBAT
19	SEG5 (K5)	45	
20	SEG6 (K6)	46	
21	SEG7 (K7)	47	
22	SEG8 (K8)	48	
23	SEG9 (K9)	49	
24	SEG10 (K10)	50	
25	SEG11 (K11)	51	
26	SEG12 (K12)	52	

**Symbol Description**

'<>' : Pin name in TM8723/TM8763

'()' : Attached function

'/' : Option function

## PIN DESCRIPTION

Name	I/O	Description
BAK	P	Positive Back-up voltage. If BAK=VL1/2 or VREG at BCF=0, connect a 0.1uF capacitor to GND. Positive voltage is need to BAK for Serial Program/Read Mode.
VBAT	P	Positive supply voltage. Positive voltage is need to VBAT for Serial Program/Read Mode.
VL1~3	P	LCD supply voltage. In 1.5V Power Mode & “LCD CHARGE PUMP MODE” option = “VL1 (NO REGULATOR”, connect positive power output to VL1. In 3V Power mode & “LCD CHARGE PUMP MODE” option = “VL1(NO REGULATOR)” or “VL2 (NO REGULATOR)”, connect positive power to VL2. If “LCD CHARGE PUMP MODE” option = “VDL (1.05V)” or “VDL (2.10V)”, connect Capacitors to VL1~3 For 1/3Bias by Capacitor Voltage Divider mode, connect positive power to VL3. Positive voltage is need to VL3 for Serial Program/Read Mode.
RESET	I	Input pin for external reset request signal, built-in internal pull-down resistor. High voltage is need to RESET pin for Serial Program/Read Mode.
INT	I	Input pin for external INT request signal. • Falling edge or rising edge triggered is defined by option. • Internal pull-down or pull-up resistor is defined by option.
CUP1,2	O	Switching pins for supply the LCD driving voltage to the VL1~3 pins. • Connect the CUP1 to CUP2 pins with non-polarized electrolytic capacitors when chip operated in 1/2 or 1/3 bias mode.
XIN XOUT	I O	In DUAL or SLOW ONLY mode option, is used as Low speed oscillator, generates clock for time base functions (clock specified. LCD alternating frequency. Alarm signal frequency) or system clock oscillation. • The usage of 32 KHz Crystal oscillator or external RC oscillator is defined by option. In FAST ONLY & USE EXTERNAL RESISTOR mode option, connect an external resistor could compose a RC oscillator .
COM1~5	O	Output pins for driving the common pins of the LCD panel. COM1~5 can be defined as COMS or Open Drain type output by option. COM1 & SEG35 force same PSTB & DBUS option for CMOS or P_open drain type output.
SEG1-12, 21-35	O	Output pins for driving the LCD panel segment. SEG24~27 can be defined as IOA1~4/CX, RR, RT, RH by option. SEG28~31 can be defined as IOB1~4/ELC, ELP, BZB, BZ by option. SEG32~35 can be defined as IOC1~4/KI1~4 by option. SEG1~12,21~35 can be defined as COMS or Open Drain type output by option. COM1 & SEG35 force same PSTB & DBUS option for CMOS or P_open drain type output.
IOA1-4	I/O	Input/Output port A, and can be defined as SEG24~27/CX,RR,RT,RH by option.
IOB1-4	I/O	Input/Output port B, and can be defined as SEG28~31/ELC,ELP,BZB,BZ by option.
IOC1-4	I/O	Input/Output port C, and can be defined as SEG32~35/KI1~4 by option. IOC3, 4 is Signal for Serial Program/Read Mode.
CX RR,RT,RH	I O	1 input pin and 3 output pins for RFC application, and can be defined as SEG24~27/IOA1~4 by option.
ELC/ELP	O	Output port for El panel driver, and can be defined as SEG28, 29/IOB1, 2 by option.
BZB/BZ	O	Output port for alarm, clock or single tone melody generator, and can be defined as SEG30, 31/IOB3, 4 by option.
KO1~KO12	O	Output port for key matrix scanning, shared with SEG1~12.
KI1~4	I	Input port for key matrix scanning, and can be defined as SEG32~35/IOC1~4 by option.



Name	I/O	Description
GND	P	Negative supply voltage.

## SERIAL PROGRAM/READ CONNECT PINS:

VBAT, BAK, VL3, GND, RESET, IOC3, IOC4

## ABSOLUTE MAXIMUM RATINGS

GND=0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VBAT	-0.3 to 3.6	V
	VL1	-0.3 to 2.1	
	VL2	-0.3 to 3.6	
	VL3	-0.3 to 6.0	
	VL4	-0.3 to 6.0	
	VL5	-0.3 to 6.0	
Maximum Input Voltage	Vin1	-0.3 to VBAT +0.3	V
	Vin2	-0.3 to VL1/2 +0.3	
Maximum output Voltage	Vout1	-0.3 to VBAT +0.3	V
	Vout2	-0.3 to VL1/2 +0.3	
	Vout3	-0.3 to VL3 +0.3	
	Vout4	-0.3 to VL4 +0.3	
	Vout5	-0.3 to VL5 +0.3	
Maximum Operating Temperature	Topg	-40 to+80	°C
Maximum Storage Temperature	Tstg	-40 to+125	

## ALLOWABLE OPERATING CONDITIONS

at#1: 1.5V Power Mode Ta=-20°C to 70°C, GND=0V

at#2: 3V Power Mode (BCF=0: BAK<VBAT), Ta= -20°C to 70°C, GND=0V

at#3: 3V Power Mode (BCF=0: BAK=VBAT), Ta= -40°C to 80°C, GND=0V

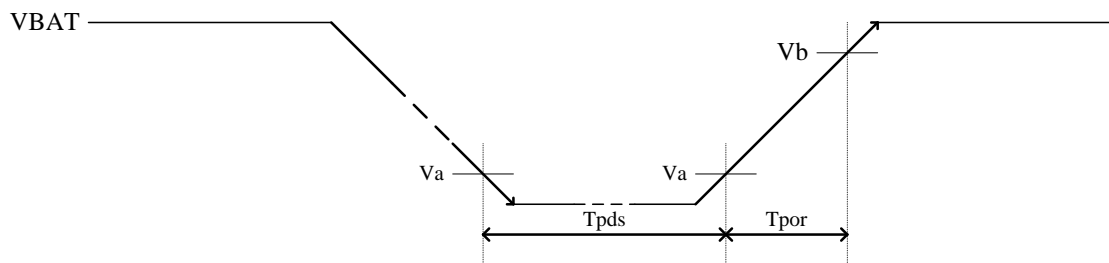
Crystal Mode condition: XIN&XOUT without match capacitor

Name	Symb.	Condition	Min.	Max.	Unit
Supply LCD Voltage	VL1		0.95	1.8	V
	VL2		1.8	3.6	
	VL3		1.8	5.4	
Oscillator Start-Up Voltage	BAK	Crystal Mode BCF=1, #1	1.4		V
		Crystal Mode BCF=1, #2	1.5		
		Crystal Mode BCF=1, #3	1.6		
Oscillator Sustain Voltage	BAK	Crystal Mode BCF=0, #1	1.1	1.8	

Name	Symb.	Condition	Min.	Max.	Unit
		Crystal Mode BCF=0, #2	1.1	3.6	
		Crystal Mode BCF=0, #3	1.3	3.6	
Supply Voltage	BAK		*1, *2	3.6	
Supply Voltage	VBAT	1.5V Power Mode	1.30*1	1.8	
Supply Voltage	VBAT	3V Power Mode BAK=VBAT for BCF=0	1.8	3.6	
Supply Voltage	VBAT	3V Power Mode BAK=VL1 for BCF=0	2.4	3.6	
Input "H" Voltage	Vih1	I/O, INT, RESETB, CX	0.8xVBAT	VBAT	
Input "L" Voltage	Vil1		0	0.2 x VBAT	
Input "H" Voltage	Vih2	OSCIN	0.8xBAK	BAK	
Input "L" Voltage	Vil2		0	0.2 x BAK	
Operating Freq	Fopg1	Crystal Mode	32		KHz
	Fopg2	RC Mode	10	4096	
	Fopg3	CF Mode	1000	4096	
Power-down stable time before Power-on reset activation	Tpds	Va= 0.1xVBAT	1		S
Power-on reset activation power rise time	Tpor	Va/Vb=0.1/0.9 x VBAT VBAT>=1.2V		10	mS

\*1: Crystal mode need take care Oscillator Start-Up Voltage.

\*2: BAK Minimum Operating Voltage follow=1.2/1.3/1.4V at 0/-20/-40°C



## ALLOWABLE OPERATING FREQUENCY

At #1 Ta= 0°C to 80°C, GND=0V

At #2 Ta= -20°C to 80°C, GND=0V

At #3 Ta= -40°C to 80°C, GND=0V

Condition	Maximum Operating Frequency
BAK=1.2V #1	500 KHz
BAK=1.3V #2	1 MHz
BAK=1.4V #3	1.5 MHz
BAK=1.8V #3	4 MHz
BAK=2.2V #3	6 MHz

## ELECTRICAL CHARACTERISTICS

### Power Consumption

at Ta= -40°C to 80°C, GND=0V

Halt Condition: BCF=0, 1/3Bias, 1/5Duty, LCD Alternating Frequency=PH7, Charge Pump Cycle=PH5, Only 32.768 KHz Crystal oscillator operating, without loading.

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
HALT mode	IHALT1	1.5V Power Mode, VBAT=1.5V		5		uA
	IHALT2	3V Power Mode (BCF=0=> BAK=VL1), VBAT=3.0V without regulator current		2		
	IHALT3	3V Power Mode (BCF=0=> BAK=VBAT), VBAT=3.0V without regulator current		10		
STOP mode	ISTOP				1	

Note: When RC oscillator function is operating, the current consumption will depend on the frequency of oscillation.

### Internal RC Frequency Range

at #1: Ta=0°C to 80°C, GND= 0V

at #2: Ta= -20°C to 80°C, GND= 0V

at #3: Ta= -40°C to 80°C, GND= 0V

Option Mode	BAK	Min.	Typ.	Max.
2 MHz	1.2V, #1	0.5 MHz	1.2 MHz	2.2 MHz
	1.3V, #2	0.5 MHz	1.5 MHz	2.5 MHz
	1.4V, #3	0.6 MHz	1.6 MHz	2.6 MHz
	1.5V, #3	0.7 MHz	1.7 MHz	2.7 MHz
	1.8V, #3	0.9 MHz	1.9 MHz	2.9 MHz
	2.4V, #3	1.0 MHz	2.0 MHz	3.0 MHz
	3.0V, #3	1.0 MHz	2.05 MHz	3.0 MHz
	3.6V, #3	1.0 MHz	2.1 MHz	3.0 MHz

## Input Resistance

at#1: VBAT=1.5V (1.5V Power Mode)

at#2: VBAT=3.0V (3V Power Mode)

at Ta= -40°C to 80°C, GND=0V

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
“L” Level Hold Tr. (IOC)	Rllh1	Vi=0.2VBAT, #1	10	40	100	KΩ
	Rllh2	Vi=0.2VBAT, #2	10	40	100	
IOA, B, C,D, E Pull-Down Tr.	Rmad1	Vi=VBAT, #1	200	500	1000	
	Rmad2	Vi=VBAT, #2	200	500	1000	
INT Pull-up Tr.	Rintu1	Vi=VBAT, #1	50	200	1000	
	Rintu2	Vi=VBAT, #2	50	350	1000	
INT Pull-Down Tr.	Rintd1	Vi=GND, #1	200	500	1000	
	Rintd2	Vi=GND, #2	200	500	1000	
RES Pull-Up R	Rres1	Vi=GND or VBAT, # 1	10	40	100	
	Rres2	Vi=GND or VBAT, #2	10	40	100	

## DC Output Characteristics

at#1: VBAT=1.2V

at#2: VBAT=2.4V

at Ta= -40°C to 80°C, GND=0V

Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output “H” Voltage	Voh1a	Ioh=-100uA, #1	COM1~5 & SEG1~12,21~35 (for DC/OD), IOB~C, ELC, ELP, BZB, BZ	1.0			V
	Voh2a	Ioh=-1mA, #2		2.0			
Output “L” Voltage	Vol1a	Iol=200uA, #1				0.2	
	Vol2a	Iol=2mA, #2				0.4	
Output “H” Voltage	Voh1b	Ioh=-200uA, #1	IOA, RR, RT, RH, INT&CX ( Vol only)	1.0			
	Voh2b	Ioh=-3mA, #2		2.0			
Output “L” Voltage	Vol1b	Iol=400uA, #1				0.2	
	Vol2b	Iol=5mA, #2				0.4	
Output “L” Voltage	Vol2c	Iol=40mA, #2	COM1~5 (for LED)			0.6	

## Segment Driver Output Characteristics

at#1: VL1=1.2V

at#2: VL2=2.4V

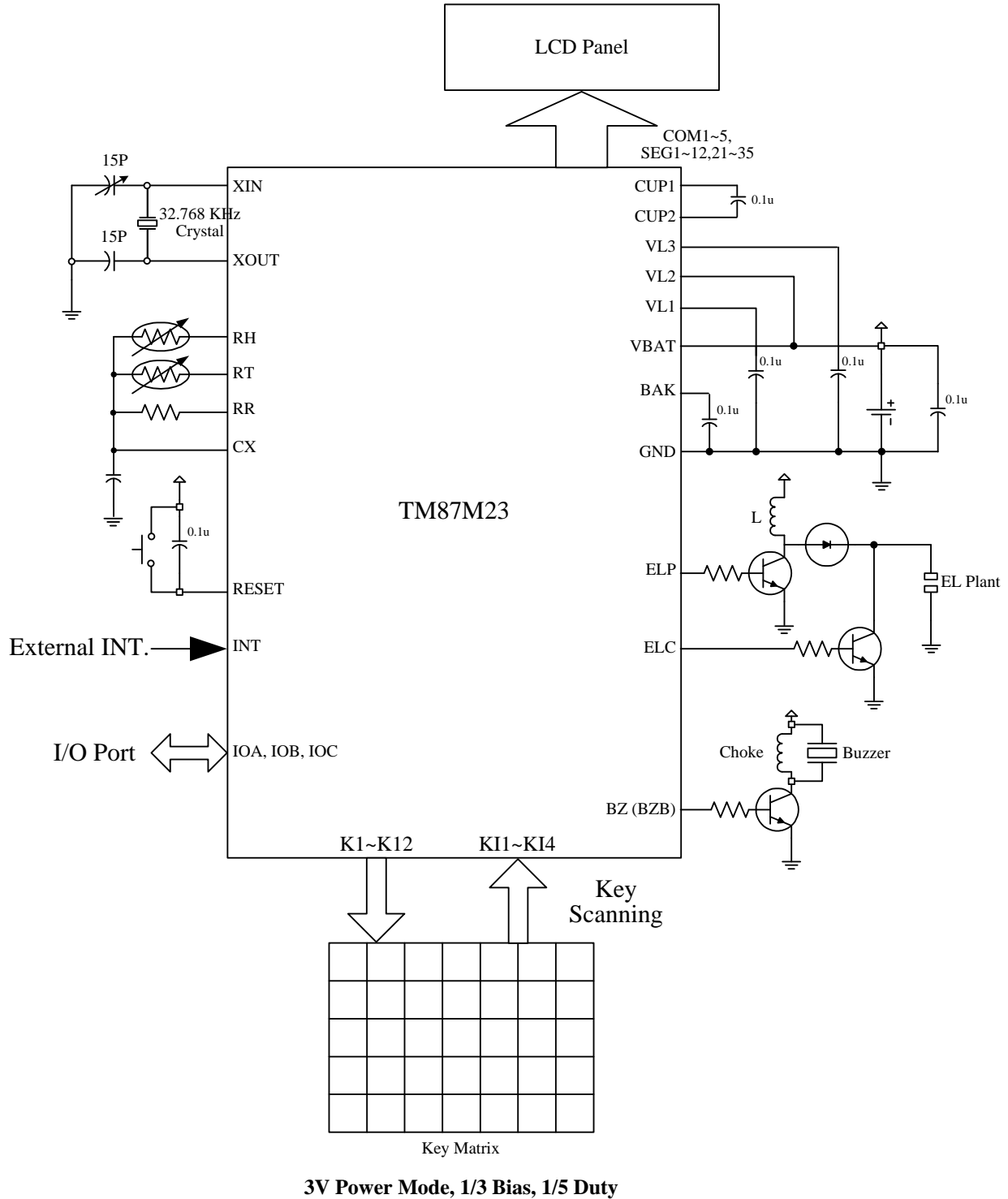
at#5: VL3=2.4V

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit.
Static display Mode							
Output “H” Voltage	Voh12f	Ioh=-1uA,#1,#2	SEG-n	2.2			V
Output “L” Voltage	Vol12f	Iol=1uA,#1,#2				0.2	

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit.	
Output "H" Voltage	Voh12g	Ioh=-10uA,#1,#2	COM-n	2.2			V	
Output "L" Voltage	Vol12g	Iol=10uA,#1,#2				0.2		
1/2 Bias display Mode								
Output "H" Voltage	Voh12f	Ioh=-1uA,#1,#2	SEG-n	2.2			V	
Output "L" Voltage	Vol12f	Iol=1uA,#1,#2				0.2		
Output "H" Voltage	Voh12g	Ioh=-10uA,#1,#2	COM-n	2.2			V	
Output "M1" Voltage	Vom112g	Iol/h=+/-10uA,#1,#2			1.0	1.4		
Output "L" Voltage	Vol12g	Iol=10uA,#1,#2				0.2		
1/3 Bias display Mode								
Output "H" Voltage	Voh12h	Ioh=-1uA,#1,#2	SEG-n	3.4			V	
	Voh5h	Ioh=-1uA,#5			2.2			
Output "M1" Voltage	Vom112h	Iol/h=+/-1uA,#1,#2			1.0	1.4		
	Vom15h	Iol/h=+/-1uA,#5			0.6	1.0		
Output "M2" Voltage	Vom212h	Iol/h=+/-1uA,#1,#2			2.2	2.6		
	Vom25h	Iol/h=+/-1uA,#5			1.4	1.8		
Output "L" Voltage	Vol12h	Iol=1uA,#1,#2				0.2		
	Vol5h	Iol=1uA,#5			0.2			
Output "H" Voltage	Voh12i	Ioh=-10uA,#1,#2	COM-n	3.4			V	
	Voh5i	Ioh=-1uA,#5			2.2			
Output "M1" Voltage	Vom112i	Iol/h=+/-10uA,#1,#2			1.0	1.4		
	Vom15i	Iol/h=+/-10uA,#5			0.6	1.0		
Output "M2" Voltage	Vom212i	Iol/h=+/-10uA,#1,#2			2.2	2.6		
	Vom25i	Iol/h=+/-10uA,#5			1.4	1.8		
Output "L" Voltage	Vol12i	Iol=10uA,#1,#2				0.2		
	Vol5i	Iol=10uA,#5			0.2			

### TYPICAL APPLICATION CIRCUIT

This application circuit is simply an example, and is not guaranteed to work.



**Appendix A TM87M23 Instruction Table**

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
IDC&		0000 0001 0100 1010	HL	← HL+1	
LCT	Lz, Ry	0000 001Z ZZZZ YYYY	Lz	← (7SEG ← Ry)	Ry=70H~7FH
LCB	Lz, Ry	0000 010Z ZZZZ YYYY	Lz	← (7SEG ← Ry)	Blank Zero
LCP	Lz, Ry	0000 011Z ZZZZ YYYY	Lz	← Ry & AC	
LCD	Lz, @HL	0000 100Z ZZZZ 0000	Lz	← T@HL	
LCD#	Lz, @HL	0000 100Z ZZZZ 1000	Lz	← T@HL ← HL+1	
LCT	Lz, @HL	0000 100Z ZZZZ 0001	Lz	← (7SEG ← @HL)	
LCT#	Lz, @HL	0000 100Z ZZZZ 1001	Lz	← (7SEG ← @HL) ← HL+1	
LCB	Lz, @HL	0000 100Z ZZZZ 0010	Lz	← (7SEG ← @HL)	Blank Zero
LCB#	Lz, @HL	0000 100Z ZZZZ 1010	Lz	← (7SEG ← @HL) ← HL+1	Blank Zero
LCP	Lz, @HL	0000 100Z ZZZZ 0011	Lz	← @HL & AC	
LCP#	Lz, @HL	0000 100Z ZZZZ 1011	Lz	← @HL & AC ← HL+1	
LCDX	D	0000 100D 0000 0100	Multi-Lz D=0 D=1	← T@HL : Multi-Lz=00H~0FH : Multi-Lz=10H~1FH	
LCTX	D	0000 100D 0000 0101	Multi-Lz	← (7SEG ← @HL)	
LCBX	D	0000 100D 0000 0110	Multi-Lz	← (7SEG ← @HL)	Blank Zero
LCPX	D	0000 100D 0000 0111	Multi-Lz	← @HL & AC	
OPA	Rx	0000 1010 0XXX XXXX	Port (A)	← Rx	
OPAS	Rx, D	0000 1011 DXXX XXXX	A1, 2, 3, 4	← Rx0,Rx1,D,Pulse	
OPB	Rx	0000 1100 0XXX XXXX	Port (B)	← Rx	
OPC	Rx	0000 1101 0XXX XXXX	Port (C)	← Rx	
FRQ	D, Rx	0001 00DD 0XXX XXXX	FREQ D=00 D=01 D=10 D=11	← Rx & AC : 1/4 Duty : 1/3 Duty : 1/2 Duty : 1/1 Duty	
FRQ	D, @HL	0001 01DD 0000 0000	FREQ	← T@HL	
FRQ#	D, @HL	0001 01DD 0000 1000	FREQ	← T@HL ← HL+1	
FRQX	D, X	0001 10DD XXXX XXXX	FREQ	← X	
MVL	Rx	0001 1100 0XXX XXXX	IDBF0~3	← Rx	
MVH	Rx	0001 1101 0XXX XXXX	IDBF4~11	← Rx,AC	
ADC	Rx	0010 0000 0XXX XXXX	AC	← Rx + AC + CF	CF
ADC	@HL	0010 0000 1000 0000	AC	← @HL + AC + CF	CF
ADC#	@HL	0010 0000 1100 0000	AC HL	← @HL + AC + CF ← HL+1	CF
ADC	@HL, DA	0010 0000 1001 0000	AC	← BCD(@HL + AC + CF)	CF
ADC#	@HL, DA	0010 0000 1101 0000	AC HL	← BCD(@HL + AC + CF) ← HL+1	CF
ADC*	Rx	0010 0001 0XXX XXXX	AC, Rx	← Rx + AC + CF	CF
ADC*	@HL	0010 0001 1000 0000	AC, @HL	← @HL + AC + CF	CF

Instruction		Machine Code	Function		Flag/Remark
ADC*#	@HL	0010 0001 1100 0000	AC, @HL HL	← @HL + AC + CF ←HL+1	CF
ADC*	@HL, DA	0010 0001 1001 0000	AC, @HL	← BCD (@HL + AC + CF)	CF
ADC*#	@HL, DA	0010 0001 1101 0000	AC, @HL HL	← BCD (@HL + AC + CF) ←HL+1	CF
SBC	Rx	0010 0010 0XXX XXXX	AC	← Rx + ACB + CF	CF
SBC	@HL	0010 0010 1000 0000	AC	← @HL + ACB + CF	CF
SBC#	@HL	0010 0010 1100 0000	AC HL	← @HL + ACB + CF ←HL+1	CF
SBC	@HL, DA	0010 0010 1001 0000	AC	←BCD (@HL + ACB + CF)	CF
SBC#	@HL, DA	0010 0010 1101 0000	AC HL	←BCD (@HL + ACB + CF) ←HL+1	CF
SBC*	Rx	0010 0011 0XXX XXXX	AC, Rx	← Rx + ACB + CF	CF
SBC*	@HL	0010 0011 1000 0000	AC, @HL	← @HL + ACB + CF	CF
SBC*#	@HL	0010 0011 1100 0000	AC, @HL HL	← @HL + ACB + CF ←HL+1	CF
SBC*	@HL, DA	0010 0011 1001 0000	AC, @HL	←BCD (@HL + ACB + CF)	CF
SBC*#	@HL, DA	0010 0011 1101 0000	AC, @HL HL	←BCD (@HL + ACB + CF) ←HL+1	CF
ADD	Rx	0010 0100 0XXX XXXX	AC	← Rx + AC	CF
ADD	@HL	0010 0100 1000 0000	AC	← @HL + AC	CF
ADD#	@HL	0010 0100 1100 0000	AC HL	← @HL + AC ←HL+1	CF
ADD	@HL, DA	0010 0100 1001 0000	AC	← BCD (@HL + AC)	CF
ADD#	@HL, DA	0010 0100 1101 0000	AC HL	← BCD (@HL + AC) ←HL+1	CF
ADD*	Rx	0010 0101 0XXX XXXX	AC, Rx	← Rx + AC	CF
ADD*	@HL	0010 0101 1000 0000	AC, @HL	← @HL + AC	CF
ADD*#	@HL	0010 0101 1100 0000	AC, @HL HL	← @HL + AC ←HL+1	CF
ADD*	@HL, DA	0010 0101 1001 0000	AC, @HL	← BCD(@HL + AC)	CF
ADD*#	@HL, DA	0010 0101 1101 0000	AC, @HL HL	← BCD(@HL + AC) ←HL+1	CF
SUB	Rx	0010 0110 0XXX XXXX	AC	← Rx + ACB + 1	CF
SUB	@HL	0010 0110 1000 0000	AC	← @HL + ACB + 1	CF
SUB#	@HL	0010 0110 1100 0000	AC HL	← @HL + ACB + 1 ←HL+1	CF
SUB	@HL, DA	0010 0110 1001 0000	AC	← BCD (@HL + ACB + 1)	CF
SUB#	@HL, DA	0010 0110 1101 0000	AC HL	← BCD (@HL + ACB + 1) ←HL+1	CF
SUB*	Rx	0010 0111 0XXX XXXX	AC, Rx	← Rx + ACB + 1	CF
SUB*	@HL	0010 0111 1000 0000	AC, @HL	← @HL + ACB + 1	CF
SUB*#	@HL	0010 0111 1100 0000	AC, @HL HL	← @HL + ACB + 1 ←HL+1	CF
SUB*	@HL, DA	0010 0111 1001 0000	AC, @HL	← BCD (@HL + ACB + 1)	CF
SUB*#	@HL, DA	0010 0111 1101 0000	AC, @HL HL	← BCD (@HL + ACB + 1) ←HL+1	CF
ADN	Rx	0010 1000 0XXX XXXX	AC	← Rx + AC	
ADN	@HL	0010 1000 1000 0000	AC	← @HL + AC	
ADN#	@HL	0010 1000 1100 0000	AC	← @HL + AC	



Instruction		Machine Code	Function		Flag/Remark
			HL	←HL+1	
ADN*	Rx	0010 1001 0XXX XXXX	AC, Rx	← Rx + AC	
ADN*	@HL	0010 1001 1000 0000	AC, @HL	← @HL + AC	
ADN*#	@HL	0010 1001 1100 0000	AC, @HL HL	← @HL + AC ←HL+1	
AND	Rx	0010 1010 0XXX XXXX	AC	← Rx AND AC	
AND	@HL	0010 1010 1000 0000	AC	← @HL AND AC	
AND#	@HL	0010 1010 1100 0000	AC HL	← @HL AND AC ←HL+1	
AND*	Rx	0010 1011 0XXX XXXX	AC, Rx	← Rx AND AC	
AND*	@HL	0010 1011 1000 0000	AC, @HL	← @HL AND AC	
AND*#	@HL	0010 1011 1100 0000	AC, @HL HL	← @HL AND AC ←HL+1	
EOR	Rx	0010 1100 0XXX XXXX	AC	← Rx EOR AC	
EOR	@HL	0010 1100 1000 0000	AC	← @HL EOR AC	
EOR#	@HL	0010 1100 1100 0000	AC HL	← @HL EOR AC ←HL+1	
EOR*	Rx	0010 1101 0XXX XXXX	AC,Rx	← Rx EOR AC	
EOR*	@HL	0010 1101 1000 0000	AC, @HL	← @HL EOR AC	
EOR*#	@HL	0010 1101 1100 0000	AC, @HL HL	← @HL EOR AC ←HL+1	
OR	Rx	0010 1110 0XXX XXXX	AC	← Rx OR AC	
OR	@HL	0010 1110 1000 0000	AC	← @HL OR AC	
OR#	@HL	0010 1110 1100 0000	AC HL	← @HL OR AC ←HL+1	
OR*	Rx	0010 1111 0XXX XXXX	AC, Rx	← Rx OR AC	
OR*	@HL	0010 1111 1000 0000	AC, @HL	← @HL OR AC	
OR*#	@HL	0010 1111 1100 0000	AC, @HL HL	← @HL OR AC ←HL+1	
ADCI	Ry, D	0011 0000 DDDD YYYY	AC	← Ry + D + CF	CF
ADCI*	Ry, D	0011 0001 DDDD YYYY	AC, Ry	← Ry + D + CF	CF
SBCI	Ry, D	0011 0010 DDDD YYYY	AC	← Ry + DB + CF	CF
SBCI*	Ry, D	0011 0011 DDDD YYYY	AC, Ry	← Ry + DB + CF	CF
ADDI	Ry, D	0011 0100 DDDD YYYY	AC	← Ry + D	CF
ADDI*	Ry, D	0011 0101 DDDD YYYY	AC, Ry	← Ry + D	CF
SUBI	Ry, D	0011 0110 DDDD YYYY	AC	← Ry + DB + 1	CF
SUBI*	Ry, D	0011 0111 DDDD YYYY	AC, Ry	← Ry + DB + 1	CF
ADNI	Ry, D	0011 1000 DDDD YYYY	AC	← Ry + D	
ADNI*	Ry, D	0011 1001 DDDD YYYY	AC, Ry	← Ry + D	
ANDI	Ry, D	0011 1010 DDDD YYYY	AC	← Ry AND D	
ANDI*	Ry, D	0011 1011 DDDD YYYY	AC, Ry	← Ry AND D	
EORI	Ry, D	0011 1100 DDDD YYYY	AC	← Ry EOR D	
EORI*	Ry, D	0011 1101 DDDD YYYY	AC, Ry	← Ry EOR D	
ORI	Ry, D	0011 1110 DDDD YYYY	AC	← Ry OR D	
ORI*	Ry, D	0011 1111 DDDD YYYY	AC, Ry	← Ry OR D	
INC*	Rx	0100 0000 0XXX XXXX	AC, Rx	← Rx + 1	CF
INC*	@HL	0100 0000 1000 0000	AC, @HL	← @HL + 1	CF
INC*#	@HL	0100 0000 1100 0000	AC, @HL HL	← @HL + 1 ←HL+1	CF

Instruction		Machine Code	Function		Flag/Remark
DEC*	Rx	0100 0001 0XXX XXXX	AC, Rx	← Rx - 1	CF
DEC*	@HL	0100 0001 1000 0000	AC, @HL	← @HL - 1	CF
DEC*#	@HL	0100 0001 1100 0000	AC, @HL HL	← @HL - 1 ← HL+1	CF
IPA	Rx	0100 0110 0XXX XXXX	AC, (Rx)	← Port(A)	
IPB	Rx	0100 0110 1XXX XXXX	AC, (Rx)	← Port(B)	
IPC	Rx	0100 0111 0XXX XXXX	AC, Rx	← Port(C)	
LDS	@HL, D	0100 1001 1000 DDDD	AC, @HL	← D	
LDS#	@HL, D	0100 1001 1100 DDDD	AC, @HL HL	← D ← HL+1	
MAF	Rx	0100 1010 0XXX XXXX	AC, Rx	← STS1	B3: CF B2: ZERO B1: (No use) B0: (No use)
RTM2L	Rx	0100 1010 1XXX XXXX	AC, (Rx)	← TM2 (0~3)	
MSB	Rx	0100 1011 0XXX XXXX	AC, Rx	← STS2	B3: (No use) B2: SCF2 (HRx) B1: SCF1 (CPT) B0: BCF
RTM21	Rx	0100 1011 1XXX XXXX	AC, (Rx)	← TM2 (4, 5), 1 (0, 1)	
MSC	Rx	0100 1100 0XXX XXXX	AC, Rx	← STS3	B3: SCF7 (PDV) B2: PH15 B1: SCF5 (TM1) B0: SCF4 (INT)
RTM1H	Rx	0100 1100 1XXX XXXX	AC, (Rx)	← TM1 (2~5)	
MCX	Rx	0100 1101 0XXX XXXX	AC, Rx	← STS3X	B3: SCF9(RFC) B2: (No use) B1: SCF6 (TM2) B0: SCF8 (SKI)
MSD	Rx	0100 1110 0XXX XXXX	AC, Rx	← STS4	B3: (No use) B2: RFOVF B1: WDF B0: CSF
SR0	Rx	0101 0000 0XXX XXXX	ACn, Rxn AC3, Rx3	← Rx (n+1) ← 0	
SR1	Rx	0101 0000 1XXX XXXX	ACn, (Rx)n AC3, (Rx)3	← (Rx) (n+1) ← 1	
SL0	Rx	0101 0001 0XXX XXXX	ACn, (Rx)n AC0, (Rx)0	← (Rx) (n-1) ← 0	
SL1	Rx	0101 0001 1XXX XXXX	ACn, (Rx)n AC0, (Rx)0	← (Rx) (n-1) ← 1	
RRC	Rx	0101 0010 0XXX XXXX	ACn, (Rx)n AC3, (Rx)3 CF	← (Rx) (n+1) ← CF ← (Rx) 0	CF
RRC RRC#	@HL	0101 0010 1B00 0000	ACn, (@HL)n AC3, (@HL)3 CF '#': HL	← (@HL) (n+1) ← CF ← (@HL) 0 ← HL+1	' ': B6=0 '#': B6=1
RLC	Rx	0101 0011 0XXX XXXX	ACn, (Rx)n AC0, (Rx)0	← (Rx) (n-1) ← CF	CF ' ': B6=0

Instruction		Machine Code	Function		Flag/Remark
RLC RLC#	@HL	0101 0011 1B00 0000	CF ACn, (@HL)n AC0, (@HL)0 CF '#': HL	← (Rx) 3 ← (@HL) (n-1) ← CF ← (@HL) 3 ← HL+1	'#': B6=1
DAA		0101 0100 0000 0000	AC	← BCD (AC)	
DAA*	Rx	0101 0101 0XXX XXXX	AC, Rx	← BCD (AC)	
DAA*	@HL	0101 0101 1000 0000	AC, @HL	← BCD (AC)	
DAA*#	@HL	0101 0101 1100 0000	AC, @HL HL	← BCD (AC) ← HL+1	
DAS		0101 0110 0000 0000	AC	← BCD (AC)	
DAS*	Rx	0101 0111 0XXX XXXX	AC, Rx	← BCD (AC)	
DAS*	@HL	0101 0111 1000 0000	AC, @HL	← BCD (AC)	
DAS*#	@HL	0101 0111 1100 0000	AC, @HL HL	← BCD (AC) ← HL+1	
LDS	Rx, D	0101 1DDD DXXX XXXX	AC, Rx	← D	
LDH	Rx, @HL	0110 0000 0XXX XXXX	AC, Rx	← H (T@HL)	
LDH*	Rx, @HL	0110 0001 0XXX XXXX	AC, Rx HL	← H (T@HL) ← HL + 1	
LDL	Rx, @HL	0110 0010 0XXX XXXX	AC, Rx	← L (T@HL)	
LDL*	Rx, @HL	0110 0011 0XXX XXXX	AC, Rx HL	← L (T@HL) ← HL + 1	
MRF1	Rx	0110 0100 0XXX XXXX	AC, Rx	← RFC3-0	
MRF2	Rx	0110 0101 0XXX XXXX	AC, Rx	← RFC7-4	
MRF3	Rx	0110 0110 0XXX XXXX	AC, Rx	← RFC11-8	
MRF4	Rx	0110 0111 0XXX XXXX	AC, Rx	← RFC15-12	
STA	Rx	0110 1000 0XXX XXXX	Rx	← AC	
STA	@HL	0110 1000 1000 0000	@HL	← AC	
STA#	@HL	0110 1000 1100 0000	@HL HL	← AC ← HL+1	
LDA	Rx	0110 1100 0XXX XXXX	AC	← Rx	
LDA	@HL	0110 1100 1000 0000	AC	← @HL	
LDA#	@HL	0110 1100 1100 0000	AC HL	← @HL ← HL+1	
MRA	Rx	0110 1101 0XXX XXXX	CF	← Rx3	
MRW	@HL, Rx	0110 1110 0XXX XXXX	AC, @HL	← Rx	
MRW#	@HL, Rx	0110 1110 1XXX XXXX	AC, @HL HL	← Rx ← HL+1	
MWR	Rx, @HL	0110 1111 0XXX XXXX	AC, Rx	← @HL	
MWR#	Rx, @HL	0110 1111 1XXX XXXX	AC, Rx HL	← @HL ← HL+1	
MRW	Ry, Rx	0111 0YYY YXXX XXXX	AC, Ry	← Rx	
MWR	Rx, Ry	0111 1YYY YXXX XXXX	AC, Rx	← Ry	
JB0	X	1000 0XXX XXXX XXXX	PC	← X	if AC0 = 1
JB1	X	1000 1XXX XXXX XXXX	PC	← X	if AC1 = 1
JB2	X	1001 0XXX XXXX XXXX	PC	← X	if AC2 = 1
JB3	X	1001 1XXX XXXX XXXX	PC	← X	if AC3 = 1
JNZ	X	1010 0XXX XXXX XXXX	PC	← X	if AC ≠ 0
JNC	X	1010 1XXX XXXX XXXX	PC	← X	if CF = 0

Instruction		Machine Code	Function		Flag/Remark
JZ	X	1011 0XXX XXXX XXXX	PC	← X	if AC = 0
JC	X	1011 1XXX XXXX XXXX	PC	← X	if CF = 1
CALL	X	1100 0XXX XXXX XXXX	STACK PC	← PC + 1 ← X	
JMP	X	1101 0XXX XXXX XXXX	PC	← X	
TMS	Rx	1110 0000 0XXX XXXX	AC3, 2 = 11 AC3, 2 = 10 AC3, 2 = 01 AC3, 2 = 00 AC1, 0, PB3~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TMS	@HL	1110 0001 0000 0000	TD7, 6 = 11 TD7, 6 = 10 TD7, 6 = 01 TD7, 6 = 00 TD5~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TMS#	@HL	1110 0001 0000 1000	TD7, 6 = 11 TD7, 6 = 10 TD7, 6 = 01 TD7, 6 = 00 TD5~0 HL	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value ← HL+1	
TMSX	X	1110 0010 XXXX XXXX	X7, 6=011 X7, 6=010 X7, 6=001 X7, 6=000 X5~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TM2	Rx	1110 0100 0XXX XXXX	Timer2	← Rx & AC	
TM2	@HL	1110 0101 0000 0000	Timer2	← T@HL	
TM2#	@HL	1110 0101 0000 1000	Timer2 HL	← T@HL ← HL+1	
TM2X	X	1110 011X XXXX XXXX	X8, 7, 6=111 X8, 7, 6=110 X8, 7, 6=101 X8, 7, 6=100 X8, 7, 6=011 X8, 7, 6=010 X8, 7, 6=001 X8, 7, 6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer2 Value	
SHE	X	1110 1000 0XXX XXX0	X6 X5 X4 X3 X2 X1	: Enable HEF6 : Enable HEF5 : Enable HEF4 : Enable HEF3 : Enable HEF2 : Enable HEF1	RFC KEY_S TMR2 PDV INT TMR1
SIE*	X	1110 1001 0XXX XXXX	X6 X5 X4 X3 X2 X1 X0	: Enable IEF6 : Enable IEF5 : Enable IEF4 : Enable IEF3 : Enable IEF2 : Enable IEF1 : Enable IEF0	RFC KEY_S TMR2 PDV INT TMR1 C/DPT
PLC	X	1110 101X 0XXX XXXX	X8	: Reset PH15~11	

Instruction		Machine Code	Function		Flag/Remark
			X6=0	: Reset HRF6-0	
SRF	X	1110 1100 00XX XXXX	X5 X4 X3 X2 X1 X0	: Enable Cx Control : Enable TM2 Control : Enable Counter : Enable RH Output : Enable RT Output : Enable RR Output	ENX EHM ETP ERR
SRE	X	1110 1101 X0XX 0000	X7 X5 X4	: Enable SRF7 : Enable SRF5 : Enable SRF4	SRF7(KEY_S) SRF5 (INT) SRF4 (C Port)
FAST	(X)	1110 1110 0000 0XXX	B/SCLK X=7 X=6 X=5 X=4 X=3 X=2 X=1 X=0 or None	: High Speed Clock : B/SCLK=FTOSC/128 : B/SCLK=FTOSC/64 : B/SCLK=FTOSC/32 : B/SCLK=FTOSC/16 : B/SCLK=FTOSC/8 : B/SCLK=FTOSC/4 : B/SCLK=FTOSC/2 : B/SCLK=FTOSC	
SLOW		1110 1111 0000 0000	SCLK	: Low Speed Clock	
SPK	X	1110 0011 XXXX XXXX	X6=1 X6=0  X7, 5, 4=000  X7, 5, 4=001 X7, 5, 4=010 X7, 5, 4=10X  X7, 5, 4=110  X7, 5, 4=111	: KEY_S release by scanning cycle : KEY_S release by normal key scanning  : Set one of KO1~16 =1 by X3~0  : Set all = 1 : Set all Hi-z : Set eight of KO1~16 =1 by X3 X3=0 => KO1~8 X3=1 => KO9~16  : Set four of KO1~16 =1 by X3, 2 X3,2=00 => KO1~4 X3,2=01 => KO5~8 X3,2=10 => KO9~12 X3,2=11 => KO13~16  : Set two of KO1~16 =1 by X3, 2, 1 X3~1=000 => KO1, 2 X3~1=001 => KO3, 4 X3~1=010 => KO5, 6 X3~1=011 => KO7, 8 X3~1=100 => KO9, 10 X3~1=101 => KO11, 12 X3~1=110 => KO13, 14 X3~1=111 => KO15, 16	
RTS		1101 1000 0000 0000	PC	← STACK	CALL Return
SCC	X	1101 1001 0X00 0XXX	X6=1 X6=0 X2, 1, 0=001 X2, 1, 0=010	: Cfq=BCLK : Cfq=PH0 : Cch = PH10 : Cch = PH8	



Instruction		Machine Code	Function		Flag/Remark
			X1	: Dis-ENX Reset	DED
			X0	: Reload 2 Reset	RL2
HALT		1111 1110 0000 0000	Halt Operation		
STOP		1111 1111 0000 0000	Stop Operation		

## Symbol Description

AC	: Accumulator	D	: Immediate Data
ACB	: Invert of Accumulator	DB	: Invert of Immediate Data
ACn	: Accumulator bit n	PC	: Program Counter
X	: Address or Set data	CF	: Carry Flag
Rx	: Address of Data RAM	ZERO	: Zero Flag
(Rx) n	: Bit n of (Rx)	WDF	: Watch-Dog Timer Enable Flag
Ry	: Address of working register	PDV	: Pre-Divider
BCF	: Back-up Flag	BCLK	: System clock stop only in STOP condition
IEFn	: Interrupt Enable Flag	SEFn	: Switch Enable Flag
HRFn	: HALT Release Flag	SRFn	: STOP Release Enable Flag
HEFn	: HALT Release Enable Flag	SCFn	: Start Condition Flag
TMR	: Timer Overflow Release Flag	Cch	: Clock Source of Chattering Detector
Ctm	: Clock Source of Timer	Cfq	: Clock Source of Frequency Generator
Lz	: Address of LCD data	FREQ	: Frequency Generator setting Value
RFOVF	: RFC Overflow Flag	( )	: Content of Address Register
MUI	: Multiplication Input Register	MU	: Multiplication High nibble Result Register
@HL	: Address assigned by Index Register	HL	: Index Register
H (T@HL)	: High Nibble of Index ROM data	L (T@HL)	: Low Nibble of Index ROM Data
IDBF	: Content of Index Register		
T@HL	: Index ROM address assigned by Index Register	DA	: BCD for result
CSF	: Clock Source Flag		
FTOSC	: Fast Oscillation clock		
(@HL)	: 4bits data type for Data RAM		
T(@HL)	: 8 bits data type for Index ROM		
HL+1	: +1 to index address bit0		