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TM8727

DATA SHEET

Rev 1.1

AMENDMENT HISTORY

Version	Date	Description
1.0	Aug, 2004	New release.
1.1	Dec, 2016	P.13 Delete the Static data from Segment Driver Output Characteristics

CONTENTS

GENERAL DESCRIPTION

The TM8727 is an embedded high-performance 4-bit microcomputer with LCD driver. It contains all the necessary functions, such as 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock operation, Resistance to Frequency Converter(RFC), EL panel driver, LCD driver, look-up table, watchdog timer and key matrix scanning circuitry in a signal chip.

FEATURE

1. Low power dissipation.

2. Powerful instruction set (178 instructions).

- Binary addition, subtraction, BCD adjust, logical operation in direct and index addressing mode.
- Single-bit manipulation (set, reset, decision for branch).
- Various conditional branch.
- 16 working registers and manipulation.
- Table look-up.
- LCD driver data transfer.

3. Memory capacity.

- ROM capacity 12288 x 16 bits.

  Program Address X100~X1FFh reversed for Bank Convert Area.
- RAM capacity 1024 x 4 bits.

4. LCD driver output.

- 9 common outputs and 41 segment outputs (up to drive 369 LCD segments).
- 1/2 Duty, 1/3 Duty, 1/4 Duty, 1/5 Duty, 1/6Duty, 1/7Duty, 1/8Duty or 1/9Duty is selected by MASK option.
- 1/2 Bias, 1/3 Bias or 1/4 Bias is selected by MASK option.
- Single instruction to turn off all segments.
- COM5~9,SEG1~41 could be defined as CMOS or P_open drain type output by mask option.

5. Input/output ports.

- Port IOA 4 pins (with internal pull-low), muxed with SEG24~SEG27.
- Port IOB 4 pins (with internal pull-low). muxed with SEG28~SEG31
- Port IOC 4 pins (with internal pull-low, low-level-hold), muxed with SEG32~SEG35.

  IOC port had built in the input signal chattering prevention circuitry.
- Port IOD 4 pins (with internal pull-low) , muxed with SEG36~SEG39. IOD port had built in the input signal chattering prevention circuitry.

6. 8 level subroutine nesting.

7. Interrupt function.

- External factors 4 (INT pin, Port IOC, IOD & KI input).
- Internal factors 4 (Pre-Divider, Timer1, Timer2 & RFC).

8. Built-in EL-light driver.

- ELC, ELP (Muxed with SEG28, SEG29).

9. Built in Alarm, clock or single tone melody generator.

- BZB, BZ (Muxed with SEG30, SEG31).

10. Built-in resistance to frequency converter.

- CX, RR, RT, RH (Muxed with SEG24~SEG27).

11. Built in key matrix scanning function.

- K1~K16 (Shared with SEG1~SEG16).
- KI1~KI4 (Muxed with SEG32~SEG35).

12. Two 6-bit programmable timer with programmable clock source.

13. Watch dog timer.

14. Built-in Voltage doubler, halver, tripler, quartic charge pump circuit.

15. Dual clock operation

- slow clock oscillation can be defined as X’tal or external RC type oscillator by mask option.
- fast clock oscillation can be defined as 3.58MHz ceramic resonator, internal R or external R type oscillator by mask option.

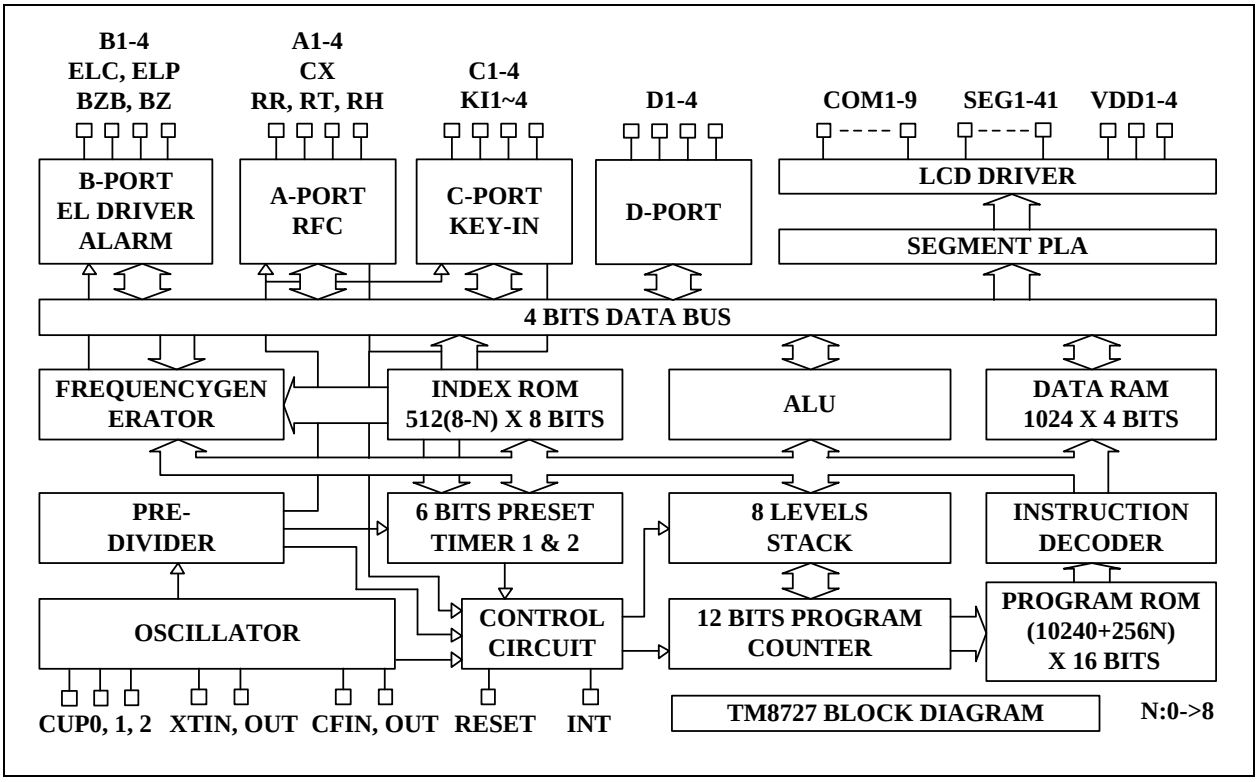
16. HALT function.

17. STOP function.

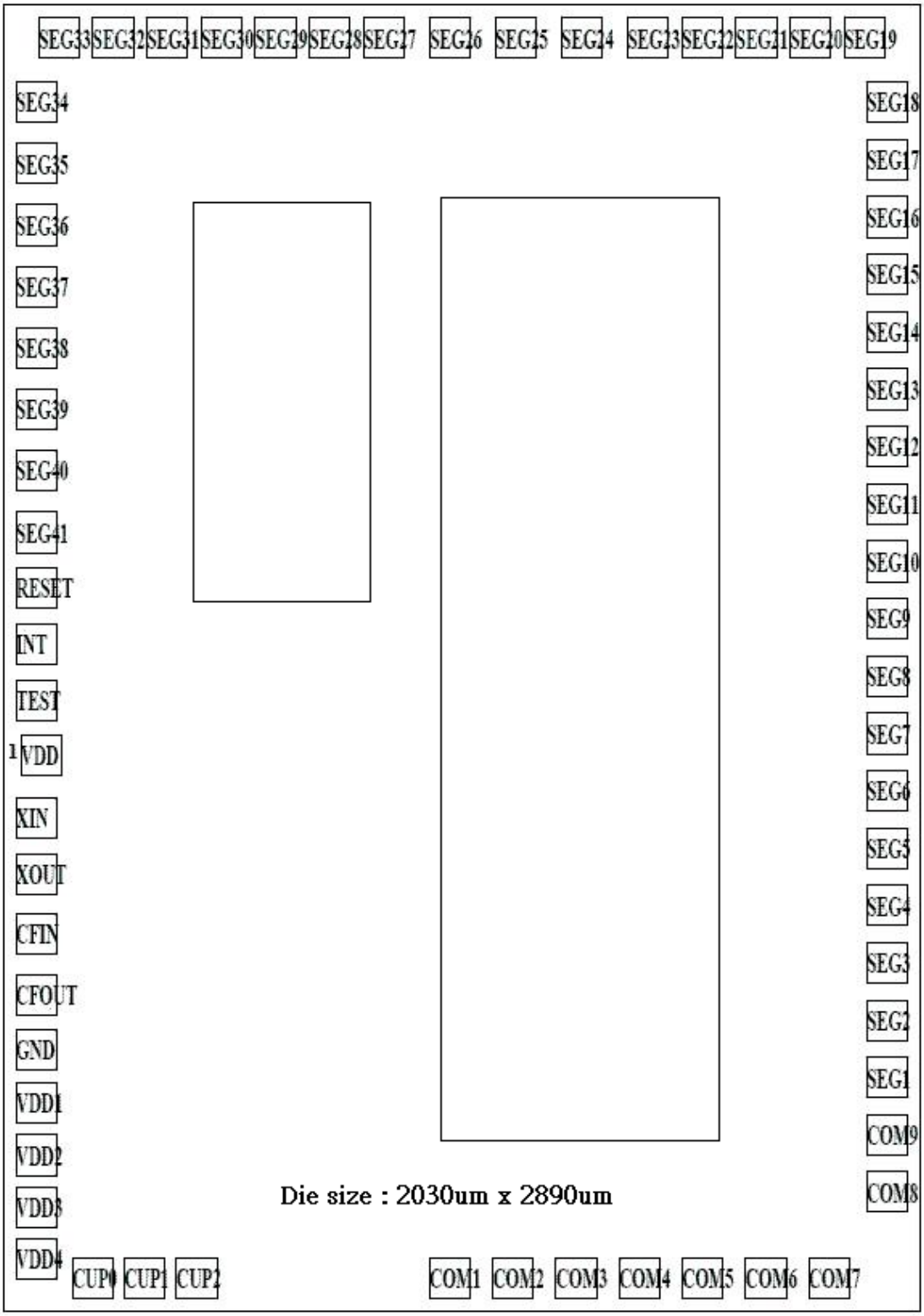
APPLICATION

- Timer/Calendar/Calculator/Thermometer

BLOCK DIAGRAM



PAD DIAGRAM



The substrate of chip should be connected to GND.

PAD COORDINATE

No	Name	X	Y	No	Name	X	Y
1	BAK	83.00	1229.20	34	SEG12(K12)	1957.50	1913.10
2	XIN	72.50	1090.30	35	SEG13(K13)	1957.50	2040.10
3	XOUT	72.50	965.40	36	SEG14(K14)	1957.50	2167.10
4	CFIN	72.50	835.40	37	SEG15(K15)	1957.50	2294.10
5	CFOUT	72.50	699.80	38	SEG16(K16)	1957.50	2421.10
6	GND	72.50	577.80	39	SEG17	1957.50	2548.10
7	VDD1	72.50	459.80	40	SEG18	1957.50	2675.10
8	VDD2	72.50	344.80	41	SEG19	1907.50	2817.50
9	VDD3	72.50	229.80	42	SEG20	1787.50	2817.50
10	VDD4	72.50	114.80	43	SEG21	1667.50	2817.50
11	CUP0	197.50	72.50	44	SEG22	1547.50	2817.50
12	CUP1	312.50	72.50	45	SEG23	1427.50	2817.50
13	CUP2	427.50	72.50	46	SEG24/IOA1/CX	1281.00	2817.50
14	COM1	988.80	72.50	47	SEG25/IOA2/RR	1135.00	2817.50
15	COM2	1128.80	72.50	48	SEG26/IOA3/RT	989.00	2817.50
16	COM3	1268.80	72.50	49	SEG27/IOA4/RH	843.00	2817.50
17	COM4	1408.80	72.50	50	SEG28/IOB1/ELC	722.50	2817.50
18	COM5	1548.80	72.50	51	SEG29/IOB2/ELP	602.50	2817.50
19	COM6	1688.80	72.50	52	SEG30/IOB3/BZB	482.50	2817.50
20	COM7	1828.80	72.50	53	SEG31/IOB4/BZ	362.50	2817.50
21	COM8	1957.50	263.10	54	SEG32/IOC1/KI1	242.50	2817.50
22	COM9	1957.50	388.10	55	SEG33/IOC2/KI2	122.50	2817.50
23	SEG1(K1)	1957.50	516.10	56	SEG34/IOC3/KI3	72.50	2675.40
24	SEG2(K2)	1957.50	643.10	57	SEG35/IOC4/KI4	72.50	2539.40
25	SEG3(K3)	1957.50	770.10	58	SEG36/IOD1	72.50	2403.40
26	SEG4(K4)	1957.50	897.10	59	SEG37/IOD2	72.50	2267.40
27	SEG5(K5)	1957.50	1024.10	60	SEG38/IOD3	72.50	2131.40
28	SEG6(K6)	1957.50	1151.10	61	SEG39/IOD4	72.50	1995.40
29	SEG7(K7)	1957.50	1278.10	62	SEG40	72.50	1859.40
30	SEG8(K8)	1957.50	1405.10	63	SEG41	72.50	1723.40
31	SEG9(K9)	1957.50	1532.10	64	RESET	72.50	1600.70
32	SEG10(K10)	1957.50	1659.10	65	INT	72.50	1475.70
33	SEG11(K11)	1957.50	1786.10	66	TEST	72.50	1350.70

PIN DESCRIPTION

Name	I/O	Description
BAK	P	Positive Back-up voltage. At Li power mode, connect a 0.1u capacitor to GND.
VDD1,2,3,4	P	LCD supply voltage, and positive supply voltage. • In Ag Mode, connect positive power to VDD1. • In Li or ExtV power mode, connect positive power to VDD2.
RESET	I	Input pin for external reset request signal, built-in internal pull-down resistor.
INT	I	Input pin for external INT request signal. • Falling edge or rising edge triggered is defined by mask option. • Internal pull-down or pull-up resistor is defined by mask option.
TEST		Test signal input pin.
CUP0,1,2	O	Switching pins for supply the LCD driving voltage to the VDD1, 2,3,4 pins. • Connect the CUP0, CUP1 and CUP2 pins with non-polarized electrolytic capacitors when chip operated in 1/2, 1/3 or 1/4 bias mode. • In no BIAS mode application, leave these pins opened.
XIN XOUT	I O	Time base counter frequency (clock specified. LCD alternating frequency. Alarm signal frequency) or system clock oscillation. • The usage of 32 KHz Crystal oscillator or external RC oscillator is defined by mask option.
CFIN CFOUT	I O	System clock oscillation for FAST clock only or DUAL clock operation. • The usage of 3.58MHz ceramic/resonator oscillator or external R type oscillator is defined by mask option
COM1~9	O	Output pins for driving the common pins of the LCD panel. COM5~9 could be defined as COMS or Open Drain type output.
SEG1-41	O	Output pins for driving the LCD panel segment.
IOA1-4	I/O	Input/Output port A, (muxed with SEG24~27)
IOB1-4	I/O	Input/Output port B, (muxed with SEG28~31)
IOC1-4	I/O	Input/Output port C, (muxed with SEG32~35)
IOD1~4	I/O	Input/Output port D, (muxed with SEG36~39)
CX RR/RT/RH	I O	1 input pin and 3 output pins for RFC application. (muxed with SEG24~27)
ELC/ELP	O	Output port for El panel driver. (muxed with SEG28~29)
BZB/BZ	O	Output port for alarm, clock or single tone melody generator. (muxed with SEG30~31)
K1~K16	O	Output port for key matrix scanning. (Shared with SEG1~SEG16)
KI1~4	I	Input port for key matrix scanning. (Muxed with SEG32~SEG35)
GND	P	Negative supply voltage.

ABSOLOUTE MAXIMUM RATINGS

GND=0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD1	-0.3 to 5.5	V
	VDD2	-0.3 to 5.5	
	VDD3	-0.3 to 8.5	
	VDD4	-0.3 to 8.5	
Maximum Input Voltage	Vin	-0.3 to VDD1/2 +0.3	
Maximum output Voltage	Vout1	-0.3 to VDD1/2 +0.3	
	Vout2	-0.3 to VDD3 +0.3	
	Vout3	-0.3 to VDD4 +0.3	
Maximum Operating Temperature	Topg	-20 to +70	°C
Maximum Storage Temperature	Tstg	-40 to +125	

POWER CONSUMPTION

at Ta= -20°C to 70°C, GND=0V

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
HALT mode	IHALT1	Only 32.768 KHz Crystal oscillator operating, without loading. Ag mode, VDD1=1.5V, BCF=0		2		uA
	IHALT2	Only 32.768 KHz Crystal oscillator operating, without loading. Li mode, VDD2=3.0V, BCF=0		2		
STOP mode	ISTOP				1	

Note: When RC oscillator function is operating, the current consumption will depend on the frequency of oscillation.

ALLOWABLE OPERATING CONDITIONS

at Ta= -20°C to 70°C, GND=0V

Name	Symb.	Condition	Min.	Max.	Unit
Supply Voltage	VDD1		1.2	5.4	V
	VDD2		2.4	5.4	
	VDD3		2.4	8.0	
	VDD4		2.4	8.0	
Oscillator Start-Up Voltage	VDDB	Crystal Mode	1.3		
Oscillator Sustain Voltage	VDDB		1.2		
Supply Voltage	VDD1	Ag Mode	1.2	1.8	
Supply Voltage	VDD2	EXT-V, Li Mode	2.4	5.4	
Input “H” Voltage	Vih1	Ag Battery Mode	VDD1-0.7	VDD1+0.7	
Input “L” Voltage	Vil1		-0.7	0.7	
Input “H” Voltage	Vih2	Li Battery Mode	VDD2-0.7	VDD2+0.7	
Input “L” Voltage	Vil2		-0.7	0.7	
Input “H” Voltage	Vih3	OSCIN at Ag Battery Mode	0.8xVDD1	VDD1	
Input “L” Voltage	Vil3		0	0.2xVDD1	
Input “H” Voltage	Vih4	OSCIN at Li Battery Mode	0.8xVDD2	VDD2	
Input “L” Voltage	Vil4		0	0.2xVDD2	
Input “H” Voltage	Vih5	CFIN at Li Battery or EXT-V Mode	0.8xVDD2	VDD2	
Input “L” Voltage	Vil5		0	0.2xVDD2	
Input “H” Voltage	Vih6	RC Mode	0.8xVDDO	VDDO	
Input “L” Voltage	Vil6		0	0.2xVDDO	
Operating Freq	Fopg1	Crystal Mode	32		KHz
	Fopg2	RC Mode	10	1000	
	Fopg3	CF Mode	1000	3580	

ALLOWABLE OPERATING FREQUENCY

at Ta= -20°C to 70°C, GND=0V

Condition	Max, Operating Frequency
BAK=1.5V (VDD1)	800 KHz
BAK=3V (VDD2)	4 MHz

INTERNAL RC FREQUENCY RANGE

Option Mode	BAK	Min.	Typ.	Max.
250 KHz	1.5V	200 KHz	300 KHz	400 KHz
	3.0V	200 KHz	250 KHz	300 KHz
500 KHz	1.5V	400 KHz	500 KHz	600 KHz
	3.0V	400 KHz	500 KHz	600 KHz

ELECTRICAL CHARACTERISTICS

at#1: VDD1=1.2V (Ag) ;

at#2: VDD2=2.4V (Li) :

at#3: VDD2=4V (Ext-V) ;

Input Resistance

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
"L" Level Hold Tr(IOC)	Rllh1	Vi=0.2VDD1, #1	10	40	100	KΩ
	Rllh2	Vi=0.2VDD2, #2	10	40	100	
	Rllh3	Vi=0.2VDD2, #3	5	20	50	
IOC Pull-Down Tr	Rmad1	Vi=VDD1, #1	200	500	1000	
	Rmad2	Vi=VDD2, #2	200	500	1000	
	Rmad3	Vi=VDD2, #3	100	250	500	
INT Pull-up Tr	Rintu1	Vi=VDD1, #1	200	500	1000	
	Rintu2	Vi=VDD2, #2	200	500	1000	
	Rintu3	Vi=VDD2, #3	100	250	500	
INT Pull-Down Tr	Rintd1	Vi=GND, #1	200	500	1000	
	Rintd2	Vi=GND, #2	200	500	1000	
	Rintd3	Vi=GND, #3	100	250	500	
RES Pull-Down R	Rres1	Vi=GND or VDD1, #1	10	40	100	
	Rres2	Vi=GND or VDD2, #2	10	40	100	
	Rres3	Vi=GND or VDD2, #3	10	40	100	

DC Output Characteristics

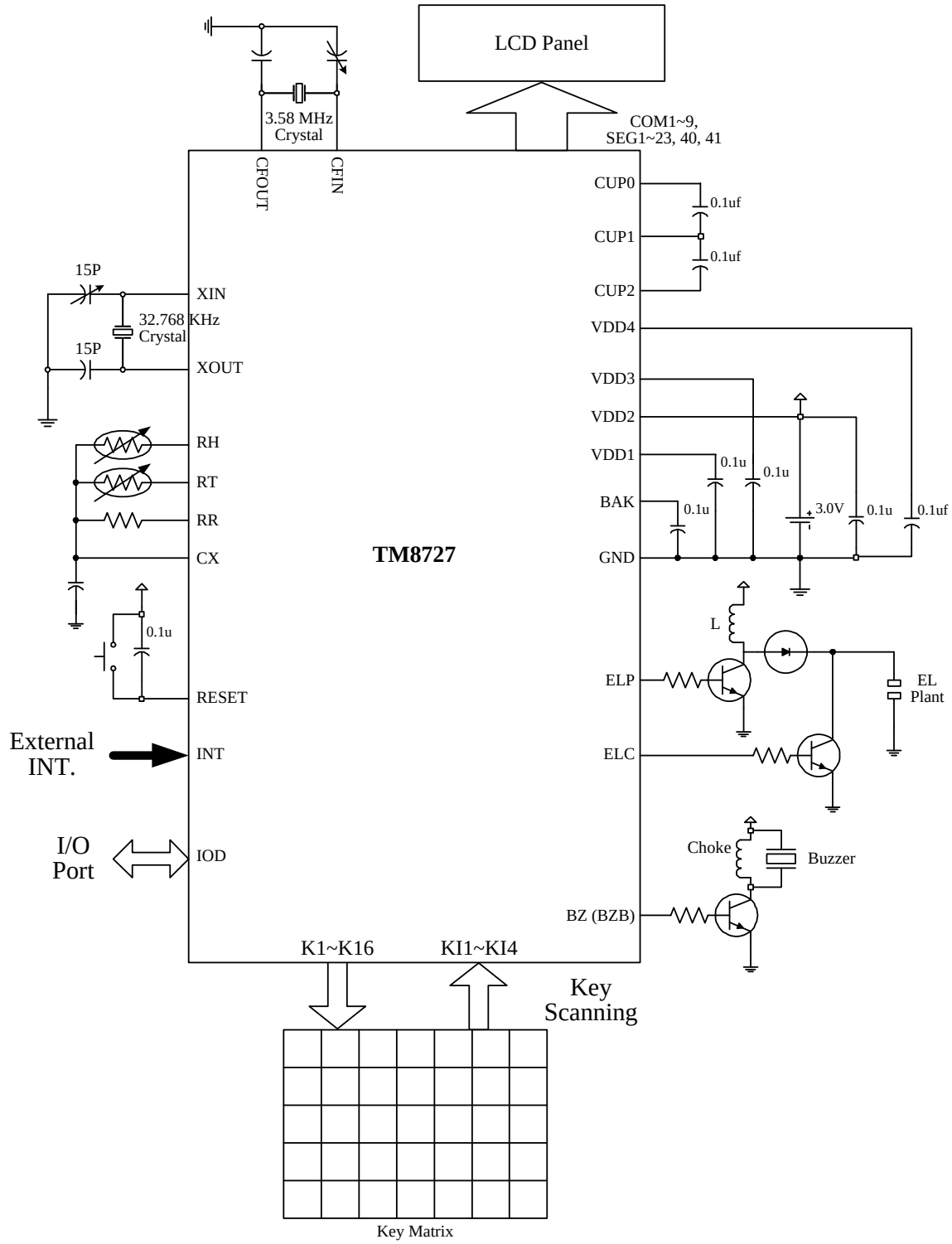
Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output "H" Voltage	Voh1c	Ioh=-200uA, #1	COM5~9 SEG1~41	0.8	0.9	1.0	V
	Voh2c	Ioh=-1mA, #2		1.5	1.8	2.1	
	Voh3c	Ioh=-3mA, #3		2.5	3.0	3.5	
Output "L" Voltage	Vol1c	Iol=400uA, #1		0.2	0.3	0.4	
	Vol2c	Iol=2mA, #2		0.3	0.6	0.9	
	Vol3c	Iol=6mA, #3		0.5	1.0	1.5	

Segment Driver Output Characteristics

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit.
1/2 Bias Display Mode							
Output ”H” Voltage	Voh12f	Ioh= -1uA, #1, #2	SEG-n	2.2			V
	Voh3f	Ioh= -1uA, #3		3.8			
Output ”L” Voltage	Vol12f	Iol=1uA, #1, #2				0.2	
	Vol3f	Iol=1uA, #3				0.2	
Output ”H” Voltage	Voh12g	Ioh= -10uA, #1, #2	COM-n	2.2			
	Voh3g	Ioh= -10uA, #3		3.8			
Output ”M” Voltage	Vom12g	Iol/h= +/-10uA, #1, #2		1.0		1.4	
	Vom3g	Iol/h= +/-10uA, #3		1.8		2.2	
1/3 Bias display Mode							
Output ”H” Voltage	Voh12h	Ioh= -1uA, #1, #2	SEG-n	3.4			V
	Voh3h	Ioh= -1uA, #3		5.8			
Output ”M1” Voltage	Vom1h	Iol/h= +/-10uA, #1, #2		1.0		1.4	
	Vom13h	Iol/h= +/-10uA, #3		1.8		2.2	
Output ”M2” Voltage	Vom22h	Iol/h= +/-10uA, #1, #2		2.2		2.6	
	Vom23h	Iol/h= +/-10uA, #3		3.8		4.2	
Output ”L” Voltage	Vol12h	Iol=1uA, #1, #2				0.2	
	Vol3h	Iol=1uA, #3				0.2	
Output ”H” Voltage	Voh12i	Ioh= -10uA, #1, #2	COM-n	3.4			
	Voh3i	Ioh= -10uA,#3		5.8			
Output ”M1” Voltage	Vom12i	Iol/h= +/-10uA, #1, #2		1.0		1.4	
	Vom13i	Iol/h= +/-10uA, #3		1.8		2.2	
Output ”M2” Voltage	Vom22i	Iol/h= +/-10uA, #1, #2		2.2		2.6	
	Vom23i	Iol/h= +/-10uA, #3		3.8		4.2	
Output ”L” Voltage	Vol12i	Iol=10uA, #1, #2				0.2	
	Vol3i	Iol=10uA, #3				0.2	
1/4 Bias display Mode							
Output ”H” Voltage	Voh12j	Ioh= -1uA, #1, #2	SEG-n	4.6			V
Output ”M2” Voltage	Vom22j	Iol/h= +/-10uA, #1, #2		2.2		2.6	
Output ”L” Voltage	Vol12j	Iol=1uA, #1, #2				0.2	
Output ”H” Voltage	Voh12k	Ioh= -10uA, #1, #2	COM-n	4.6			
Output ”M1” Voltage	Vom12k	Iol/h= +/-10uA, #1, #2		1.0		1.4	
Output ”M3” Voltage	Vom22k	Iol/h= +/-10uA, #1, #2		3.4		3.8	
Output ”L” Voltage	Vol12k	Iol=10uA, #1, #2				0.2	

TYPICAL APPLICATION CIRCUIT

This application circuit is simply an example, and is not guaranteed to work.



Li power mode, 1/4 Bias, 1/9 Duty

Appendix A TM8727 Instruction Table

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
LCT	Lz,Ry	0000 001Z ZZZZ ZYYY	(Lz)	← 7SEG ← (Ry)	Ry=70H~77H
LCB	Lz,Ry	0000 010Z ZZZZ ZYYY	(Lz)	←7SEG ← (Ry)	Blank Zero
LCP	Lz,Ry	0000 011Z ZZZZ ZYYY	(Lz)	← (Ry) , (AC)	
LCD	Lz,@HL	0000 100Z ZZZZ Z000	(Lz)	← (R@HL)	
LCT	Lz,@HL	0000 100Z ZZZZ Z001	(Lz)	←7SEG ← (R@HL)	
LCB	Lz,@HL	0000 100Z ZZZZ Z010	(Lz)	←7SEG ← (R@HL)	Blank Zero
LCP	Lz,@HL	0000 100Z ZZZZ Z011	(Lz)	← (R@HL) , (AC)	
LCDX	D	0000 100D D000 0100	(Multi-Lz) D=00 D=01 D=10 D=11	← (T@HL) : Multi-Lz=00H~0FH : Multi-Lz=10H~1FH : Multi-Lz=20H~2FH : Multi-Lz=30H~3FH	
LCTX	D	0000 100D D000 0101	((Multi-Lz) D=00 D=01 D=10 D=11	←7SEG ←(R @HL) : Multi-Lz=00H~0FH : Multi-Lz=10H~1FH : Multi-Lz=20H~2FH : Multi-Lz=30H~3FH	
LCBX	D	0000 100D D000 0110	(Multi-Lz) D=00 D=01 D=10 D=11	←7SEG ←(R @HL) : Multi-Lz=00H~0FH : Multi-Lz=10H~1FH : Multi-Lz=20H~2FH : Multi-Lz=30H~3FH	Blank Zero
LCPX	D	0000 100D D000 0111	(Multi-Lz) D=00 D=01 D=10 D=11	←(R@HL) , (AC) : Multi-Lz=00H~0FH : Multi-Lz=10H~1FH : Multi-Lz=20H~2FH : Multi-Lz=30H~3FH	
OPA	Rx	0000 1010 0XXX XXXX	(IOA)	← (Rx)	
OPAS	Rx,D	0000 1011 DXXX XXXX	IOA1,2,3,4	← (Rx)0,(Rx)1,D,Pulse	
OPB	Rx	0000 1100 0XXX XXXX	(IOB)	← (Rx)	
OPC	Rx	0000 1101 0XXX XXXX	(IOC)	← (Rx)	
OPD	Rx	0000 1110 0XXX XXXX	(IOD)	← (Rx)	
FRQ	D,Rx	0001 00DD 0XXX XXXX	FREQ D=00 D=01 D=10 D=11	← (Rx) , (AC) : 1/4 Duty : 1/3 Duty : 1/2 Duty : 1/1 Duty	
FRQ	D,@HL	0001 01DD 0000 0000	FREQ	←(T@HL)	
FRQX	D,X	0001 10DD XXXX XXXX	FREQ	← X	
MVL	Rx	0001 1100 0XXX XXXX	(@L)0~3	← (Rx)	
MVH	Rx	0001 1101 0XXX XXXX	(@H)4~7	← (Rx)	
MVU	Rx	0001 1110 0XXX XXXX	(@U)8~11	← (Rx)	
ADC	Rx	0010 0000 0XXX XXXX	(AC)	← (Rx) + (AC) + CF	CF
ADC	@HL	0010 0000 1000 0000	(AC)	← (R@HL) + (AC) + CF	CF
ADC#	@HL	0010 0000 1100 0000	(AC) (@HL)	←(R@HL) + (AC) + CF ←(@HL)+1	CF
ADC*	Rx	0010 0001 0XXX XXXX	(AC),(Rx)	←(Rx) + (AC) + CF	CF
ADC*	@HL	0010 0001 1000 0000	(AC), (R@HL)	←(R@HL) + (AC) + CF	CF
ADC*#	@HL	0010 0001 1100 0000	(AC), (R@HL) (@HL)	←(R@HL) + (AC) + CF ←(@HL)+1	CF
SBC	Rx	0010 0010 0XXX XXXX	(AC)	←(Rx) + (AC)B + CF	CF
SBC	@HL	0010 0010 1000 0000	(AC)	←(R@HL) + (AC)B + CF	CF
SBC#	@HL	0010 0010 1100 0000	(AC) (@HL)	←(R@HL) + (AC)B + CF ←(@HL)+1	CF
SBC*	Rx	0010 0011 0XXX XXXX	(AC), (R@HL)	←(R@HL) + (AC)B + CF	CF
SBC*	@HL	0010 0011 1000 0000	(AC), (R@HL)	←(R@HL) + (AC)B + CF	CF

Instruction		Machine Code	Function		Flag/Remark
SBC*#	@HL	0010 0011 1100 0000	(AC),(R@HL) (@HL)	←(R@HL) + (AC)B + CF ←(@HL)+1	CF
ADD	Rx	0010 0100 0XXX XXXX	(AC)	← (Rx) + (AC)	CF
ADD	@HL	0010 0100 1000 0000	(AC)	←(R@HL) + (AC)	CF
ADD#	@HL	0010 0100 1100 0000	(AC) (@HL)	←(R@HL) + (AC) ←(@HL)+1	CF
ADD*	Rx	0010 0101 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC)	CF
ADD*	@HL	0010 0101 1000 0000	(AC), (R@HL)	←(R@HL) + (AC)	CF
ADD*#	@HL	0010 0101 1100 0000	(AC), (R@HL) (@HL)	←(R@HL) + (AC) ←(@HL)+1	CF
SUB	Rx	0010 0110 0XXX XXXX	(AC)	← (Rx) + (AC)B + 1	CF
SUB	@HL	0010 0110 1000 0000	(AC)	←(R@HL) + (AC)B + 1	CF
SUB#	@HL	0010 0110 1100 0000	(AC) (@HL)	←(R@HL) + (AC)B + 1 ←(@HL)+1	CF
SUB*	Rx	0010 0111 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC)B + 1	CF
SUB*	@HL	0010 0111 1000 0000	(AC), (R@HL)	←(R@HL) + (AC)B + 1	CF
SUB*#	@HL	0010 0111 1100 0000	(AC), (R@HL) (@HL)	←(R@HL) + (AC)B + 1 ←(@HL)+1	CF
ADN	Rx	0010 1000 0XXX XXXX	(AC)	← (Rx) + (AC)	
ADN	@HL	0010 1000 1000 0000	(AC)	←(R@HL) + (AC)	
ADN#	@HL	0010 1000 1100 0000	(AC) (@HL)	←(R@HL) + (AC) ←(@HL)+1	
ADN*	Rx	0010 1001 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC)	
ADN*	@HL	0010 1001 1000 0000	(AC), (R@HL)	←(R@HL) + (AC)	
ADN*#	@HL	0010 1001 1100 0000	(AC), (R@HL) (@HL)	←(R@HL) + (AC) ←(@HL)+1	
AND	Rx	0010 1010 0XXX XXXX	(AC)	← (Rx) AND (AC)	
AND	@HL	0010 1010 1000 0000	(AC)	←(R@HL) AND (AC)	
AND#	@HL	0010 1010 1100 0000	(AC) (@HL)	←(R@HL) AND (AC) ←(@HL)+1	
AND*	Rx	0010 1011 0XXX XXXX	(AC),(Rx)	← (Rx) AND (AC)	
AND*	@HL	0010 1011 1000 0000	(AC), (R@HL)	←(R@HL) AND (AC)	
AND*#	@HL	0010 1011 1100 0000	(AC),(R@HL) (@HL)	← (R@HL) AND (AC) ←(@HL)+1	
EOR	Rx	0010 1100 0XXX XXXX	(AC)	← (Rx) EOR (AC)	
EOR	@HL	0010 1100 1000 0000	(AC)	← (R@HL) EOR (AC)	
EOR#	@HL	0010 1100 1100 0000	(AC) (@HL)	← (R@HL) EOR (AC) ←(@HL)+1	
EOR*	Rx	0010 1101 0XXX XXXX	(AC),(Rx)	← (Rx) EOR (AC)	
EOR*	@HL	0010 1101 1000 0000	(AC),(R@HL)	← (R@HL) EOR (AC)	
EOR*#	@HL	0010 1101 1100 0000	(AC),(R@HL) (@HL)	← (R@HL) EOR (AC) ←(@HL)+1	
OR	Rx	0010 1110 0XXX XXXX	(AC)	← (Rx) OR (AC)	
OR	@HL	0010 1110 1000 0000	(AC)	← (R@HL) OR (AC)	
OR#	@HL	0010 1110 1100 0000	(AC) (@HL)	← (R@HL) OR (AC) ←(@HL)+1	
OR*	Rx	0010 1111 0XXX XXXX	(AC),(Rx)	← (Rx) OR (AC)	
OR*	@HL	0010 1111 1000 0000	(AC),(R@HL)	← (R@HL) OR (AC)	
OR*#	@HL	0010 1111 1100 0000	(AC),(R@HL) (@HL)	← (R@HL) OR (AC) ←(@HL)+1	
ADCI	Ry,D	0011 0000 DDDD YYYY	(AC)	← (Ry) + D + CF	CF
ADCI*	Ry,D	0011 0001 DDDD YYYY	(AC),(Ry)	← (Ry) + D + CF	CF
SBCI	Ry,D	0011 0010 DDDD YYYY	(AC)	← (Ry) + D(B) + CF	CF
SBCI*	Ry,D	0011 0011 DDDD YYYY	(AC),(Ry)	← (Ry) + D(B) + CF	CF
ADDI	Ry,D	0011 0100 DDDD YYYY	(AC)	← (Ry) + D	CF
ADDI*	Ry,D	0011 0101 DDDD YYYY	(AC),(Ry)	← (Ry) + D	CF
SUBI	Ry,D	0011 0110 DDDD YYYY	(AC)	← (Ry) + D(B) + 1	CF
SUBI*	Ry,D	0011 0111 DDDD YYYY	(AC),(Ry)	← (Ry) + D(B) + 1	CF
ADNI	Ry,D	0011 1000 DDDD YYYY	(AC)	← (Ry) + D	

Instruction		Machine Code	Function		Flag/Remark
ADNI*	Ry,D	0011 1001 DDDD YYYY	(AC),(Ry)	← (Ry) + D	
ANDI	Ry,D	0011 1010 DDDD YYYY	(AC)	← (Ry) AND D	
ANDI*	Ry,D	0011 1011 DDDD YYYY	(AC),(Ry)	← (Ry) AND D	
EORI	Ry,D	0011 1100 DDDD YYYY	(AC)	← (Ry) EOR D	
EORI*	Ry,D	0011 1101 DDDD YYYY	(AC),(Ry)	← (Ry) EOR D	
ORI	Ry,D	0011 1110 DDDD YYYY	(AC)	← (Ry) OR D	
ORI*	Ry,D	0011 1111 DDDD YYYY	(AC),(Ry)	← (Ry) OR D	
INC*	Rx	0100 0000 0XXX XXXX	(AC),(Rx)	← (Rx) + 1	CF
INC*	@HL	0100 0000 1000 0000	(AC),(R@HL)	← (R@HL) + 1	CF
INC*#	@HL	0100 0000 1100 0000	(AC),(R@HL) (@HL)	← (R@HL) + 1 ←(@HL)+1	CF
DEC*	Rx	0100 0001 0XXX XXXX	(AC),(Rx)	← (Rx) – 1	CF
DEC*	@HL	0100 0001 1000 0000	(AC),(R@HL)	← (R@HL) - 1	CF
DEC*#	@HL	0100 0001 1100 0000	(AC),(R@HL) (@HL)	← (R@HL) - 1 ←(@HL)+1	CF
IPA	Rx	0100 0010 0XXX XXXX	(AC),(Rx)	← (IOA)	
IPB	Rx	0100 0100 0XXX XXXX	(AC),(Rx)	← (IOB)	
IPC	Rx	0100 0111 0XXX XXXX	(AC),(Rx)	← (IOC)	
IPD	Rx	0100 1000 0XXX XXXX	(AC),(Rx)	← (IOD)	
MAF	Rx	0100 1010 0XXX XXXX	(AC),(Rx)	← (STS1)	B3 : CF B2 : ZERO B1 : (No use) B0 : (No use)
MSB	Rx	0100 1011 0XXX XXXX	(AC),(Rx)	← (STS2)	B3 : SCF3(DPT) B2 : SCF2(HRx) B1 : SCF1(CPT) B0 : BCF
MSC	Rx	0100 1100 0XXX XXXX	(AC),(Rx)	← (STS3)	B3 : SCF7(PDV) B2 : PH15 B1 : SCF5(TM1) B0 : SCF4(INT)
MCX	Rx	0100 1101 0XXX XXXX	(AC),(Rx)	← (STS3X)	B3 : SCF9(RFC) B2 : (No use) B1 : SCF6(TM2) B0 : SCF8(SKI)
MSD	Rx	0100 1110 0XXX XXXX	(AC),(Rx)	← (STS4)	B3 : (No use) B2 : RFOVF B1 : WDF B0 : CSF
SR0	Rx	0101 0000 0XXX XXXX	(AC)n, (Rx)n (AC)3, (Rx)3	← (Rx)(n+1) ← 0	
SR1	Rx	0101 0001 0XXX XXXX	(AC)n, (Rx)n (AC)3, (Rx)3	← (Rx)(n+1) ← 1	
SL0	Rx	0101 0010 0XXX XXXX	(AC)n, (Rx)n (AC)0, (Rx)0	← (Rx)(n-1) ← 0	
SL1	Rx	0101 0011 0XXX XXXX	(AC)n, (Rx)n (AC)0, (Rx)0	← (Rx)(n-1) ← 1	
DAA		0101 0100 0000 0000	(AC)	← BCD((AC))	CF
DAA*	Rx	0101 0101 0XXX XXXX	(AC),(Rx)	← BCD((AC))	CF
DAA*	@HL	0101 0101 1000 0000	(AC),(R@HL)	← BCD((AC))	CF
DAA*#	@HL	0101 0101 1100 0000	(AC),(R@HL) (@HL)	← BCD((AC)) ←(@HL)+1	CF
DAS		0101 0110 0000 0000	(AC)	← BCD((AC))	CF
DAS*	Rx	0101 0111 0XXX XXXX	(AC),(Rx)	← BCD((AC))	CF
DAS*	@HL	0101 0111 1000 0000	(AC),(R@HL)	← BCD((AC))	CF
DAS*#	@HL	0101 0111 1100 0000	(AC),(R@HL) (@HL)	← BCD((AC)) ←(@HL)+1	CF
LDS	Rx,D	0101 1DDD DXXX XXXX	(AC),(Rx)	← D	
LDH	Rx,@HL	0110 0000 0XXX XXXX	(AC),(Rx)	← H(T@HL)	

Instruction		Machine Code	Function		Flag/Remark
LDH*	Rx,@HL	0110 0001 0XXX XXXX	(AC),(Rx) (@HL)	← H(T@HL) ←(@HL) + 1	
LDL	Rx,@HL	0110 0010 0XXX XXXX	(AC),(Rx)	← L(T@HL)	
LDL*	Rx,@HL	0110 0011 0XXX XXXX	(AC),(Rx) (@HL)	← L(T@HL) ←(@HL) + 1	
MRF1	Rx	0110 0100 0XXX XXXX	(AC),(Rx)	← (RFC)3-0	
MRF2	Rx	0110 0101 0XXX XXXX	(AC),(Rx)	← (RFC)7-4	
MRF3	Rx	0110 0110 0XXX XXXX	(AC),(Rx)	← (RFC)11-8	
MRF4	Rx	0110 0111 0XXX XXXX	(AC),(Rx)	← (RFC)15-12	
STA	Rx	0110 1000 0XXX XXXX	(Rx)	← (AC)	
STA	@HL	0110 1000 1000 0000	@HL	← (AC)	
STA#	@HL	0110 1000 1100 0000	@HL (@HL)	← (AC) ←(@HL)+1	
LDA	Rx	0110 1100 0XXX XXXX	(AC)	← (Rx)	
LDA	@HL	0100 1100 1000 0000	(AC)	← (R@HL)	
LDA#	@HL	0100 1100 1100 0000	(AC) (@HL)	← (R@HL) ←(@HL)+1	
MRA	Rx	0110 1101 0XXX XXXX	CF	← (Rx)3	
MRW	@HL,Rx	0110 1110 0XXX XXXX	(AC),(R@HL)	← (Rx)	
MRW#	@HL,Rx	0110 1110 1XXX XXXX	(AC),(R@HL) (@HL)	← (Rx) ←(@HL)+1	
MWR	Rx,@HL	0110 1111 0XXX XXXX	(AC),(Rx)	← (R@HL)	
MWR#	Rx,@HL	0110 1111 1XXX XXXX	(AC),(Rx) (@HL)	← (R@HL) ←(@HL)+1	
MRW	Ry,Rx	0111 0YYY YXXX XXXX	(AC),(Ry)	← (Rx)	
MWR	Rx,Ry	0111 1YYY YXXX XXXX	(AC),(Rx)	← (Ry)	
JB0	X	1000 0XXX XXXX XXXX	(PC)	← X(x000h~x7FFh ; x800h~xFFFh)	if (AC)0 = 1
JB1	X	1000 1XXX XXXX XXXX	(PC)	← X(x000h~x7FFh ; x800h~xFFFh)	if (AC)1 = 1
JB2	X	1001 0XXX XXXX XXXX	(PC)	← X(x000h~x7FFh ; x800h~xFFFh)	if (AC)2 = 1
JB3	X	1001 1XXX XXXX XXXX	(PC)	← X(x000h~x7FFh ; x800h~xFFFh)	if (AC)3 = 1
JNZ	X	1010 0XXX XXXX XXXX	(PC)	← X(x000h~x7FFh ; x800h~xFFFh)	if (AC) ≠ 0
JNC	X	1010 1XXX XXXX XXXX	(PC)	← X(x000h~x7FFh ; x800h~xFFFh)	if CF = 0
JZ	X	1011 0XXX XXXX XXXX	(PC)	← X(x000h~x7FFh ; x800h~xFFFh)	if (AC) = 0
JC	X	1011 1XXX XXXX XXXX	(PC)	← X(x000h~x7FFh ; x800h~xFFFh)	if CF = 1
CALL	X	1100 XXXX XXXX XXXX	(STACK) (PC)	← (PC) + 1 ← X (0000h~2FFFh)	Jump BANK is processed by Compiler
JMP	X	1101 XXXX XXXX XXXX	(PC)	← X (0000h~2FFFh)	Jump BANK is processed by Compiler
TMS	Rx	1110 0000 0XXX XXXX	(AC)3,2 = 11 (AC)3,2 = 10 (AC)3,2 = 01 (AC)3,2 = 00 (AC)1~0, (Rx)3~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	Setting of Timer 1
TMS	@HL	1110 0001 0000 0000	(T@HL)7,6 = 11 (T@HL)7,6 = 10 (T@HL)7,6 = 01	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	Setting of Timer 1

Instruction		Machine Code	Function		Flag/Remark
			(T@HL)7,6 = 00 (T@HL)5~0		
TMSX	X	1110 001X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	Setting of Timer 1
TM2	Rx	1110 0100 0XXX XXXX	(AC)3,2 = 11 (AC)3,2 = 10 (AC)3,2 = 01 (AC)3,2 = 00 (AC)1~0, (Rx)3~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	Setting of Timer 2
TM2	@HL	1110 0101 0000 0000	(T@HL)7,6 = 11 (T@HL)7,6 = 10 (T@HL)7,6 = 01 (T@HL)7,6 = 00 (T@HL)5~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	Setting of Timer 2
TM2X	X	1110 011X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer2 Value	Setting of Timer 2
SHE	X	1110 1000 0XXX XXX0	X6 X5 X4 X3 X2 X1	: Enable HEF6 : Enable HEF5 : Enable HEF4 : Enable HEF3 : Enable HEF2 : Enable HEF1	RFC KEY_S TMR2 PDV INT TMR1
SIE*	X	1110 1001 0XXX XXXX	X6 X5 X4 X3 X2 X1 X0	: Enable IEF6 : Enable IEF5 : Enable IEF4 : Enable IEF3 : Enable IEF2 : Enable IEF1 : Enable IEF0	RFC KEY_S TMR2 PDV INT TMR1 C,DPT
PLC	X	1110 101X 0XXX XXXX	X8 X6-0	: Reset PH15~11 : Reset HRF6-0	
SRF	X	1110 1100 00XX XXXX	X5 X4 X3 X2 X1 X0	: Enable Cx Control : Enable TM2 Control : Enable Counter : Enable RH Output : Enable RT Output : Enable RR Output	ENX EHM ETP ERR
SRE	X	1110 1101 X0XX X000	X7 X5 X4 X3	: Enable SRF7 : Enable SRF5 : Enable SRF4 : Enable SRF3	SRF7(KEY_S) SRF5 (INT) SRF4 (C Port) SRF3 (D port)

Instruction		Machine Code	Function		Flag/Remark
FAST		1110 1110 0000 0000		: Switch to High Speed Clock	
SLOW		1110 1110 1000 0000		: Switch to Low Speed Clock	
CPHL	X	1110 1111 XXXX XXXX		Skip next instruction when X7~0=(@HL)7~0	
SPKX	X	1111 0010 XXXX XXXX	X6=1 X6=0 X7,5,4=000 X7,5,4=001 X7,5,4=010 X7,5,4=10X X7,5,4=110 X7,5,4=111	: KEY_S release by scanning cycle : KEY_S release by normal key scanning : Set one of KO1~16 =1 by X3~0 : Set all = 1 : Set all Hi-z : Set eight of KO1~16 =1 by X3 X3=0 => KO1~8 X3=1 => KO9~16 : Set four of KO1~16 =1 by X3,2 X3,2=00 => KO1~4 X3,2=01 => KO5~8 X3,2=10 => KO9~12 X3,2=11 => KO13~16 : Set two of KO1~16 =1 by X3,2,1 X3~1=000=>KO1,2 X3~1=001=>KO3,4 X3~1=010=>KO5,6 X3~1=011=>KO7,8 X3~1=100=>KO9,10 X3~1=101=>KO11,12 X3~1=110=>KO13,14 X3~1=111=>KO15,16	
SPK	Rx	1111 0000 0XXX XXXX	(AC)2=1 (AC)2=0 (AC)7,5,4=000 (AC)7,5,4=001 (AC)7,5,4=010 (AC)7,5,4=10X (AC)7,5,4=110 (AC)7,5,4=111	: KEY_S release by scanning cycle : KEY_S release by normal key scanning : Set one of KO1~16 =1 by (Rx)3~0 : Set all = 1 : Set all Hi-z : Set eight of KO1~16 =1 by (Rx)3 (Rx)3=0 => KO1~8 (Rx)3=1 => KO9~16 : Set four of KO1~16 =1 by (Rx)3,2 (Rx)3,2=00 => KO1~4 (Rx)3,2=01 => KO5~8 (Rx)3,2=10 => KO9~12 (Rx)3,2=11 => KO13~16 : Set two of KO1~16 =1 by X3,2,1 (Rx)3~1=000=>KO1,2 (Rx)3~1=001=>KO3,4 (Rx)3~1=010=>KO5,6 (Rx)3~1=011=>KO7,8 (Rx)3~1=100=>KO9,10 (Rx)3~1=101=>KO11,12 (Rx)3~1=110=>KO13,14 (Rx)3~1=111=>KO15,16	

Instruction		Machine Code	Function		Flag/Remark
SPK	@HL	1111 0001 0000 0000	(T@HL)6=1 (T@HL)6=0 (T@HL)7,5,4 = 000 (T@HL)7,5,4 = 001 (T@HL)7,5,4 = 010 (T@HL)7,5,4 = 10X (T@HL)7,5,4 = 110 (T@HL)7,5,4 = 111	: KEY_S release by scanning cycle : KEY_S release by normal key scanning : Set one of KO1~16 =1 by (T@HL)3~0 : Set all = 1 : Set all Hi-z : Set eight of KO1~16 =1 by (T@HL)3 (T@HL)3=0 => KO1~8 (T@HL)3=1 => KO9~16 : Set four of KO1~16 =1 by (T@HL)3,2 (T@HL)3,2=00 => KO1~4 (T@HL)3,2=01 => KO5~8 (T@HL)3,2=10 => KO9~12 (T@HL)3,2=11 => KO13~16 : Set two of KO1~16 =1 by (T@HL)3,2,1 (T@HL)3~1=000=>KO1,2 (T@HL)3~1=001=>KO3,4 (T@HL)3~1=010=>KO5,6 (T@HL)3~1=011=>KO7,8 (T@HL)3~1=100=>KO9,10 (T@HL)3~1=101=>KO11,12 (T@HL)3~1=110=>KO13,14 (T@HL)3~1=111=>KO15,16	
RTS		1111 0100 0000 0000	(PC)	← STACK	CALL Return
SCC	X	1111 0100 1X0X XXXX	X6 = 1 X6 = 0 X4=1 X3=1 X2,1,0=001 X2,1,0=010 X2,1,0=100	: Cfq = BCLK : Cfq = PH0 Set IOC Cch Set IOD Cch : Cch = PH10 : Cch = PH8 : Cch = PH6	
SCA	X	1111 0101 000X X000	X4 X3	: Enable SEF4 : Enable SEF3	C1-4 D1-4
SPA	X	1111 0101 100X XXXX	X4 X3~0	: Enable IOA4-1 Pull-Low : Set IOA4-1 I/O mode	
SPB	X	1111 0101 101X XXXX	X4 X3~0	: Enable IOB4-1 Pull-Low : Set IOB4-1 I/O mode	
SPC	X	1111 0101 110X XXXX	X4 X3-0	: Enable IOC4-1 Pull-Low / Low-Level-Hold : Set IOC4-1 I/O mode	
SPD	X	1111 0101 111X XXXX	X4 X3-0	: Enable IOD4-1 Pull-Low : Set IOD4-1 I/O mode	
SF	X	1111 0110 X00X XXXX	X7 X4 X3 X2 X1 X0	: Enable TM1 Reload function : Enable watchdog timer : HALT after EL driver enable : Enable EL panel driver : Set BCF flag : Set CF	RL1 WDF BCF CF
RF	X	1111 0111 X00X 0XXX	X7	: Disable TM1 Reload	RL1

Instruction		Machine Code	Function		Flag/Remark
			X4 X2 X1 X0	function : Disable watchdog timer : Disable EL panel driver : Reset BCF : Reset CF	WDF BCF CF
ELC	X	1111 10XX XXXX XXXX	X8=1 X8=0 X7,6=11 X7,6=10 X7,6=01 X7,6=00 X9,5,4=101 X9,5,4=100 X9,5,4=x11 X9,5,4=x10 X9,5,4=001 X9,5,4=000 X3,2=11 X3,2=10 X3,2=01 X3,2=00 X1,0=11 X1,0=10 X1,0=01 X1,0=00	BCLKX PH0 BCLK/8 BCLK/4 BCLK/2 BCLK 2/3 3/4 1/1 1/2 1/3 1/4 PH5 PH6 PH7 PH8 1/1 1/2 1/3 1/4	ELP - CLK BCLKX ELP - DUTY ELC - CLK ELC - DUTY
ALM	X	1111 110X XXXX XXXX	X8,7,6=111 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: FREQ : DC “1” : PH3 : PH4 : PH5 : DC “0” ← PH15~10	
SF2	X	1111 1110 0BBB XXXX	B6 B5,4=00 B5,4=01 B5,4=10 X3 X2 X1 X0	: Enable set Program ROM bank & jump. : PC=0XXXh : PC=1XXXh : PC=2XXXh : Enable INT strong Pull-low dev. : Turn off all Segments : Set DED flag : Enable TM2 Reload function	B6,5,4 used by compiler INTPL RSOFF DED RL2
RF2	X	1111 1110 1000 XXXX	X3 X2 X1 X0	: Disable INT powerful Pull-low : Release Segments : Reset DED flag : Disable TM2 Reload function	INTPL RSOFF DED RL2
HALT		1111 1111 0000 0000	Halt Operation		
STOP		1111 1111 1000 0000	Stop Operation		

Symbol Description

Symbol	Description	Symbol	Description
( )	Content of Register	D	Immediate Data
AC	Accumulator	(D) B	Complement of Immediate Data
(AC) n	Content of Accumulator (bit n)	PC	Program Counter
(AC) B	Complement of content of Accumulator	CF	Carry Flag
X	Address of program or control data	ZERO	Zero Flag
Rx	Address X of data RAM	WDF	Watch-Dog Timer Enable Flag
(Rx)n	Bit n content of Rx	7SEG	7 segment decoder for LCD
Ry	Address Y of working register	BCLK	System clock for instruction
R@HL	Address of data RAM specified by @HL	IEFn	Interrupt Enable Flag
BCF	Back-up Flag	HRFn	HALT Release Flag
@HL	Generic Index address register	HEFn	HALT Release Enable Flag
(@HL)	Content of generic Index address register	Lz	Address of LCD PLA Latch
(@L)	Content of lowest nibble Index register	SRFn	STOP Release Enable Flag
(@H)	Content of middle nibble Index register	SCFn	Start Condition Flag
(@U)	Content of highest nibble Index register	Cch	Clock Source of Chattering prevention ckt.
T@HL	Address of Table ROM	Cfq	Clock Source of Frequency Generator
H (T@HL)	High Nibble content of Table ROM	SEFn	Switch Enable Flag
L (T@HL)	Low Nibble content of Table ROM	FREQ	Frequency Generator setting Value
TMR	Timer Overflow Release Flag	CSF	Clock Source Flag
Ctm	Clock Source of Timer	P	Program Page
PDV	Pre-Divider	RFOVF	RFC Overflow Flag
STACK	Content of stack	RFC	Resistor to Frequency counter
TM1	Timer 1	(RFC) n	Bit data of Resistor to Frequency counter
TM2	Timer 2	B	Bank set