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TM52F8658

DATA SHEET

Rev 0.92

Special for Humidifier

(Please read the precautions on the second page before use)

PRECAUTIONS

1. Chip cannot enter Stop Mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0~2)
2. Use MOVC to read flash, MOVX read flash is forbidden.

AMENDMENT HISTORY

Version	Date	Description
V0.90	Apr, 2021	New release
V0.91	Jul, 2022	1. Modify system Block Diagram
V0.92	May, 2023	1. Add CODECRC option in CFGWH

CONTENTS

$TM52_{Series}$ F85xx FAMILY

Common Features

CPU	MTP/Flash Program Memory	RAM Bytes	Dual Clock	Operation Mode	Timer0 Timer1 Timer2	UART	Real-time Timer3	LVR
Fast 8051 (2T)	4K~16K With ICP	256 ~ 512	SXT SRC FXT FRC	Fast Slow Idle Stop	8051 Standard		15-bit	2.7V 3.2V 3.8V 4.3V

Family Members Features

P/N	Program Memory	Data Memory	RAM Bytes	IO Pin	PWM	SAR ADC	OPA	CMP	Serial Interface
TM52-F8558	Flash 8K Bytes	EEPROM 128 Bytes	512	17	16-bit x2	12-bit 12-ch	1 set	5 set	Master I2C*1 UART*1
TM52-F8658	Flash 8K Bytes	EEPROM 128 Bytes	512	17	16-bit x2	12-bit 12-ch	1 set	5 set	Master I2C*1 UART*1

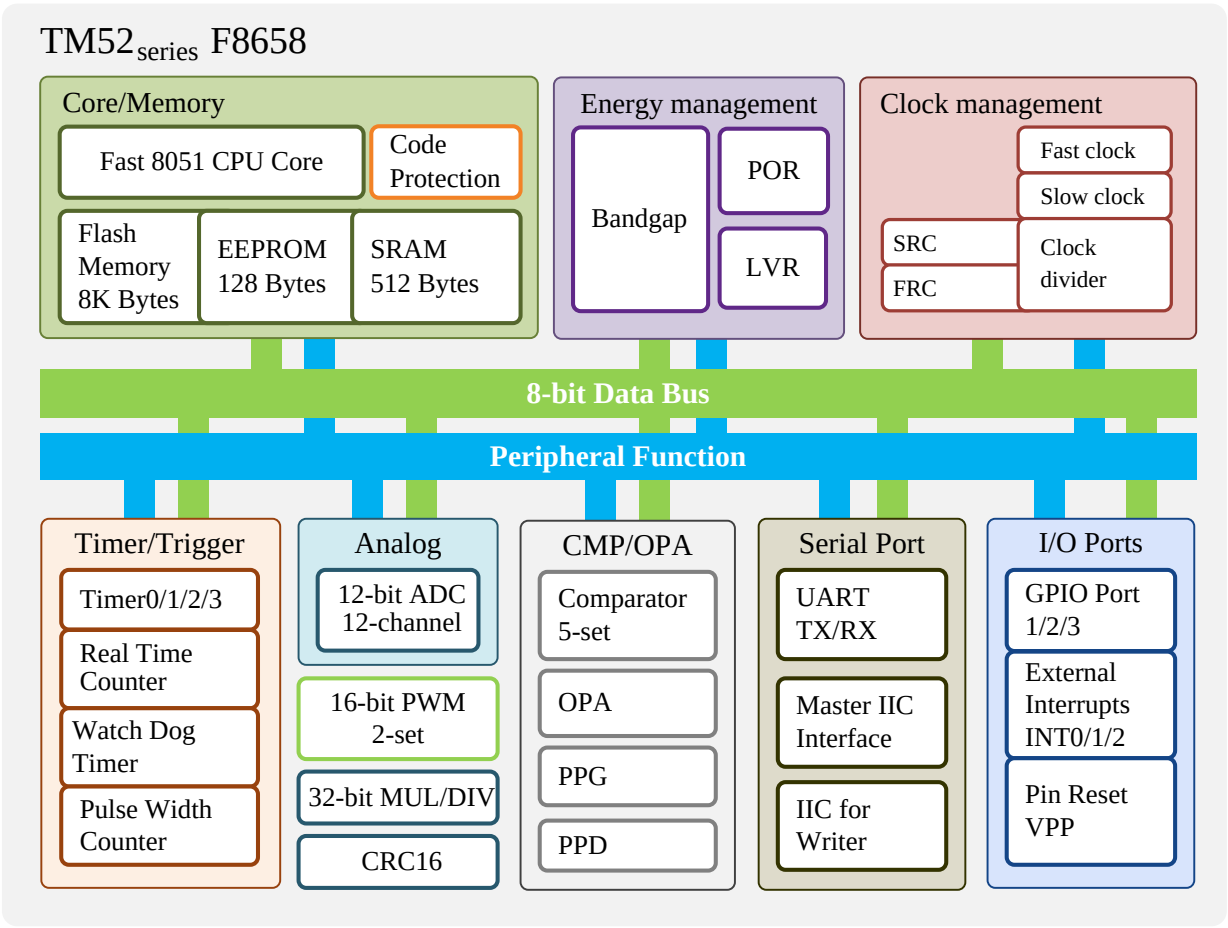
P/N	Operation Voltage	Operation Current (V_{CC}=5V) PWRSAV=1				Max. System Clock (Hz)			
		Fast FRC	Slow SRC	Idle SRC	Stop	SXT	SRC	FXT	FRC
TM52-F8558	2.7~5.5V	8.9mA	2.6mA	424μA	< 0.1μA	–	80K	–	16.588M
TM52-F8658	2.7~5.5V	8.9mA	2.6mA	424μA	< 0.1μA	–	80K	–	16.588M

GENERAL DESCRPTION

TM52 Series F8658 are versions of a new, fast 8051 architecture for an 8-bit microcontroller single chip with an instruction set fully compatible with industry standard 8051, and retains most 8051 peripheral's function block. Typically, the **TM52-F8658** executes instructions six times faster than standard 8051.

The **TM52-F8658** provides improved performance, lower cost and fast time-to-market by integrating features on the chip, including 8K Bytes Flash program memory, 128 Bytes EEPROM, 512 Bytes SRAM, Low Voltage Reset (LVR), dual clock power saving operation mode, 8051 standard UART and Timer0/1/2, real time clock Timer3, Master IIC Interface, Operational Amplifier, 5 Voltage Comparators, 2 set 16-bit PWMs, 12 channels 12-bit A/D Convertor, 9-bit Programmable Pulse Generator (PPG) and Watchdog Timer. Its high reliability and low power consumption feature can be widely applied in consumer and home appliance products.

BLOCK DIAGRAM



FEATURES

1. **Standard 8051 Instruction set, fast machine cycle**
   - Executes instructions six times faster than standard 8051
2. **8K Bytes Flash Program Memory**
   - Support “In Circuit Programming” (ICP) for the Flash code
   - Code Protection Capability
   - 10K erase times at least
   - 10 years data retention at least
3. **128 Bytes EEPROM Memory**
   - 50K erase times at least
   - 10 years data retention at least
4. **Total 512 Bytes SRAM (IRAM+XRAM)**
   - 256 Bytes IRAM in the 8051 internal data memory area
   - 256 Bytes XRAM in the 8051 external data memory area (accessed by MOVX Instruction)
5. **Two System Clock type Selections**
   - Fast clock from Internal RC (FRC, 16.5888 MHz)
   - Slow clock from Internal RC (SRC, 80 KHz)
   - System clock can be divided by 1/2/4/16 option
6. **8051 Standard Timer – Timer0/1/2**
   - 16-bit Timer0, also supports T0O clock output for Buzzer application
   - 16-bit Timer1, also supports T1O clock output for Buzzer application
   - 16-bit Timer2, also supports T2O clock output for Buzzer application
7. **15-bit Time3**
   - Clock source is Slow clock or FRC/512
   - Interrupt period can be clock divided by 32768/16384/8192/128 option
8. **8051 Standard UART**
   - One Wire UART option
9. **Two independent 16 bits PWMs with period-adjustment/buffer-reload/clear and hold function**
10. **One Master I^2C Interface**
11. **12-bit ADC with 12 Channels External Pin Input, 2 Channels Internal Reference Voltage and 1 OPA Output Voltage**
12. **Build-In OP Amp x 1 for the IGBT Current Sensing**

- Low Power Rail-to-Rail Input / Output
- Vos < |2mV| by calibration
- High Gain-Bandwidth 2.1MHz
- High Open Loop Gain 90dB
- CMRR 80dB, PSRR 80dB

13. Build-In Voltage Comparator x 5

- Vos < |2mV| by calibration
- |40mV| Hysteresis Option (Disable / Enable)
- Phase Protect Detector (PPD)

14. One 9-Bit Programmable Pulse Generator (PPG) Output Channel

- Sing Pulse Mode / Synchronous Mode
- Direct / Approach Reload Mode
- Programmable Output Delay Time (Synchronous Mode only)
- Auto-Decrement Pulse Width Control
- Over-Voltage / Over-Current Protection

15. Multiplication and division

- 8 bits Multiplier & Divider (standard 8051)
- 16 bits Multiplier & Divider
- 32 bits ÷ 16 bits hardware Divider

16. Integrated 16-bit Cyclic Redundancy Check function

17. 20 Sources, 4-level Priority Interrupt

- Timer0/Timer1/Timer2/Timer3 Interrupt
- INT0/INT1 Falling-Edge/Low-Level Interrupt
- Port1 Pin Change Interrupt
- UART TX/RX Interrupt
- P3.7 (INT2) Interrupt
- ADC Interrupt
- I2C Interrupt
- PPG/PPD Interrupt
- CMP1~5 Interrupt
- PWM0/PWM1 Interrupt

18. Pin Interrupt can Wake up CPU from Power-Down (Stop) mode

- P3.2/P3.3 (INT0/INT1) Interrupt & Wake-up
- P3.7 (INT2) Interrupt & Wake-up
- Each Port1 pin can be defined as Interrupt & Wake-up pin (by pin change)

19. Max. 17 Programmable I/O pins

- CMOS Output
- Pseudo-Open-Drain, or Open-Drain Output
- Schmitt Trigger Input
- Pin Pull-up can be Enable or Disable

20. Independent RC Oscillating Watchdog Timer

- 400ms/200ms/100ms/50ms Selectable WDT Timeout options

21. Five types Reset

- Power on Reset
- Selectable External Pin Reset
- Software Command Reset
- Selectable Watchdog Timer Reset
- Selectable Low Voltage Reset

22. 4-level Low Voltage Reset

- 2.7V/3.2V/3.8V/4.3V

23. Four Power Saving Operation Modes

- Fast/Slow/Idle/Stop Mode

24. On-chip Debug/ICE interface

- Use P3.0/P3.1 pin
- Share with ICP programming pin

25. Operating Voltage and Current

- V_{CC}=3.7V ~ 5.5V @F_{SYSCLK}=16.5888 MHz
- V_{CC}=2.5V ~ 5.5V @F_{SYSCLK}=8.2944 MHz
- I_{CC}=52μA @Stop mode, LVR enable, PWRSAV=0, V_{CC}=5V
- I_{CC}=47μA @Stop mode, LVR enable, PWRSAV=0, V_{CC}=3V
- I_{CC}<0.1μA @Stop mode, LVR disable, PWRSAV=1, V_{CC}=5V

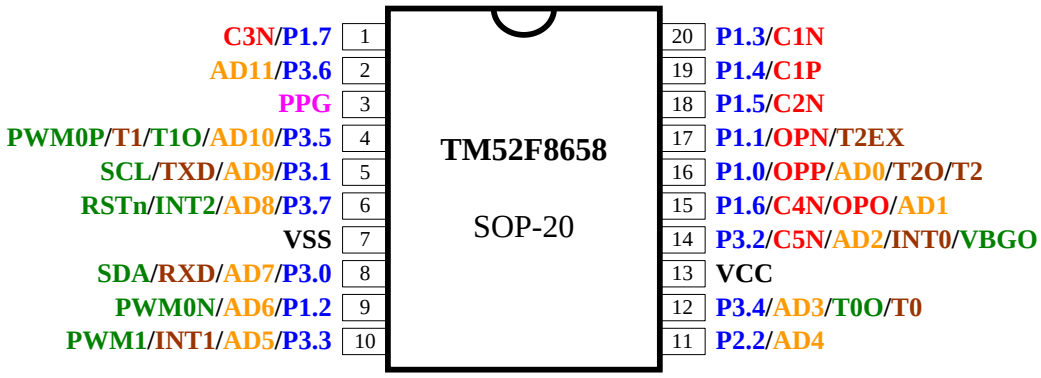
26. Operating Temperature Range

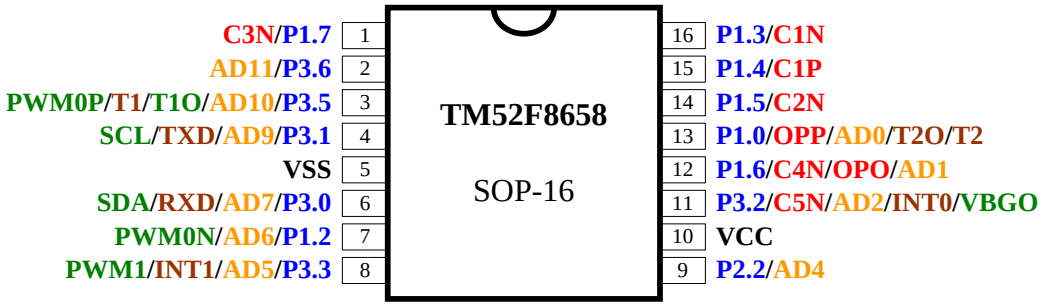
- –40°C ~ +85°C

27. Package Types

- SOP 20-pin (300 mil)
- SOP 16-pin (150 mil)

PIN ASSIGNMENT





PIN DESCRIPTION

Name	In/Out	Pin Description
P1.0~P1.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software. These pin's level change can wake up CPU from Idle/Stop mode.
P2.2	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software.
P3.0~P3.2	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "pseudo open drain" output. Pull-up resistors are assignable by software.
P3.3~P3.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software.
INT0, INT1	I	External low level or falling edge Interrupt input, Idle/Stop mode wake up input.
INT2	I	External falling edge Interrupt input, Idle/Stop mode wake up input.
RXD	I/O	UART Mode0 transmit & receive data, Mode1/2/3 receive data.
TXD	I/O	UART Mode0 transmit clock, Mode1/2/3 transmit data. In One Wire UART mode, this pin transmits and receives serial data.
T0, T1, T2	I	Timer0, Timer1, Timer2 event count pin input
T0O	O	Timer0 overflow divided by 64 output
T1O	O	Timer1 overflow divided by 2 output
T2O	O	Timer2 overflow divided by 2 output
T2EX	I	Timer2 external trigger input
VBGO	O	Bandgap voltage output
PWM0P PWM0N PWM1	O	16 bits PWM output
AD0~AD11	I	ADC input
OPP	I	OPA positive input
OPN	I	OPA negative input
OPO	O	OPA output
C1P	I	Comparator 1 positive input
C1N	I	Comparator 1 negative input
C2N	I	Comparator 2 negative input
C3N	I	Comparator 3 negative input
C4N	I	Comparator 4 negative input
C5N	I	Comparator 5 negative input
SCL	O	Master IIC clock output
SDA	I/O	Master IIC data input or output
PPG	O	PPG output
RSTn	I	External active low reset input, Pull-up resistor is fixed enable
VCC, VSS	P	Power input pin and ground

PIN SUMMARY

TM52F8658

Pin Number		Pin Name	Type	Input			Output			Alternate Function								Misc
SOP-20	SOP-16			Pull-up Control	Wake up	Ext. Interrupt	P.P.	P.O.D.	O.D.	OPA	ADC	COMP	IIC	UART	PWM	Timer		
1	1	C3N/P1.7	I/O	⭘	●		●		●			●						
2	2	AD11/P3.6	I/O	⭘			●		●		●							
3		PPG	O						●									
4	3	PWM0P/T1/T1O/AD10/P3.5	I/O	⭘			●		●		●				●	●		
5	4	SCL/TXD/AD9/P3.1	I/O	⭘			●	●			●		●	●				
6		RSTn/INT2/AD8/P3.7	I/O	⭘	●	●	●		●		●							Reset
7	5	VSS	P															
8	6	SDA/RXD/AD7/P3.0	I/O	⭘			●	●			●		●	●				
9	7	PWM0N/AD6/P1.2	I/O	⭘	●		●		●		●				●			
10	8	PWM1/INT1/AD5/P3.3	I/O	⭘	●	●	●		●		●				●			
11	9	AD4/P2.2	I/O	⭘			●		●		●							
12		T0/T0O/AD3/P3.4	I/O	⭘			●		●		●					●		
13	10	VCC	P						●									
14	11	VBGO/INT0/AD2/C5N/P3.2	I/O	⭘	●	●	●	●			●	●						VBGO
15	12	AD1/OPO/C4N/P1.6	I/O	⭘	●		●		●	●	●	●						
16	13	T2/T2O/AD0/OPP/P1.0	I/O	⭘	●		●		●	●	●					●		
17		T2EX/OPN/P1.1	I/O	⭘	●		●		●	●								
18	14	C2N/P1.5	I/O	⭘	●		●		●			●						
19	15	C1P/P1.4	I/O	⭘	●		●		●			●						
20	16	C1N/P1.3	I/O	⭘	●		●		●			●						

Symbol:

P.P. = Push-Pull Output
O.D. = Open Drain
P.O.D. = Pseudo Open Drain

PS:

1. ⭘ Port1, Port3, P2.2 these pins control Pull up resistor by operation modes

FUNCTIONAL DESCRIPTION

1. CPU Core

In the 8051 architecture, the C programming language is used as a development platform. The TM52 device features a fast 8051 core in a highly integrated microcontroller, allowing designers to be able to achieve improved performance compared to a classic 8051 device. TM52 series microcontrollers provide a complete binary code with standard 8051 instruction set compatibility, ensuring an easy migration path to accelerate the development speed of system products. The CPU core includes an ALU, a program status word (PSW), an accumulator (ACC), a B register, a stack point (SP), DPTRs, a program counter, an instruction decoder, and core special function registers (SFRs).

1.1 Accumulator (ACC)

This register provides one of the operands for most ALU operations. Accumulators are generally referred to as A or Acc and sometimes referred to as Register A. In this document, the accumulator is represented as “A” or “ACC” including the instruction table. The accumulator, as its name suggests, is used as a general register to accumulate the intermediate results of a large number of instructions. The accumulator is the most important and frequently used register to complete arithmetic and logical operations. It holds the intermediate results of most arithmetic and logic operations and assists in data transportation.

SFR **E0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E0h.7~0 **ACC:** Accumulator

1.2 B Register (B)

The “B” register is very similar to the ACC and may hold a 1 Byte value. This register provides the second operand for multiply or divide instructions. Otherwise, it may be used as a scratch pad register. The B register is only used by two 8051 instructions, MUL and DIV. When A is to be multiplied or divided by another number, the other number is stored in B. For MUL and DIV instructions, it is necessary that the two operands are in A and B.

ex: DIV AB

When this instruction is executed, data inside A and B are divided, and the answer is stored in A.

SFR **F0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0h.7~0 **B:** B register

1.3 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the Stack Pointer. The Stack Pointer points to the top location of the stack.

SFR **81h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP	SP							
R/W	R/W							
Reset	0	0	0	0	0	1	1	1

81h.7~0 **SP:** Stack Point

1.4 Dual Data Pointer (DPTRs)

TM52 device has two DPTRs, which share the same SFR address. Each DPTR is 16 bits in size and consists of two registers: the DPTR high byte (DPH) and the DPTR low byte (DPL). The DPTR is used for 16-bit-address external memory accesses, for offset code byte fetches, and for offset program jumps. Setting the DPSEL control bit allows the program code to switch between the two physical DPTRs.

SFR **82h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

82h.7~0 **DPL:** Data Point low byte

SFR **83h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	DPH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

83h.7~0 **DPH:** Data Point high byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W
Reset	0	0	–	0	0	0	–	0

F8h.0 **DPSEL:** Active DPTR Select

1.5 Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operations. The instructions that affect the PSW are listed below.

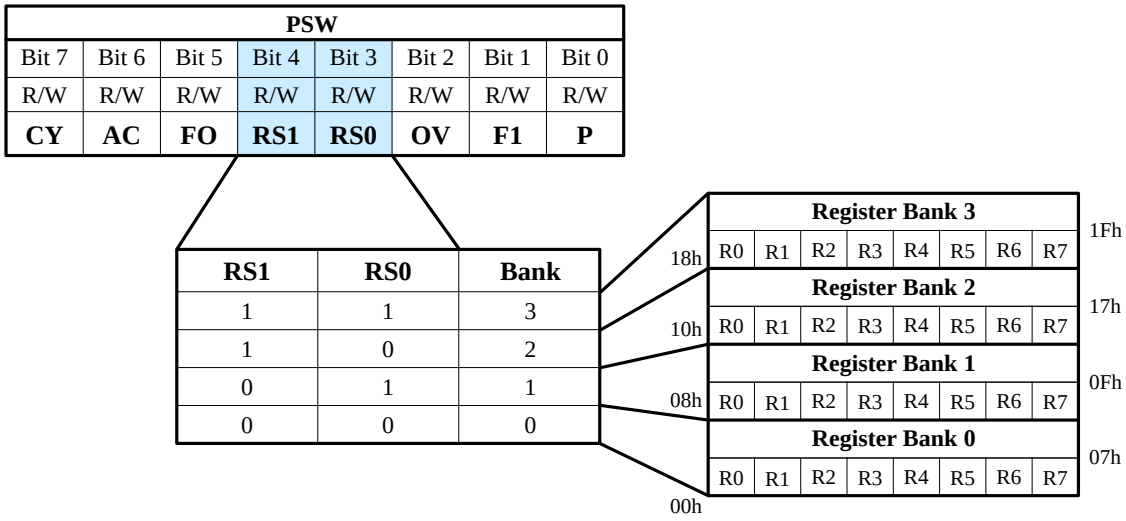
Instruction	Flag		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		

Instruction	Flag		
	C	OV	AC
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
ORL C, /bit	X		
MOV C, bit	X		
CJNE	X		

A “0” means the flag is always cleared, a “1” means the flag is always set and an “X” means that the state of the flag depends on the result of the operation.

SFR **D0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D0h.7 **CY:** ALU carry flag
D0h.6 **AC:** ALU auxiliary carry flag
D0h.5 **F0:** General purpose user-definable flag
D0h.4~3 **RS1, RS0:** The contents of (RS1, RS0) enable the working register banks as:
00: Bank 0 (00h~07h)
01: Bank 1 (08h~0Fh)
10: Bank 2 (10h~17h)
11: Bank 3 (18h~1Fh)
D0h.2 **OV:** ALU overflow flag
D0h.1 **F1:** General purpose user-definable flag
D0h.0 **P:** Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of “one” bits in the accumulator.



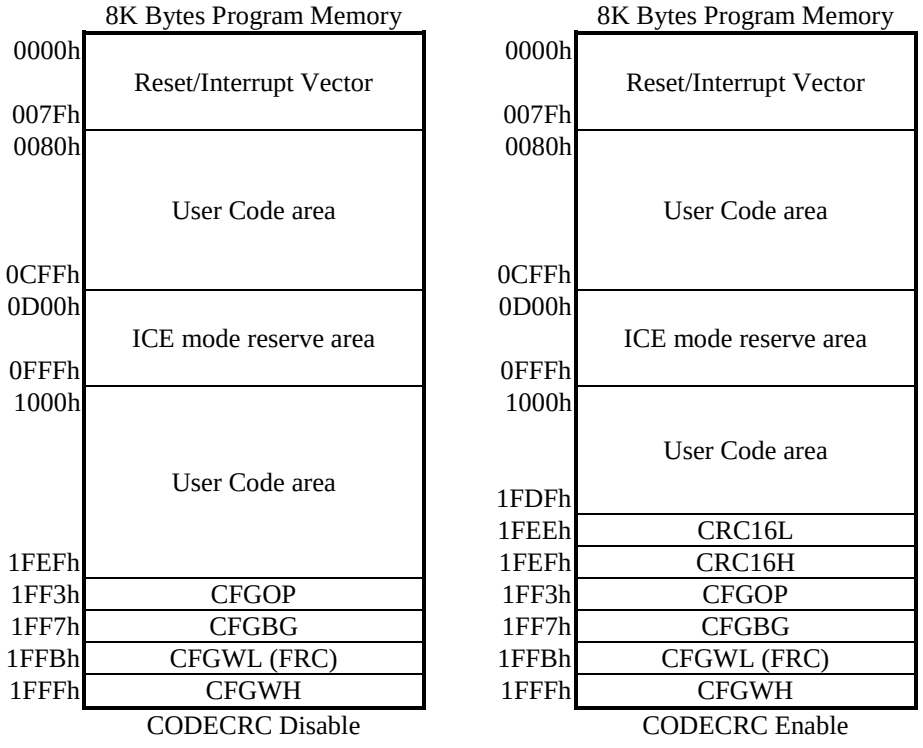
2. Memory

2.1 Program Memory

The Chip has an 8K Bytes Flash program memory, which can support In Circuit Programming (ICP) function mode. The Flash write endurance is at least 10K cycles. The Flash program memory address continuous space (0000h~1FFFh) is partitioned to several sectors for device operation.

2.1.1 Program Memory Functional Partition

The last 16 bytes (1FF0h~1FFFh) of program memory is defined as chip Configuration Word (CFGW), which is loaded into the device control registers upon power on reset (POR). The address space 0000h~007Fh is occupied by Reset/Interrupt vectors as standard 8051 definition. In the in-circuit emulation (ICE) mode, user also needs to reserve the address space 0D00h~0FFFh for ICE System communication. CRC16H/L is the reserved area of the checksum. Tenx can provide a CRC verification subroutine. The user can calculate the checksum by the CRC verification subroutine to compare with CRC16H/L and check the validity of the ROM code. The ROM code CRC16 verification can disable or enable by CODECRC (CFGWH.2) bit. While CODECRC enable, the address space 1FE0h~1FEFh will be reserved for CRC16H/L.



Flash **1FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE		–	CODECRC	MVCLOCK	FRCPSC

1FFFh.2 **CODECRC:** User Code CRC16 Verification
0: Disable (Valid User Code Range is 0000h~1FEFh)
1: Enable (Valid User Code Range is 0000h~1FDFh)

2.1.2 Flash ICP Mode

The Flash memory can be programmed by the tenx proprietary writer **(TWR98/TWR99)**, which needs at least four wires (VCC, VSS, P3.0, and P3.1 pins) to connect to this chip. If the user wants to program the Flash memory on the target circuit board (In Circuit Programming, ICP), these pins must be reserved sufficient freedom to be connected to the Writer.

Writer wire number	Pin connection
4-Wire	VCC, VSS, P3.0, P3.1

2.2 EEPROM Memory

The **F8658** contains 128 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 50K write/erase cycles.

EEPROM Memory

EE00h	EEPROM[0]
EE04h	EEPROM[1]
EE08h	. . .
EFF8h	EEPROM[126]
EFFCh	EEPROM[127]

The EEPROM Write usage is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target EEPROM address (EE00h~EFFCh, ADDR=ADDR+4), and the ACC contains the data being written. EEPROM writing requires approximately 2ms@V_{CC}=3V, 1ms@V_{CC}=5V. Meanwhile, the CPU stays in a waiting state, but all peripheral modules (Timers, PWM, and others) continue running during the writing time. The software must handle the pending interrupts after an EEPROM write. The **F8658** has a build-in EEPROM Time-out function for escaping write fail state. EEPROM writing needs V_{CC}>3.0V.

The EEPROM Read can be performed by the "MOVX A, @DPTR" instruction as long as the target address points the EE00h~EFFCh area. The EEPROM read does require approximately 300ns.

```
; EEPROM example code
; need VCC>3.0V
MOV     DPTR, #EE00h        ; DPTR=EE00h=target EEPROM[0] address
MOV     A, #5Ah             ; A=5Ah=target EEPROM[0] write data
MOV     EEPWE, #E2h         ; EEPROM write enable
MOV     AUX2, #02h          ; EEPROM Time-Out function enable
MOVX    @DPTR, A            ; EEPROM[0] =5Ah, after EEPROM write
                            ; 1ms~2ms H/W writing time, CPU wait
MOV     EEPWE, #00h         ; EEPROM write disable, immediately after EEPROM write
CLR     A                   ; A=0
MOVX    A, @DPTR            ; A=5Ah
```

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPWE	EEPWE							
	–	EEPTO	EEPWE	–				
R/W	W	R/W	R/W	W				
Reset	–	0	0	–				

C9h.7~0 **EEPWE (W):** Write E2h to set EEPWE control flag; Write other value to clear EEPWE flag. It is recommended to clear it immediately after EEPROM write.

C9h.6 **EEPTO (R):** EEPROM write Time-Out flag, set by H/W when EEPROM write Time-out occurs. Cleared by H/W when EEPWE=0.

C9h.5 **EEPWE (R):** Flag indicates EEPROM memory can be written or not, 1=EEPROM write enable.

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	EEPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	0

F7h.2~1 **EEPTE:** EEPROM write watchdog timer enable

00: Disable

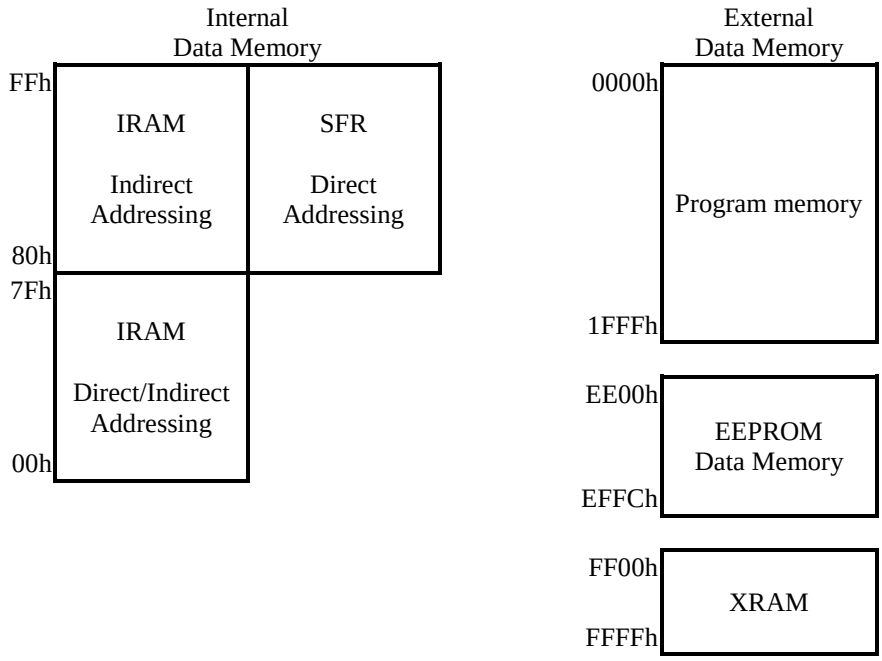
01: wait 0.8mS trigger watchdog time-out flag, and escape the write fail state

10: wait 3.1mS trigger watchdog time-out flag, and escape the write fail state

11: wait 6.2mS trigger watchdog time-out flag, and escape the write fail state

2.3 Data Memory

As the standard 8051, the Chip has both Internal and External Data Memory space. The Internal Data Memory space consists of 256 Bytes IRAM and 97 SFRs, which are accessible through a rich instruction set. The External Data Memory space consists of 256 Bytes XRAM and 128 Bytes EEPROM, which can be only accessed by MOVX instruction.



2.3.1 IRAM

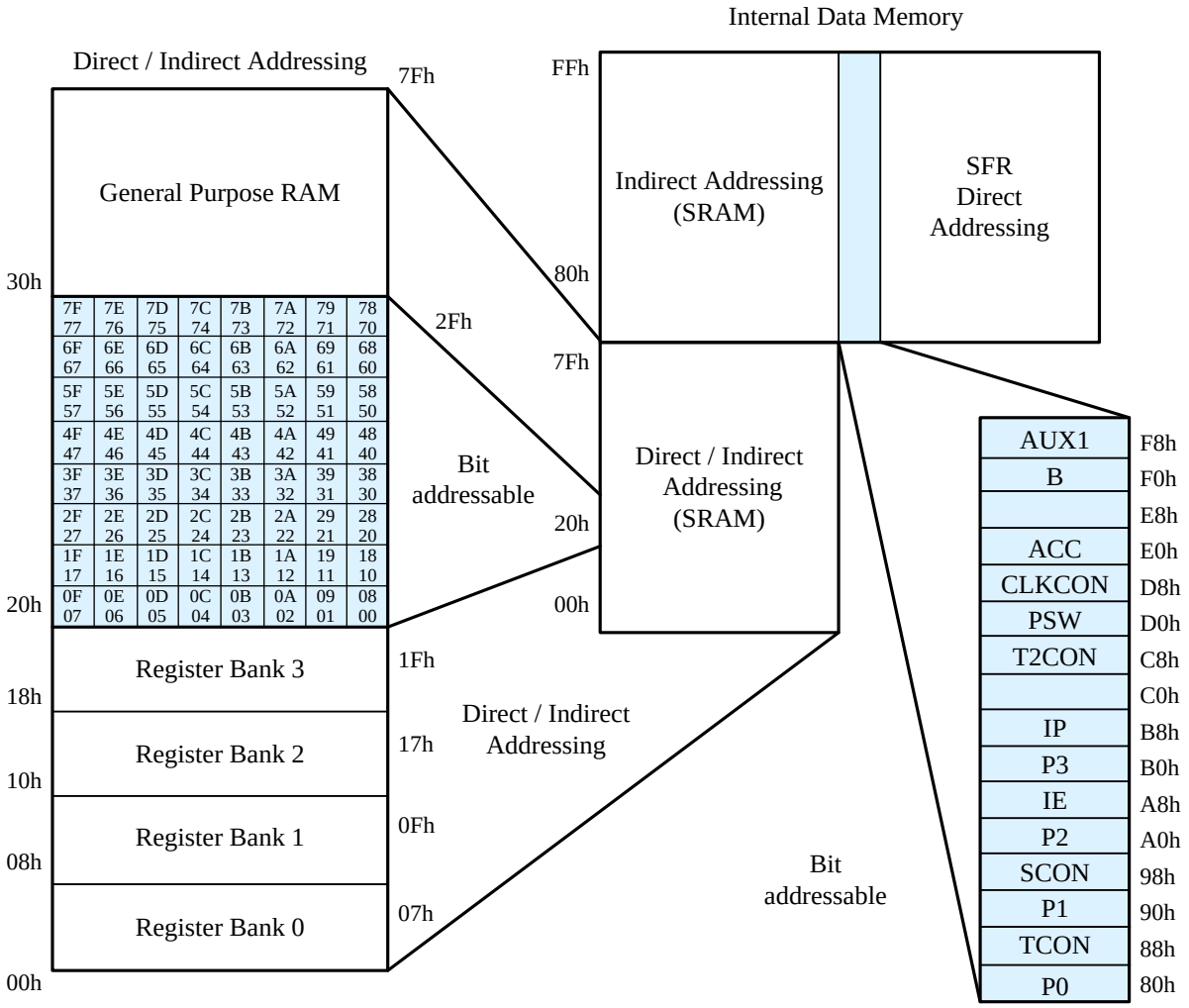
IRAM is located in the 8051 internal data memory space. The whole 256 Bytes IRAM are accessible using indirect addressing but only the lower 128 Bytes are accessible using direct addressing. There are four directly addressable register banks (switching by PSW), which occupy IRAM space from 00h to 1Fh. The address 20h to 2Fh 16 Bytes IRAM space is bit-addressable. IRAM can be used as scratch pad registers or program stack.

2.3.2 XRAM

XRAM is located in the 8051 external data memory space (address from FF00h to FFFFh). The 256 Bytes XRAM can be only accessed by “MOVX” instruction.

2.3.3 SFRs

All peripheral functional modules such as I/O ports, Timers and UART operations for the chip are accessed via Special Function Registers (SFRs). These registers occupy upper 128 Bytes of direct Data Memory space locations in the range 80h to FFh. There are 14 bit-addressable SFRs (which means that eight individual bits inside a single byte are addressable), such as ACC, B register, PSW, TCON, SCON, and others. The remaining SFRs are only byte addressable. SFRs provide control and data exchange with the resources and peripherals of the Chip. The TM52 series of microcontrollers provides complete binary code with standard 8051 instruction set compatibility. Beside the standard 8051 SFRs, the Chip implements additional SFRs used to configure and access subsystems such as the ADC/PPG, which are unique to the Chip.



	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
F8h	AUX1							
F0h	B	CRCDL	CRCDH	CRCIN		CFGBG	CFGWL	AUX2
E8h		CMP1CAL	CMP2CAL	CMP3CAL	CMP4CAL	CMP5CAL	OPCON	OPCAL
E0h	ACC	MICON	MIDAT	SYNCNT	SYNDLY	LVRPD	EXA	EXB
D8h	CLKCON	PWM0PRDH	PWM0PRDL	PWM1PRDH	PWM1PRDL			
D0h	PSW	PWM0DH	PWM0DL	PWM1DH	PWM1DL			CMPIEDG
C8h	T2CON	EEPWE	RCP2L	RCP2H	TL2	TH2	EXA2	EXA3
C0h		CMP1CON	CMP2CON	CMP3CON	CMP4CON	CMP5CON	CMP23EQ	CMP45EQ
B8h	IP	IPH	IP1	IP1H				CMPEQI
B0h	P3	PPGCON0	PPGCON1	PPGRLDL			PPGTML	PPGTMH
A8h	IE	INTE1	ADCDL	ADCDH			CHSEL	
A0h	P2	PWMCON	P1MODL	P1MODH	P3MODL	P3MODH	PINMOD	PWMCON2
98h	SCON	SBUF	PPDCON	PPDSTA	PPDTH	PPDIE		
90h	P1				OPTION	INTFLG	P1WKUP	SWCMD
88h	TCON	TMOD	TL0	TL1	TH0	TH1		
80h	P0	SP	DPL	DPH	INTE2	INTFLG2		PCON

3. Power

The Chip provides Low Voltage Reset (LVR) function. There are 4-level LVR can be selected by CFGWH. It can be disabled at Fast by LVRPD (E5h) SFR. In addition, set PWRSAV will affect the LVR setting at Idle and Stop Mode.

SFR **E5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVRPD	LVRPD							
R/W	W							
Reset	0	0	0	0	0	0	0	0

E5h **LVRPD:** LVR and POR power down option
Write 0x37 to force LVR disable, POR disable
Write 0x38 to force LVR disable, POR enable

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	EEPTE		MULDIV16
R/W	R/W		R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.5 **PWRSAV:** Set 1 to reduce the chip's power consumption at Idle and Stop Mode

Flash **1FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE		–	CODECRC	MVCLOCK	FRCPSC

1FFFh.5~4 **LVRE:** Low Voltage Reset function select
00: Set LVR at 4.3V
01: Set LVR at 3.8V
10: Set LVR at 3.2V
11: Set LVR at 2.7V

4. Reset

The Chip has five types of reset methods. Resets can be caused by Power on Reset (POR), External Pin Reset (XRST), Software Command Reset (SWRST), Watchdog Timer Reset (WDTR), or Low Voltage Reset (LVR). The CFGW controls the Reset functionality. The SFRs are returned to their default value after Reset.

4.1 Power on Reset

After Power on Reset, the device stays on Reset state for 25 ms as chip warm up time, then downloads the CFGW register from Flash‘s last 16 bytes. The Power on Reset needs VCC pin’s voltage first discharge to near VSS level, then rise beyond 2.7V.

4.2 External Pin Reset

External Pin Reset is active low. It needs to keep at least 2 SRC clock cycle long to be seen by the chip. External Pin Reset can be disabled or enabled by CFGWH.

4.3 Software Command Reset

Software Reset is activated by writing the SFR 97h with data 56h.

4.4 Watchdog Timer Reset

WDT overflow Reset is disabled or enabled by SFR F7h. The WDT uses SRC as its counting time base. It runs in Fast/Slow mode and runs or stops in Idle/Stop mode. WDT overflow speed can be defined by WDTPSC SFR. WDT is cleared by device Reset or CLRWDT SFR bit.

4.5 Low Voltage Reset

The Chip offers four options for LVR function. The user can make a selection by CFGWH, let LVR voltages of 4.3V, 3.8V, 3.2V, and 2.7V be selected separately. It can be disabled at Fast by LVRPD (E5h) SFR.

System Clock frequency	16 MHz	8 MHz	4 MHz	2 MHz
Minimum LVR level	LVR=4.3V	LVR=2.7V	LVR=2.7V	LVR=2.7V

LVR setting table

Note: LVR must be enable, also refer to AP-TM52XXXXX_02S for LVR setting information.

Flash **1FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE		–	CODECRC	MVCLOCK	FRCPSC

1FFFh.6 **XRSTE:** External Pin Reset control
0: Disable External Pin Reset
1: Enable External Pin Reset

1FFFh.5~4 **LVRE:** Low Voltage Reset function select
00: Set LVR at 4.3V
01: Set LVR at 3.8V
10: Set LVR at 3.2V
11: Set LVR at 2.7V

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	TM3CKS	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.5~4 **WDTPSC:** Watchdog Timer pre-scalar time select
00: 400ms WDT overflow rate
01: 200ms WDT overflow rate
10: 100ms WDT overflow rate
11: 50ms WDT overflow rate

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	SWRST							
	–						WDTO	–
R/W	W						R/W	W
Reset	–						0	–

97h.7~0 **SWRST:** Write 56h to generate S/W Reset

SFR **E5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVRPD	LVRPD							
R/W	W							
Reset	0	0	0	0	0	0	0	0

E5h **LVRPD:** LVR and POR power down option
Write 0x37 to force LVR disable, POR disable
Write 0x38 to force LVR disable, POR enable

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	EEPTE		MULDIV16
R/W	R/W		R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.7~6 **WDTE:** Watchdog Timer Reset control
0x: Watchdog Timer Reset disable
10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Stop mode
11: Watchdog Timer Reset always enable

F7h.5 **PWRSAV:** Set 1 to reduce the chip's power consumption at Idle and Stop Mode

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W
Reset	0	0	–	0	0	0	–	0

F8h.7 **CLRWDT:** Set to clear WDT, H/W auto clear it at next clock cycle

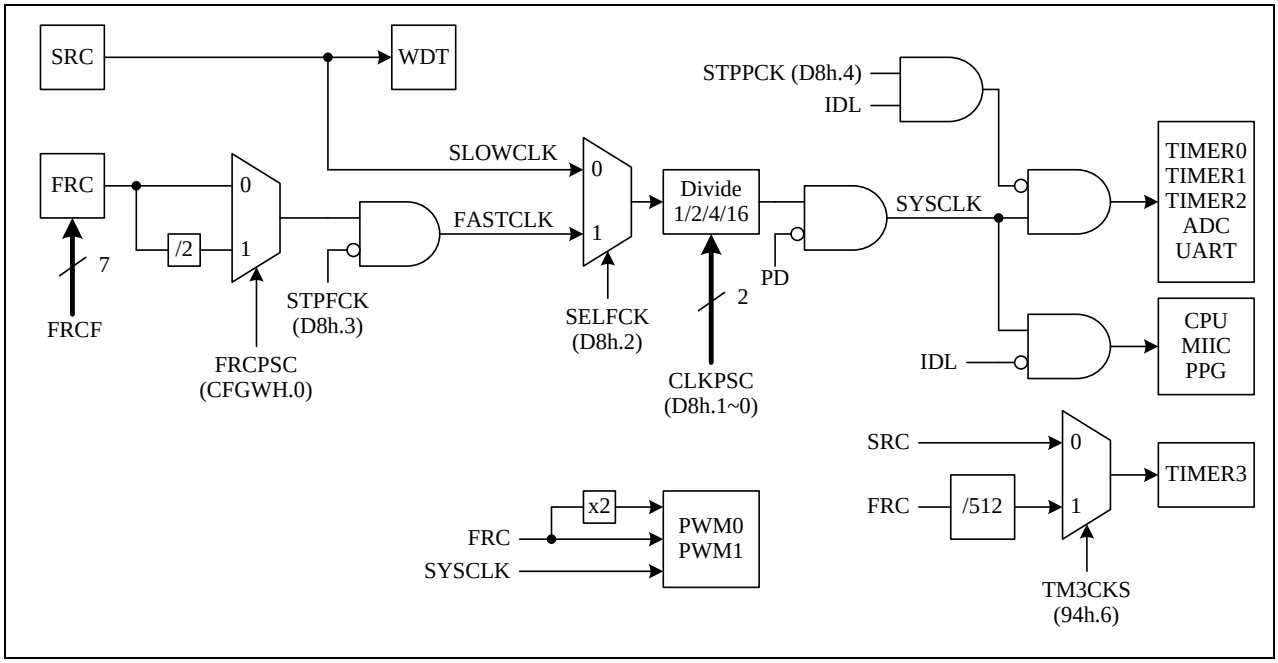
5. Clock Circuitry and Operation Mode

5.1 System Clock

The Chip is designed with dual-clock system. During runtime, user can directly switch the System clock from fast to slow or from slow to fast. It also can directly select a clock divider of 1, 2, 4 or 16. The Fast clock is FRC (Fast Internal RC, 16.5888 MHz or 8.2944MHz). The Slow clock is SRC (Slow Internal RC, 80 KHz). Fast mode and Slow mode are defined as the CPU running at Fast and Slow clock speeds.

After Reset, the device is running at Slow mode with 80KHz SRC. S/W should select the proper clock rate for chip operation safety. The higher V_{CC} allows the chip to run at a higher System clock frequency. In a typical condition, an 8 MHz System clock rate requires V_{CC}>2.0V.

The **CLKCON** SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow clock type in Fast mode and change the Fast clock type in Slow mode. Never to write both STPFCK=1 & SELFCK=1. It is recommended to write this SFR bit by bit.



Flash **1FFBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	–	FRCF						

1FFBh.6~0 **FRCF:** FRC frequency adjustment
FRC is trimmed to 16.5888 MHz in chip manufacturing. FRCF records the adjustment data.

SFR **F6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	–	FRCF						
R/W	–	R/W						
Reset	–	–	–	–	–	–	–	–

F6h.6~0 **FRCF:** FRC frequency adjustment
00=lowest frequency, 7Fh=highest frequency
The frequency range is about 13MHz (FRCF=00h) to 22MHz (FRCF=7Fh) with approaching linearity. Due to the chip process issue, the frequency range is different between each chip.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	–	–	–	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	–	–	–	R/W	R/W	R/W	R/W	
Reset	–	–	–	0	0	0	1	1

D8h.4 **STPPCK:** Set 1 to stop UART/Timer0/Timer1/Timer2/ADC clock in Idle mode for current reducing. If set, only Timer3 and pin interrupts are alive in Idle Mode.

D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.

D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock

D8h.1~0 **CLKPSC:** System clock prescaler. Effective after 16 clock cycles (Max.) delay.
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

SYSCLK	CLKCON (D8h)	
	Bit3 STPFCK	Bit2 SELFCK
Fast FRC	0	1
Slow SRC	0/1	0
Stop FRC	0 → 1	0
Switch to FRC	0	0 → 1
Switch to SRC	0	1 → 0

Note: Because of the CLKPSC delay, it needs to wait for 16 clock cycles (max.) before switching Slow clock to Fast clock. Also refer to AP-TM52XXXXX_01S and AP-TM52XXXXX_02S about System Clock Application Note.

5.2 Operation Mode

There are four operation modes for this device. **Fast Mode** is defined as the CPU running at Fast clock speed. **Slow Mode** is defined as the CPU running at Slow clock speed. When the System clock speed is lower, the power consumption is lower.

Idle Mode is entered by setting the IDL bit in PCON SFR. Both Fast and Slow clock can be set as the System clock source in Idle Mode, but Slow clock is better for power saving. In Idle mode, the CPU puts itself to sleep while the on-chip peripherals stay active. The "STPPCK" bit in CLKCON SFR can be set to furthermore reduce Idle mode current. If STPPCK is set, only Timer3 and pin interrupts are alive in Idle Mode, others peripherals such as Timer0/1/2, UART and ADC are stop. The slower System clock rate also helps current saving. It can be achieved by setup the CLKPSC SFR to divide System clock frequency. Idle mode is terminated by Reset or enabled Interrupts wake up.

Stop Mode is entered by setting the PD bit in PCON SFR. This mode is the so-called "Power Down" mode in standard 8051. In Stop mode, all clocks stop except the WDT is alive if it is enabled. Stop mode is terminated by Reset or pin wake up.

Note: Chip cannot enter Stop Mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0,1,2)
Note: FW must turn off Bandgap to obtain Tiny Current (PWRSAV=1, Disable OPA and CMP)

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter Stop mode.
87h.0 **IDL:** Idle mode control bit, set 1 to enter Idle mode.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	–	–	–	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	–	–	–	R/W	R/W	R/W	R/W	
Reset	–	–	–	0	0	0	1	1

D8h.4 **STPPCK:** Set 1 to stop UART/Timer0/Timer1/Timer2/ADC clock in Idle mode for current reducing. If set, only Timer3 and pin interrupts are alive in Idle Mode.
D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.
D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock
D8h.1~0 **CLKPSC:** System clock prescaler. Effective after 16 clock cycles (Max.) delay.
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

6. Interrupt and Wake-up

This Chip has a 20-source four-level priority interrupt structure. All enabled Interrupts can wake up CPU from Idle mode, but only the Pin Interrupts can wake up CPU from Stop mode. Each interrupt source has its own enable control bit. An interrupt event will set its individual Interrupt Flag, no matter whether its interrupt enable control bit is 0 or 1. The Interrupt vectors and flags are list below.

Vector	Flag	Description
0003	IE0	INT0 external pin Interrupt (can wake up Stop mode)
000B	TF0	Timer0 Interrupt
0013	IE1	INT1 external pin Interrupt (can wake up Stop mode)
001B	TF1	Timer1 Interrupt
0023	RI+TI	Serial Port (UART) Interrupt
002B	TF2+EXF2	Timer2 Interrupt
0033	–	Reserved for ICE mode use
003B	TF3	Timer3 Interrupt
0043	P1IF	Port1 external pin change Interrupt (can wake up Stop mode)
004B	IE2	INT2 external pin Interrupt (can wake up Stop mode)
0053	ADIF	ADC Interrupt
005B	MIICIF	MIIC Interrupt
0063	PPGIF+PPDIF	PPG/PPD Interrupt
006B	CMPIF	Comparator1~5 Interrupt
0073	PWMIF	PWM0~1 Interrupt

Interrupt Vector & Flag

6.1 Interrupt Enable and Priority Control

The IE and INTE1 SFRs decide whether the pending interrupt is serviced by CPU. The IP, IPH, IP1 and IP1H SFRs decide the interrupt priority. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

SFR **96h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1WKUP	P1WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

96h.7~0 **P1WKUP:** P1.7~P1.0 pin individual Wake up/Interrupt enable control
0: Disable
1: Enable

SFR **A8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A8h.7 **EA:** Global interrupt enable
0: Disable all interrupts
1: Each interrupt is enabled or disabled by its individual interrupt control bit

A8h.5 **ET2:** Timer2 interrupt enable
0: Disable Timer2 interrupt
1: Enable Timer2 interrupt

A8h.4 **ES:** Serial Port (UART) interrupt enable
0: Disable Serial Port (UART) interrupt
1: Enable Serial Port (UART) interrupt

A8h.3 **ET1:** Timer1 interrupt enable
0: Disable Timer1 interrupt
1: Enable Timer1 interrupt

A8h.2 **EX1:** INT1 pin Interrupt enable and Stop mode wake up enable
0: Disable INT1 pin Interrupt and Stop mode wake up
1: Enable INT1 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

A8h.1 **ET0:** Timer0 interrupt enable
0: Disable Timer0 interrupt
1: Enable Timer0 interrupt

A8h.0 **EX0:** INT0 pin Interrupt enable and Stop mode wake up enable
0: Disable INT0 pin Interrupt and Stop mode wake up
1: Enable INT0 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	CMPIE	PPGDIE	I2CIE	ADIE	EX2	P1IE	TM3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.7 **PWMIE:** PWM0/1 interrupt enable
0: Disable PWM0/1 interrupt
1: Enable PWM0/1 interrupt

A9h.6 **CMPIE:** CMP1~5 interrupt enable
0: Disable CMP1~5 interrupt
1: Enable CMP1~5 interrupt

A9h.5 **PPGDIE:** PPG/PPD interrupt enable
0: Disable PPG/PPD interrupt
1: Enable PPG/PPD interrupt

A9h.4 **I2CIE:** Master I^2C interrupt enable
0: Disable Master I^2C interrupt
1: Enable Master I^2C interrupt

A9h.3 **ADIE:** ADC interrupt enable
0: Disable ADC interrupt
1: Enable ADC interrupt

A9h.2 **EX2:** INT2 pin Interrupt enable and Stop mode wake up enable
0: Disable INT2 pin Interrupt and Stop mode wake up
1: Enable INT2 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

A9h.1 **P1IE:** Port1 pin change interrupt enable
0: Disable Port1 pin change interrupt
1: Enable Port1 pin change interrupt

A9h.0 **TM3IE:** Timer3 interrupt enable
0: Disable Timer3 interrupt
1: Enable Timer3 interrupt

SFR **B9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPH	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

SFR **B8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

B9h.5, B8h.5 **PT2H, PT2:** Timer2 interrupt priority control. (PT2H, PT2) =
00: Level 0 (lowest priority)
01: Level 1
10: Level 2
11: Level 3 (highest priority)

B9h.4, B8h.4 **PSH, PS:** Serial Port (UART) interrupt priority control. Definition as above.
B9h.3, B8h.3 **PT1H, PT1:** Timer1 interrupt priority control. Definition as above.
B9h.2, B8h.2 **PX1H, PX1:** INT1 pin interrupt priority control. Definition as above.
B9h.1, B8h.1 **PT0H, PT0:** Timer0 interrupt priority control. Definition as above.
B9h.0, B8h.0 **PX0H, PX0:** INT0 pin interrupt priority control. Definition as above.

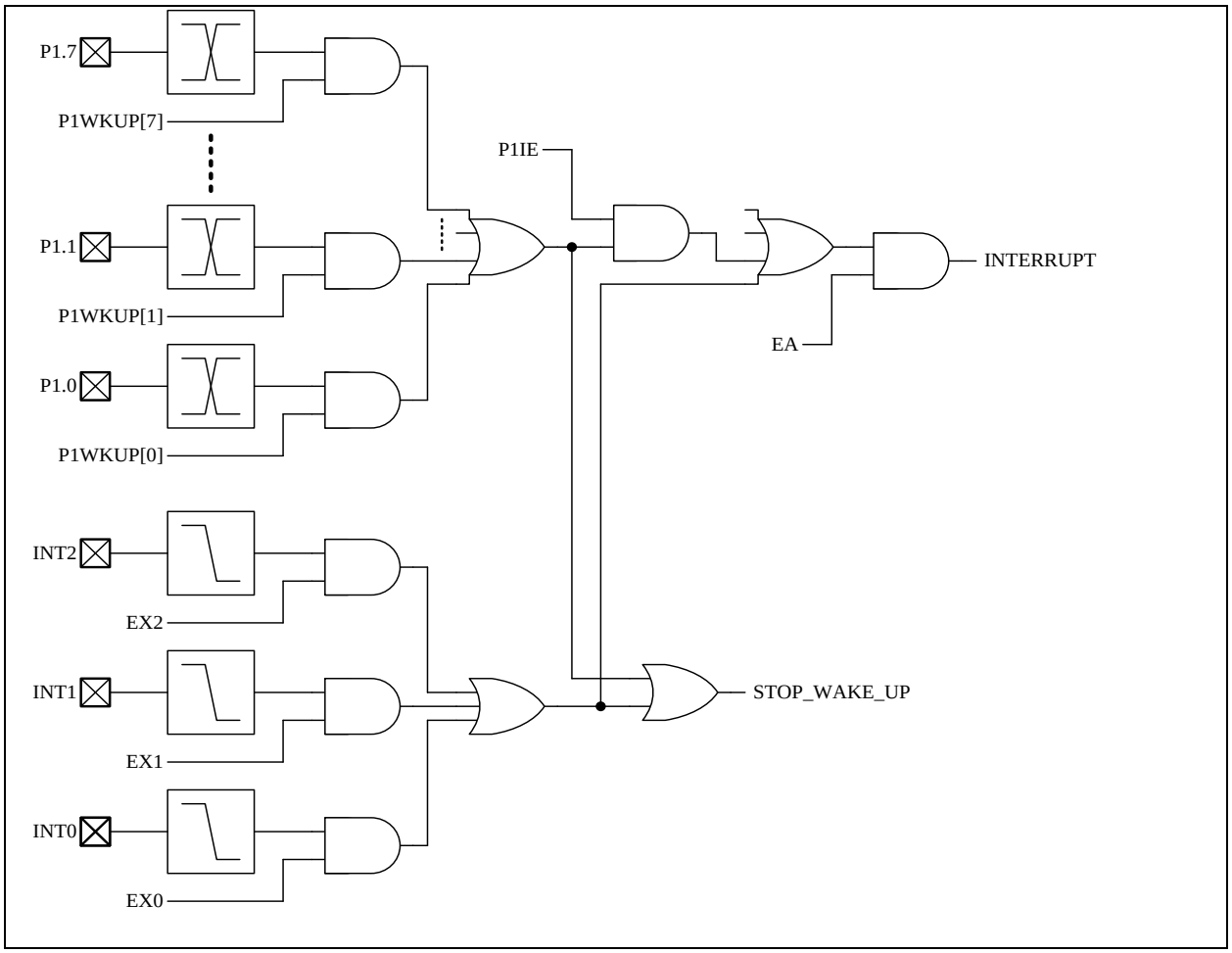
SFR **BBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1H	PPWMH	PCMPH	PPPGDH	PI2CH	PADH	PX2H	PP1H	PT3H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR **BAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1	PPWM	PCMP	PPPGD	PI2C	PAD	PX2	PP1	PT3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

BBh.7, BAh.7 **PPWMH, PPWM:** PWM0~1 interrupt priority control. Definition as above.
BBh.6, BAh.6 **PCMPH, PCMP:** CMP1~5 interrupt priority control. Definition as above.
BBh.5, BAh.5 **PPPGDH, PPPGD:** PPG/PPD interrupt priority control. Definition as above.
BBh.4, BAh.4 **PI2CH, PI2IC:** Master I^2C interrupt priority control. Definition as above.
BBh.3, BAh.3 **PADH, PAD:** ADC interrupt priority control. Definition as above.
BBh.2, BAh.2 **PX2H, PX2:** INT2 pin interrupt priority control. Definition as above.
BBh.1, BAh.1 **PP1H, PP1:** Port1 pin change interrupt priority control. Definition as above.
BBh.0, BAh.0 **PT3H, PT3:** Timer3 interrupt priority control. Definition as above.

6.2 Pin Interrupt

Pin Interrupts include INT0 (P3.2), INT1 (P3.3), INT2 (P3.7) and Port1 Change Interrupt. These pins also have the Stop mode wake up capability. INT0 and INT1 are falling edge or low level triggered as the 8051 standard. INT2 is falling edge triggered and Port1 Change Interrupt is triggered by any Port1 pin state change.



Pin Interrupt & Wake up

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.3 **IE1:** External Interrupt 1 (INT1 pin) edge flag
Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.2 **IT1:** External Interrupt 1 control bit
0: Low level active (level triggered) for INT1 pin
1: Falling edge active (edge triggered) for INT1 pin

88h.1 **IE0:** External Interrupt 0 (INT0 pin) edge flag
Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.0 **IT0:** External Interrupt 0 control bit
0: Low level active (level triggered) for INT0 pin
1: Falling edge active (edge triggered) for INT0 pin

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	–	ADIF	–	IE2	P1IF	TF3
R/W	–	–	–	R/W	–	R/W	R/W	R/W
Reset	–	–	–	0	–	0	0	0

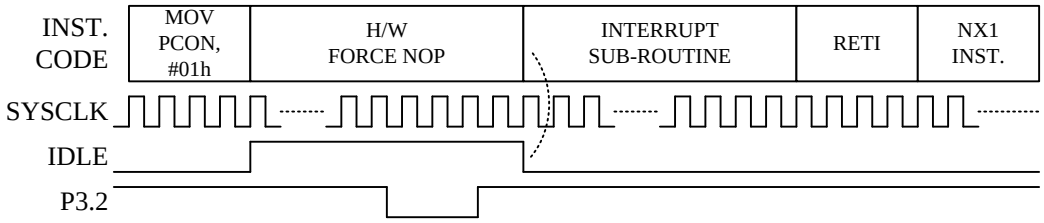
95h.2 **IE2:** External Interrupt 2 (INT2 pin) edge flag
Set by H/W when a falling edge is detected on the INT2 pin state, no matter the EX2 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.
S/W writes FBh to INTFLG to clear this bit.

95h.1 **P1IF:** Port1 pin change interrupt flag
Set by H/W when a P1 pin state change is detected, and its interrupt enable bit is set (P1WKUP).
P1IE does not affect this flag's setting.
It is cleared automatically when the program performs the interrupt service routine.
S/W writes FDh to INTFLG to clear this bit.

Note: Chip cannot enter Stop Mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0~2)

6.3 Idle Mode Wake up and Interrupt

Idle mode is waked up by enabled Interrupts, which means individual interrupt enable bit (ex: EX0) and EA bit must be both set to 1 to establish Idle mode wake up capability. All enabled Interrupts (Pins, Timers, ADC, CMP, MIIC, PWM and UART) can wake up CPU from Idle mode. Upon Idle wake-up, Interrupt service routine is entered immediately. "The first instruction behind IDL (PCON.0) setting" is executed after interrupt service routine return.



EA=EX0=1, Idle mode wake-up and Interrupt by P3.2 (INT0)

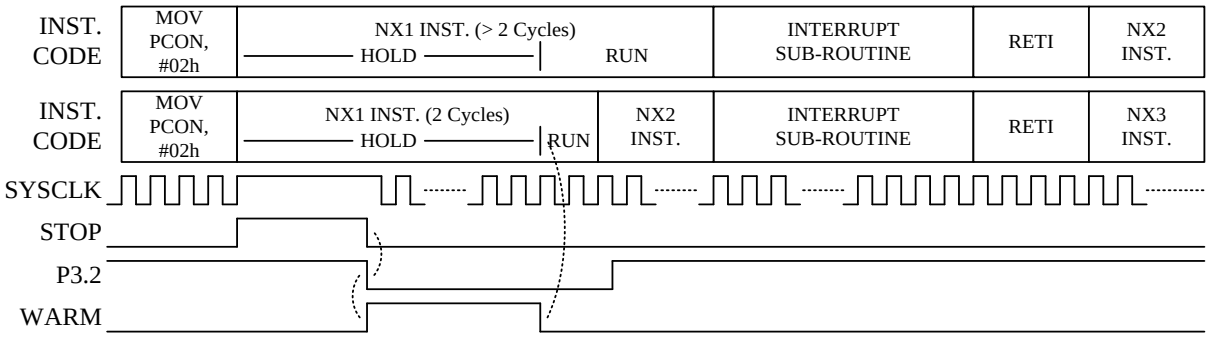
SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Stop bit. If 1, Stop mode is entered.
87h.0 **IDL:** Idle bit. If 1, Idle mode is entered.

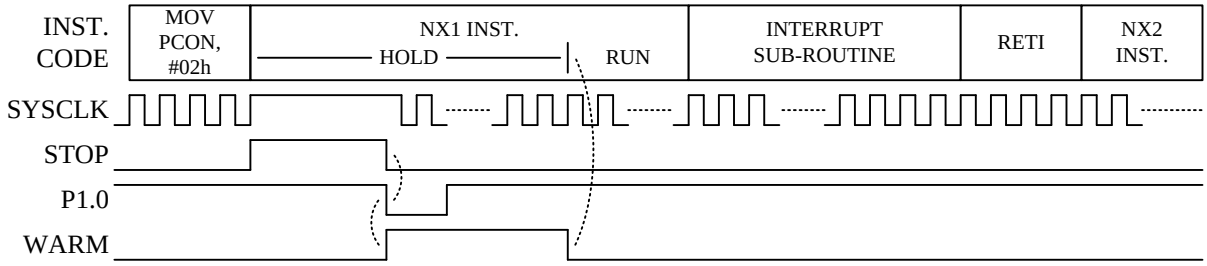
6.4 Stop Mode Wake up and Interrupt

Stop mode wake up is simple, as long as the individual pin interrupt enable bit (ex: EX0) is set, the pin wake up capability is asserted. Set EX0/EX1/EX2 can enable INT0/INT1/INT2 pins' Stop mode wake up capability. Set P1WKUP bit 7~0 can enable P1.7~P1.0's Stop mode wake up capability. Upon Stop wake up, "the first instruction behind PD (PCON.1) setting" is executed immediately before Interrupt service. Interrupt entry needs EA=1 (P1WKUP also needs P1IE=1) and the trigger state of the pin staying sufficiently long to be observed by the System clock. This feature allows CPU to enter or not enter Interrupt sub-routine after Stop mode wake up.

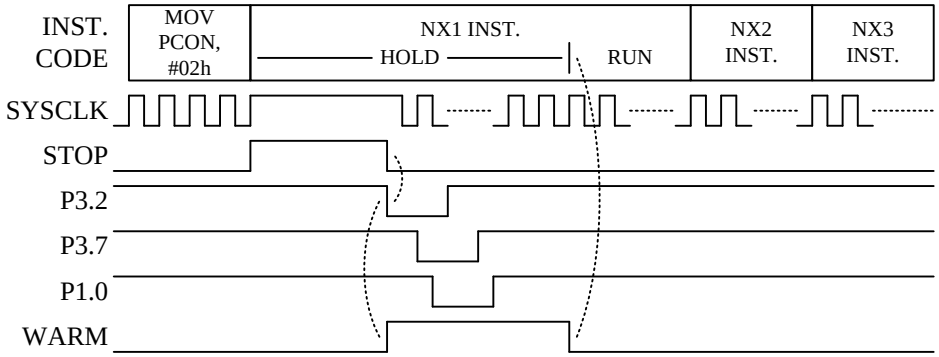
Note: It is recommended to place the NX1/NX2 with NOP Instruction in figures below.



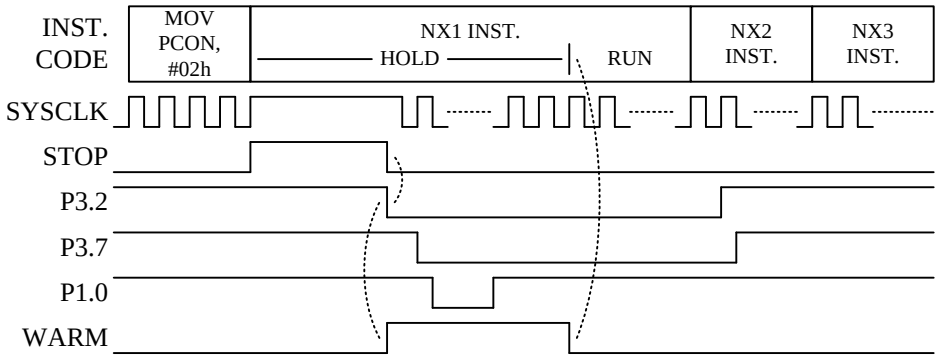
EA=EX0=1
P3.2 (INT0) is sampled after warm-up, Stop mode wake-up and Interrupt.



EA=P1IE=P1WKUP=1
P1.0 change (not need clock sample), Stop mode wake-up and Interrupt.



EA=EX0=EX2=P1WKUP=1, P1IE=0
Stop mode wake-up but not Interrupt, P3.2/P3.7 pulse too narrow.



EX0=EX2=P1WKUP=P1IE=1, EA=0
Stop mode wake-up but not Interrupt.

7. I/O Ports

The Chip has total 17 multi-function I/O pins. All I/O pins follow the standard 8051 "Read-Modify-Write" feature. The instructions that read the SFR rather than the Pin State are the ones that read a port or port bit value, possibly change it, and then rewrite it to the SFR. (ex: ANL P1, A; INC P2; CPL P3.0)

7.1 Port1 & P2.2 & Port3

These pins can operate in four different modes as below.

Mode	Port1, P2.2, Port3 pin function		Px.n SFR data	Pin State	Resistor Pull-up	Digital Input
	P3.2~P3.0	Others				
Mode 0	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Pull-up	Y	Y
Mode 1	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Hi-Z	N	Y
Mode 2	CMOS Output		0	Drive Low	N	N
			1	Drive High	N	N
Mode 3	Alternative Function, such as ADC		X (don't care)	–	N	N

Port1, P2.2, Port3 I/O Pin Function Table

If a Port1, P2.2 or Port3 pin is used for Schmitt-trigger input, S/W must set the I/O pin to Mode0 or Mode1 and set the corresponding Port Data SFR to 1 to disable the pin's output driving circuitry.

Beside I/O port function, each Port1, P2.2 and Port3 pin has one or more alternative functions, such as CMP, ADC and OPA. Most of the functions are activated by setting the individual pin mode control SFR to Mode3. Port1/Port3 pins have standard 8051 auxiliary definition such as INT0/1, T0/1/2, or RXD/TXD. These pin functions need to set the pin mode SFR to Mode0 or Mode1 and keep the P1.n/P3.n SFR at 1.

Pin Name	8051	Wake-up	CKO	ADC	CMP/OPA	others	Mode3
P1.0	T2	Y	T2O	AD0	OPP		AD0
P1.1	T2EX	Y			OPN		
P1.2		Y		AD6		PWM0N	AD6
P1.3		Y			C1N		
P1.4		Y			C1P		
P1.5		Y			C2N		
P1.6		Y		AD1	C4N/OPO		AD1
P1.7		Y			C3N		
P2.2				AD4			AD4
P3.0	RXD			AD7		SDA	AD7
P3.1	TXD			AD9		SCL	AD9
P3.2	INT0	Y		AD2	C5N		AD2
P3.3	INT1	Y		AD5		PWM1	AD5
P3.4	T0		T0O	AD3			AD3
P3.5	T1		T1O	AD10		PWM0P	AD10
P3.6				AD11			AD11
P3.7		Y		AD8		INT2	AD8

Port1, P2.2, Port3 multi-function Table

The necessary SFR setting for Port1/P2.2/Port3 pin's alternative function is list below.

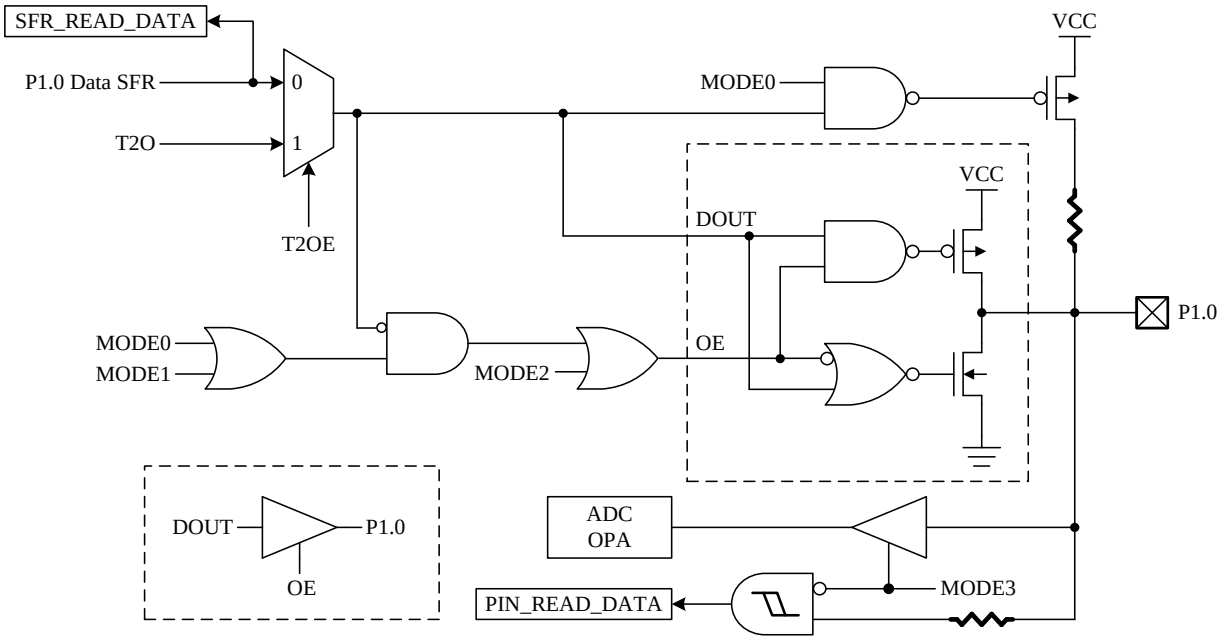
Alternative Function	Mode	Px.n SFR data	Pin State	Other necessary SFR setting
T0, T1, T2, T2EX, INT0, INT1, INT2	**0**	1	Input with Pull-up	
	1	1	Input	
RXD, TXD	**0**	1	Input with Pull-up/Pseudo Open Drain Output	
	1	1	Input/Pseudo Open Drain Output	
T0O, T1O, T2O	**0**	X	Clock Open Drain Output with Pull-up	PINMOD
	1	X	Clock Open Drain Output	
	2	X	Clock Output (CMOS Push-Pull)	
C1P, C1N	**X**	X	Comparator1 Voltage Input	CMP1CON
C2N	**X**	X	Comparator2 Voltage Input	CMP2CON
C3N	**X**	X	Comparator3 Voltage Input	CMP3CON
C4N	**X**	X	Comparator4 Voltage Input	CMP4CON
C5N	**X**	X	Comparator5 Voltage Input	CMP5CON
OPP, OPN	**X**	X	OP-Amp Input	OPCON OPCAL
OPO	**1**	1	OP-Amp Output	OPCON
PWM0P, PWM0N, PWM1	**0**	X	PWM Open Drain Output with Pull-up	PINMOD
	1	X	PWM Open Drain Output	
	2	X	PWM Output (CMOS Push-Pull)	
SDA	**0**	X	Input with Pull-up/Open Drain Output	MICON
	1	X	Input/Open Drain Output	
SCL	**0**	X	Master IIC Clock Open Drain Output with Pull-up	MICON
	1	X	Master IIC Clock Open Drain Output	
	2	X	Master IIC Clock Output (CMOS Push-Pull)	

Mode Setting for Port1, P2.2, Port3 Alternative Function

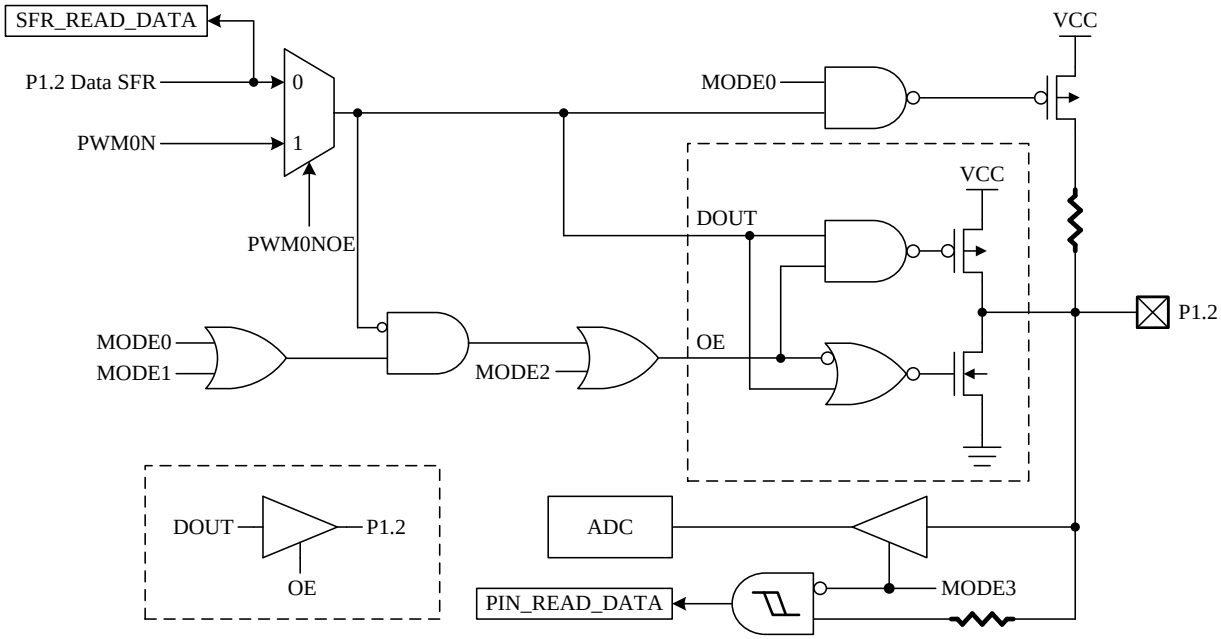
For tables above, a **"COMS Output"** pin means it can sink and drive at least 4mA current. It is not recommended to use such pin as input function.

An **"Open Drain"** pin means it can sink at least 4mA current but only drive a small current (<20μA). It can be used as input or output function and typically needs an external pull up resistor.

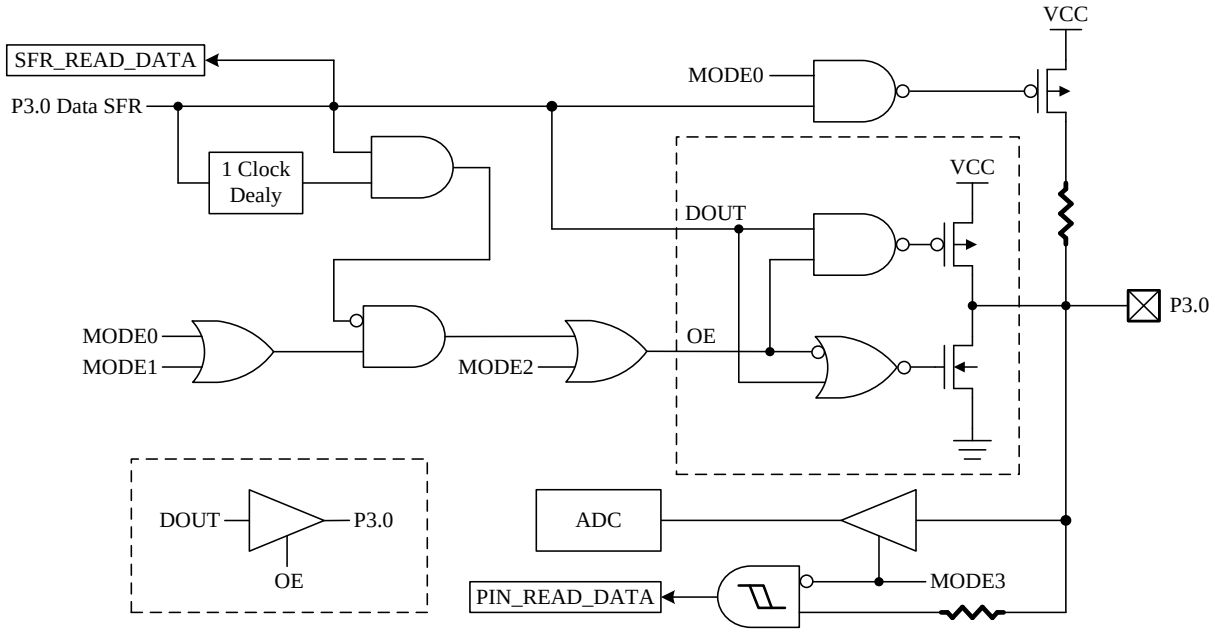
An 8051 standard pin is a **"Pseudo Open Drain"** pin. It can sink at least 4 mA current when output is at low level, and drives at least 4 mA current for 1~2 clock cycle when output transits from low to high, then keeps driving a small current (<20μA) to maintain the pin at high level. It can be used as input or output function.



P1.0 Pin Structure



P1.2 Pin Structure



P3.0 Pin Structure

SFR **90h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

90h.7~0 **P1:** Port1 data

SFR **A0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

A0h.2 **P2.2:** P2.2 data

SFR **B0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

B0h.7~0 **P3:** Port3 data

SFR **A2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODL	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A2h.7~6 **P1MOD3:** P1.3 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A2h.5~4 **P1MOD2:** P1.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.2 is ADC input

A2h.3~2 **P1MOD1:** P1.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A2h.1~0 **P1MOD0:** P1.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.0 is ADC input

SFR **A3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODH	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A3h.7~6 **P1MOD7:** P1.7 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A3h.5~4 **P1MOD6:** P1.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.6 is ADC input

A3h.3~2 **P1MOD5:** P1.5 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A3h.1~0 **P1MOD4:** P1.4 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

SFR **A4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODL	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A4h.7~6 **P3MOD3:** P3.3 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.3 is ADC input

A4h.5~4 **P3MOD2:** P3.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.2 is ADC input

A4h.3~2 **P3MOD1:** P3.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.1 is ADC input

A4h.1~0 **P3MOD0:** P3.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.0 is ADC input

SFR **A5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODH	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A5h.7~6 **P3MOD7:** P3.7 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.7 is ADC input

A5h.5~4 **P3MOD6:** P3.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.6 is ADC input

A5h.3~2 **P3MOD5:** P3.5 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.5 is ADC input

A5h.1~0 **P3MOD4:** P3.4 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.4 is ADC input

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1OE	PWM0POE	PWM0NOE	T2OE	T1OE	T0OE	P2MOD2	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	1

A6h.7 **PWM1OE:** PWM1 signal output enable
0: Disable PWM1 signal output to P3.3
1: Enable PWM1 signal output to P3.3

A6h.6 **PWM0POE:** PWM0P signal output enable
0: Disable PWM0P signal output to P3.5
1: Enable PWM0P signal output to P3.5

A6h.5 **PWM0NOE:** PWM0N signal output enable
0: Disable PWM0N signal output to P1.2
1: Enable PWM0N signal output to P1.2

A6h.4 **T2OE:** Timer2 signal output enable
0: Disable Timer2 overflow divided by 2 output to P1.0
1: Enable Timer2 overflow divided by 2 output to P1.0

A6h.3 **T1OE:** Timer1 signal output enable
0: Disable Timer1 overflow divided by 2 output to P3.5
1: Enable Timer1 overflow divided by 2 output to P3.5

A6h.2 **T0OE:** Timer0 signal output enable
0: Disable Timer0 overflow divided by 64 output to P3.4
1: Enable Timer0 overflow divided by 64 output to P3.4

A6h.1~0 **P2MOD2:** P2.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P2.2 is ADC input

SFR **C1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP1CON	CMP1EN	CMP1HYS	–	SYNDBT				
R/W	R/W	R/W	–	R/W				
Reset	0	0	–	0	0	0	0	0

C1h.7 **CMP1EN:** CMP1 enable
0: CMP1 disable
1: CMP1 enable, P1.3, P1.4 are CMP1 input

SFR **C2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2CON	CMP2EN	CMP2HYS	CMP2VRF					
R/W	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

C2h.7 **CMP2EN:** CMP2 enable
0: CMP2 disable
1: CMP2 enable, P1.5 is CMP2 input

SFR **C3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP3CON	CMP3EN	CMP3HYS	CMP3VRF					
R/W	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

C3h.7 **CMP3EN:** CMP3 enable
0: CMP3 disable
1: CMP3 enable, P1.7 is CMP3 input

SFR **C4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP4CON	CMP4EN	CMP4HYS	CMP4VRF					
R/W	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

C4h.7 **CMP4EN:** CMP4 enable
0: CMP4 disable
1: CMP4 enable, P1.6 is CMP4 input

SFR **C5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP5CON	CMP5EN	CMP5HYS	CMP5VRF					
R/W	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

C5h.7 **CMP5EN:** CMP5 enable
0: CMP5 disable
1: CMP5 enable, P3.2 is CMP5 input

SFR **E1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MICON	MIEN	MIACKO	MIIF	MIACKI	MISTART	MISTOP	MICR	
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	
Reset	0	0	0	0	0	1	0	0

E1h.7 **MIEN:** Master IIC enable
0: Master IIC disable
1: Master IIC enable, P3.0, P3.1 are Master IIC functional pins

SFR **EEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPCON	OPAEN	–	OPOE	OPFUNC		OPGAIN		
R/W	R/W	–	R/W	R/W		R/W		
Reset	0	–	0	0	0	0	0	0

EEh.7 **OPAEN:** OP-Amp enable
0: OP-Amp disable
1: OP-Amp enable, P1.0, P1.1, P16 can be defined as OP-Amp functional pins by OPOE, OPFUNC and OPMOD

EEh.5 **OPOE:** OP-Amp output enable
0: OP-Amp output disable
1: OP-Amp output enable, P1.6 is OP-Amp output when OPAEN=1

EEh.4~3 **OPFUNC:** OP-Amp function select
Normal Mode (OPMOD=0)
00: [IP]OPP (P1.0), [IN]VSS with Inter-Gain, P1.0 is OPA input
01: [IP]VSS, [IN]OPN (P1.1) with Inter-Gain, P1.1 is OPA input
10: [IP]VSS with 1K Res., [IN]OPN (P1.1) with Inter-Gain, P1.1 is OPA input
11: [IP]OPP (P1.0), [IN]OPN (P1.1), P1.0 and P1.1 are OPA inputs
Calibration Mode (OPMOD=1)
00: [IP]Vtrim, [IN]Vtrim (Vtrim = VSS or VBG, defined by CVRFS)
01: [IP]VSS, [IN]VSS with Inter-Gain
10: [IP]VSS with 1K Res., [IN]VSS with Inter-Gain
11: [IP]OPP (P1.0), [IN]OPN (P1.1), P1.0 and P1.1 are OPA inputs

SFR **EFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPCAL	OPOUT	OPMOD	CVRFS	OPADJ				
R/W	R/W	R/W	R/W	R/W				
Reset	0	0	0	0	0	0	0	0

EFh.6 **OPMOD:** OP-Amp operating mode
0: Normal mode
1: Calibration mode

8. Timers

Timer0, Timer1 and Timer2 are provided as standard 8051 compatible timer/counter. Compare to the traditional 12T 8051, the chip's Timer0/1/2 use 2 System clock cycle as the time base unit. That is, in timer mode, these timers increase at every “2 System clock” rate; in counter mode, T0/T1/T2 pin input pulse must be wider than 2 System clock to be seen by this device. In addition to the standard 8051 timers function. The T0O pin can output the “Timer0 overflow divided by 64” signal, the T1O pin can output the “Timer1 overflow divided by 2” signal, and the T2O pin can output the “Timer2 overflow divided by 2” signal. Timer3 is provided for a real-time like clock count, when its time base is FRC/512.

8.1 Timer0/1

TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the Timer0/1, with the timer/counter values stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.7 **TF1:** Timer1 overflow flag
Set by H/W when Timer/Counter 1 overflows.
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.6 **TR1:** Timer1 run control
0: Timer1 stops
1: Timer1 runs

88h.5 **TF0:** Timer0 overflow flag
Set by H/W when Timer/Counter 0 overflows.
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.4 **TR0:** Timer0 run control
0: Timer0 stops
1: Timer0 runs

SFR **89h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

89h.7 **GATE1:** Timer1 gating control bit
0: Timer1 enable when TR1 bit is set
1: Timer1 enable only while the INT1 pin is high and TR1 bit is set

89h.6 **CT1N:** Timer1 Counter/Timer select bit
0: Timer mode, Timer1 data increases at 2 System clock cycle rate
1: Counter mode, Timer1 data increases at T1 pin’s negative edge

89h.5~4 **TMOD1:** Timer1 mode select
00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow.
11: Timer1 stops

89h.3 **GATE0:** Timer0 gating control bit
0: Timer0 enable when TR0 bit is set
1: Timer0 enable only while the INT0 pin is high and TR0 bit is set

89h.2 **CT0N:** Timer0 Counter/Timer select bit
0: Timer mode, Timer0 data increases at 2 System clock cycle rate
1: Counter mode, Timer0 data increases at T0 pin’s negative edge

89h.1~0 **TMOD0:** Timer0 mode select
00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow.
11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.

SFR **8Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL0	TL0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ah.7~0 **TL0:** Timer0 data low byte

SFR **8Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL1	TL1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Bh.7~0 **TL1:** Timer1 data low byte

SFR **8Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH0	TH0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ch.7~0 **TH0:** Timer0 data high byte

SFR **8Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH1	TH1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Dh.7~0 **TH1:** Timer1 data high byte

Note: also refer to Section 6 for more information about Timer0/1 Interrupt enable and priority.
Note: also refer to Section 7 for more information about T0O/T1O pin output setting.

8.2 Timer2

Timer2 is controlled through the TCON2 register with the low and high bytes of Timer/Counter 2 stored in TL2 and TH2 and the low and high bytes of the Timer2 reload/capture registers stored in RCAP2L and RCAP2H.

SFR **C8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

C8h.7 **TF2:** Timer2 overflow flag
Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.

C8h.6 **EXF2:** T2EX interrupt pin falling edge flag
Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.

C8h.5 **RCLK:** UART receive clock control bit
0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3
1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3

C8h.4 **TCLK:** UART transmit clock control bit
0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3
1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3

C8h.3 **EXEN2:** T2EX pin enable
0: T2EX pin disable
1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0

C8h.2 **TR2:** Timer2 run control
0: Timer2 stops
1: Timer2 runs

C8h.1 **CT2N:** Timer2 Counter/Timer select bit
0: Timer mode, Timer2 data increases at 2 System clock cycle rate
1: Counter mode, Timer2 data increases at T2 pin's negative edge

C8h.0 **CPRL2N:** Timer2 Capture/Reload control bit
0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1
1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1
If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow

SFR **CAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2L	RCP2L							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CAh.7~0 **RCP2L:** Timer2 reload/capture data low byte

SFR **CBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2H	RCP2H							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CBh.7~0 **RCP2H:** Timer2 reload/capture data high byte

SFR **CCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL2	TL2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CCh.7~0 **TL2:** Timer2 data low byte

SFR **CDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH2	TH2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CDh.7~0 **TH2:** Timer2 data high byte

Note: also refer to Section 6 for more information about Timer2 Interrupt enable and priority.
Note: also refer to Section 7 for more information about T2O pin output setting.

8.3 Timer3

Timer3 works as a time-base counter, which generates interrupts periodically. It generates an interrupt flag (TF3) with the clock divided by 32768, 16384, 8192, or 128 depending on the TM3PSC bits. The Timer3 clock sources are Slow clock (SRC) or FRC 16.5888MHz/512.

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	TM3CKS	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.6 **TM3CKS:** Timer3 clock source select
0: SRC
1: FRC 16.5888MHz/512 (32.4KHz)

94h.1~0 **TM3PSC:** Timer3 interrupt rate control select
00: Interrupt rate is 32768 Timer3 clock cycle
01: Interrupt rate is 16384 Timer3 clock cycle
10: Interrupt rate is 8192 Timer3 clock cycle
11: Interrupt rate is 128 Timer3 clock cycle

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	–	ADIF	–	IE2	P1IF	TF3
R/W	–	–	–	R/W	–	R/W	R/W	R/W
Reset	–	–	–	0	–	0	0	0

95h.0 **TF3:** Timer 3 interrupt flag
Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W writes FEh to INTFLG to clear this bit.

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W
Reset	0	0	–	0	0	0	–	0

F8h.6 **CLRTM3:** Set to clear Timer3, H/W auto clear it at next clock cycle

Note: also refer to Section 6 for more information about Timer3 Interrupt enable and priority.

8.4 T0O, T1O and T2O Output Control

This device can generate various frequency waveform pin output (in CMOS push pull format) for Buzzer. The T0O, T1O and T2O waveform is divided by Timer0/Timer1/Timer2 overflow signal. The T0O waveform is Timer0 overflow divided by 64, T1O waveform is Timer1 overflow divided by 2, and T2O waveform is Timer2 overflow divided by 2. User can control their frequency by Timers auto reload speed. Set T0OE, T1OE and T2OE SFRs can output these waveforms.

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1OE	PWM0POE	PWM0NOE	T2OE	T1OE	T0OE	P2MOD2	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	1

A6h.4 **T2OE:** Timer2 signal output enable
0: Disable Timer2 overflow divided by 2 output to P1.0
1: Enable Timer2 overflow divided by 2 output to P1.0

A6h.3 **T1OE:** Timer1 signal output enable
0: Disable Timer1 overflow divided by 2 output to P3.5
1: Enable Timer1 overflow divided by 2 output to P3.5

A6h.2 **T0OE:** Timer0 signal output enable
0: Disable Timer0 overflow divided by 64 output to P3.4
1: Enable Timer0 overflow divided by 64 output to P3.4

9. UART

The UART uses SCON and SBUF SFRs. SCON is the control register, SBUF is the data register. Data is written to SBUF for transmission and SBUF is read to obtain received data. The received data and transmitted data registers are completely independent. In addition to standard 8051's full duplex mode, this chip also provides one wire mode. If the UART1W bit is set, both transmit and receive data use P3.1 pin.

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.7 **SMOD:** UART double baud rate control bit
0: Disable UART double baud rate
1: Enable UART double baud rate

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	TM3CKS	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.7 **UART1W:** One wire UART mode enable, both TXD/RXD use P3.1 pin
0: Disable one wire UART mode
1: Enable one wire UART mode

SFR **98h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

98h.7~6 **SM0,SM1:** Serial port mode select bit 0,1
00: Mode0: 8 bit shift register, Baud Rate=$F_{SYSCLK}/2$
01: Mode1: 8 bit UART, Baud Rate is variable
10: Mode2: 9 bit UART, Baud Rate=$F_{SYSCLK}/32$ or /64
11: Mode3: 9 bit UART, Baud Rate is variable

98h.5 **SM2:** Serial port mode select bit 2
SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

98h.4 **REN:** UART reception enable
0: Disable reception
1: Enable reception

98h.3 **TB8:** Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3

98h.2 **RB8:** Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit in Mode 1 if SM2=0

98h.1 **TI:** Transmit interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.

98h.0 **RI:** Receive interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

SFR **99h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF	SBUF							
R/W	R/W							
Reset	–	–	–	–	–	–	–	–

99h.7~0 **SBUF:** UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

F_{SYSCLK} denotes System clock frequency.

- Mode 0:
  Baud Rate=$F_{SYSCLK}/2$
- Mode 1, 3: if using Timer1 auto reload mode
  Baud Rate= (SMOD+1) x F_{SYSCLK}/ (32x2x (256–TH1))
- Mode 1, 3: if using Timer2
  Baud Rate=Timer2 overflow rate/16=F_{SYSCLK}/ (32x (65536–RCP2H, RCP2L))
- Mode 2:
  Baud Rate= (SMOD+1) x $F_{SYSCLK}/64$

Note: also refer to Section 6 for more information about UART Interrupt enable and priority.
Note: also refer to Section 8 for more information about how Timer2 controls UART clock.

10. PWMs

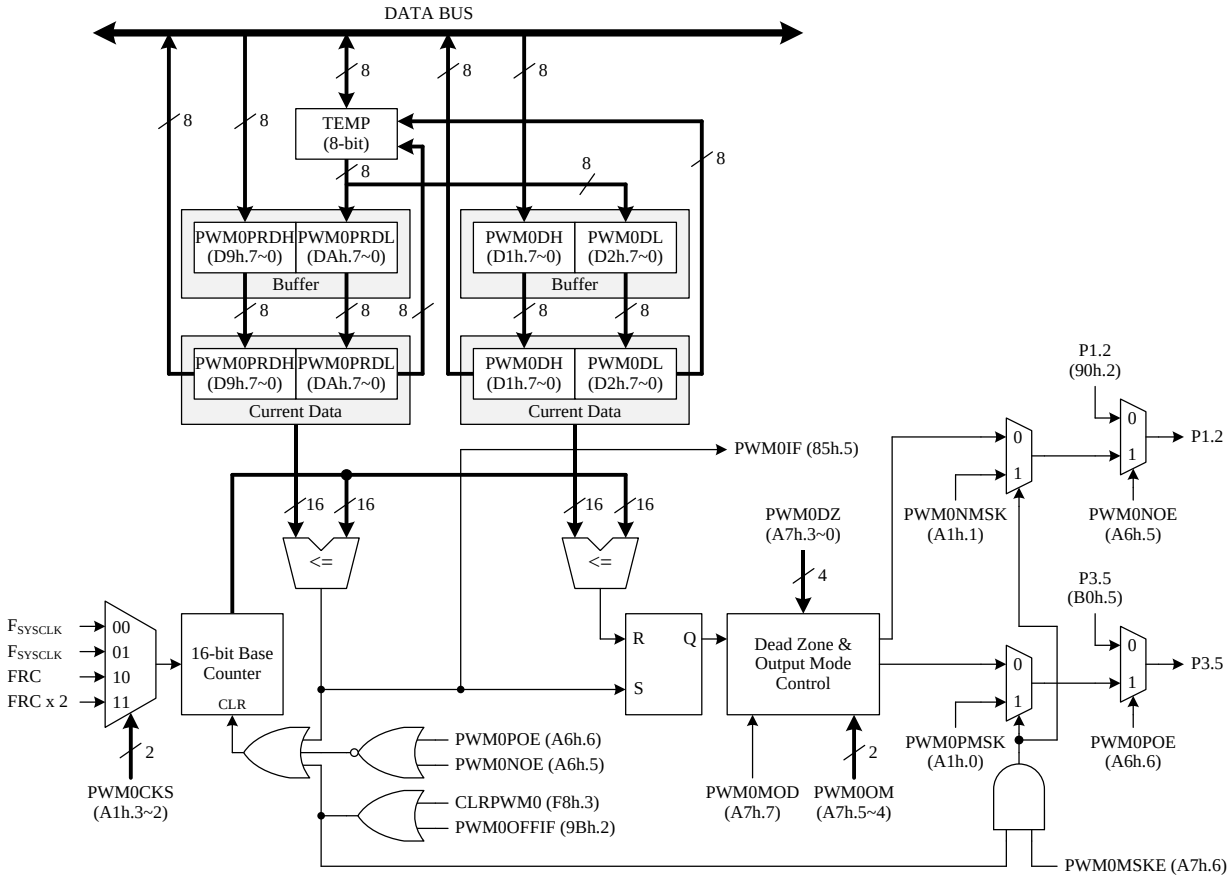
This Chip has two independent 16-bit PWM modules, PWM0 and PWM1. The PWM can generate varies frequency waveform with 65536 duty resolution on the basis of the PWM clock. The PWM clock can select FRC double frequency (FRC x 2), FRC or F_{SYSCLK} as its clock source.

The pin mode SFR controls the PWM output waveform format. Mode1 makes the PWM open drain output and Mode2 makes the PWM CMOS push-pull output. (***see section 7***)

The 16-bit PWM0PRD, PWM0D, PWM1PRD, PWM1D registers all have a low and high byte structure. The high bytes can be directly accessed, but as the low bytes can only be accessed via an internal 8-bit buffer, reading or writing to these register pairs must be carried out in a specific way. The important point to notes is that data transfer to and from the 8-bit buffer and its related low byte only takes place when write or read operation to its corresponding high bytes is executed. Briefly speaking, write low byte first and then high byte; read high byte first and then low byte.

10.1 PWM0

The PWM0POE bit is used to select the output for PWM0P, and the PWM0NOE bit is used to select the output for PWM0N. These two bits also can be PWM0 control bit. If both bits are cleared, the PWM0 will be cleared and stopped, otherwise the PWM0 is running. The CLRPWM0 bit has the same function. When CLRPWM0 bit is set, the PWM0 will be cleared and held, otherwise the PWM0 is running. Besides, the PWM0 also be cleared and held when the PWM0OFFIF bit is set by H/W, the PWM0OFFIF bit is a flag comes from Phase Protect Detector (PPD) module. The PWM0 structure is shown as follow.



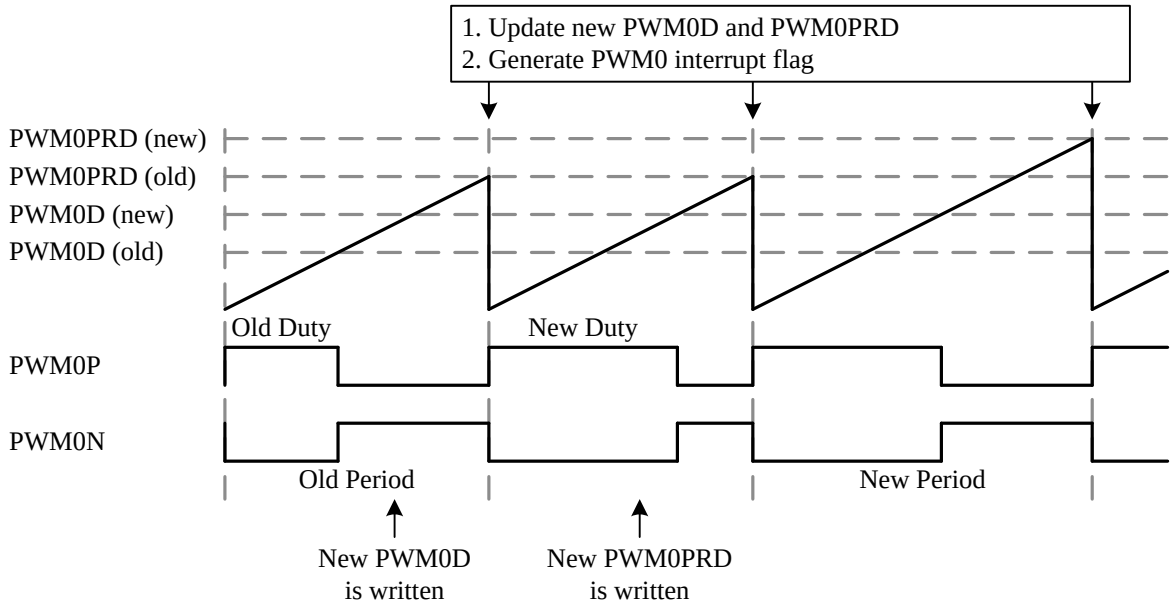
PWM0 Structure

The PWM0 duty cycle can be changed by writing to PWM0DH and PWM0DL. The PWM0 output signal resets to a low level whenever the 16-bit base counter matches the 16-bit PWM0 duty register {PWM0DH, PWM0DL}. The PWM0 period can be set by writing the period value to the PWM0PRDH and PWM0PRDL registers. After writing the PWM0D or PWM0PRD register, the new values will immediately save to their own buffer. H/W will update these values at the end of current period or while PWM0 is cleared. At the end of current period, H/W will set the PWM0IF bit and generate an interrupt if a PWM0 interrupt is enabled.

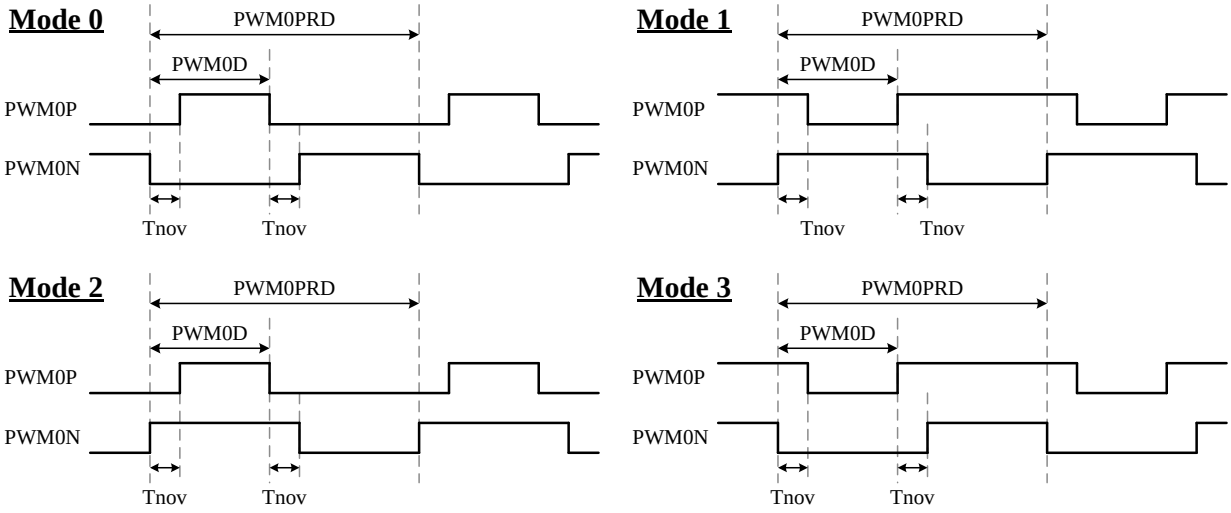
The PWM0 has two operation modes, normal mode and half-bridge mode. PWM0 output signal can be output via PWM0P (P3.5) and PWM0N (P1.2) with four different modes. These two outputs are non-overlapped with time interval Tnov. Non-overlapping time interval is also named as dead zone or dead band. Tnov is determined by setting PWM0DZ bits. The value 0~15 of PWM0DZ map onto 0~14, 16 PWM0CLK cycles respectively. If PWM0DZ=0, PWM0 outputs is directly passed to PWM0P and PWM0N so that waveforms of them have the same duty cycle. Note that, if high pulse width or low pulse width of PWM0 output is shorter than Tnov, the real waveforms of these two outputs will different from the expected waveforms. If the PWM0MSKE bit is set, the outputs will be masked to force output fix signal while S/W set the CLRPWM0 bit or the PWM0OFFIF flag is set by H/W.

10.1.1 Normal Mode

The normal mode PWM is a simple structure, which switches its output high and low at uniform repeatable intervals. The PWM0D is the output duty cycle, and the output period is PWM0PRD+1. The output waveform and the output modes are shown below.



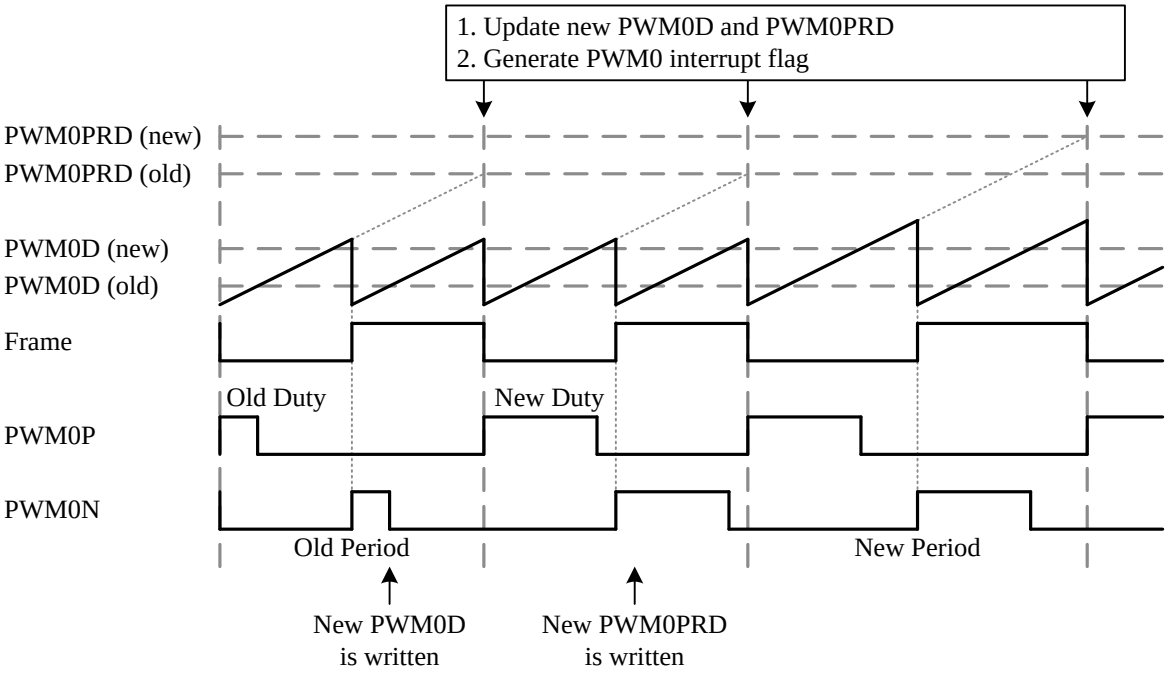
PWM0 normal mode output waveform (PWM0OM=0, PWM0DZ=0)



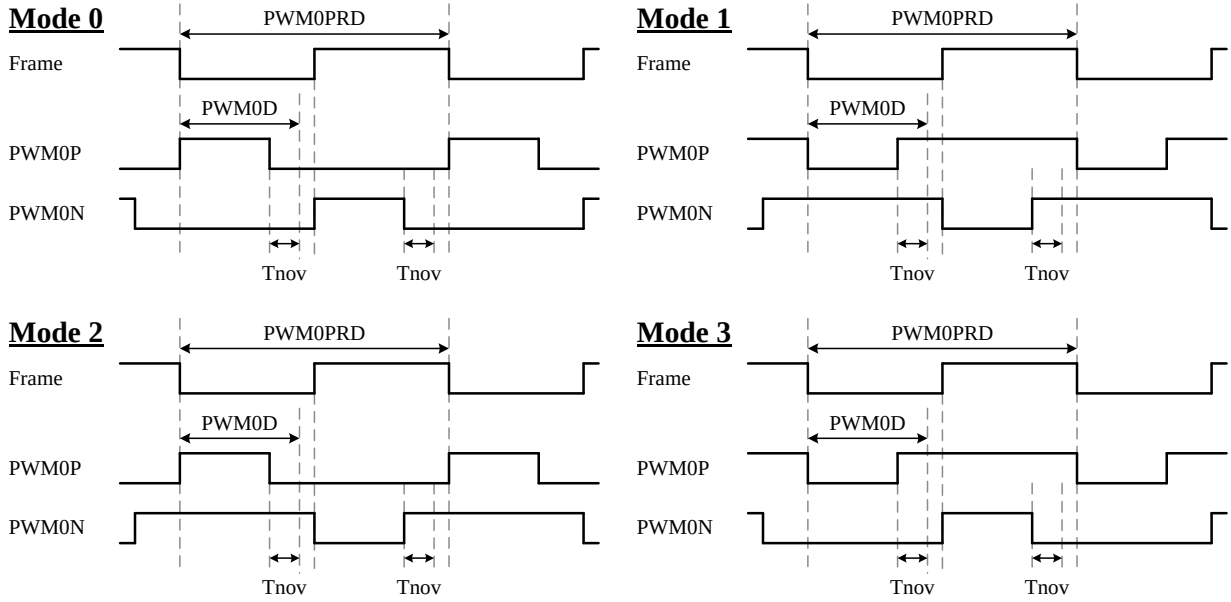
PWM0 normal mode output modes

10.1.2 Half-Bridge Mode

The half-bridge mode PWM is similar to the normal mode. It has two frames in a period, PWM0P only output in the first frame, PWM0N only output in the second frame. The width of these two frames must be same, so their width is the integer part of PWM0PRD/2. Because each output channel only output in one frame, the maximum duty cycle is same as the width of a frame. If the PWM0D is larger than PWM0PRD/2, H/W will force set the duty cycle to PWM0PRD/2. Following figure shows the output waveform and the output modes.



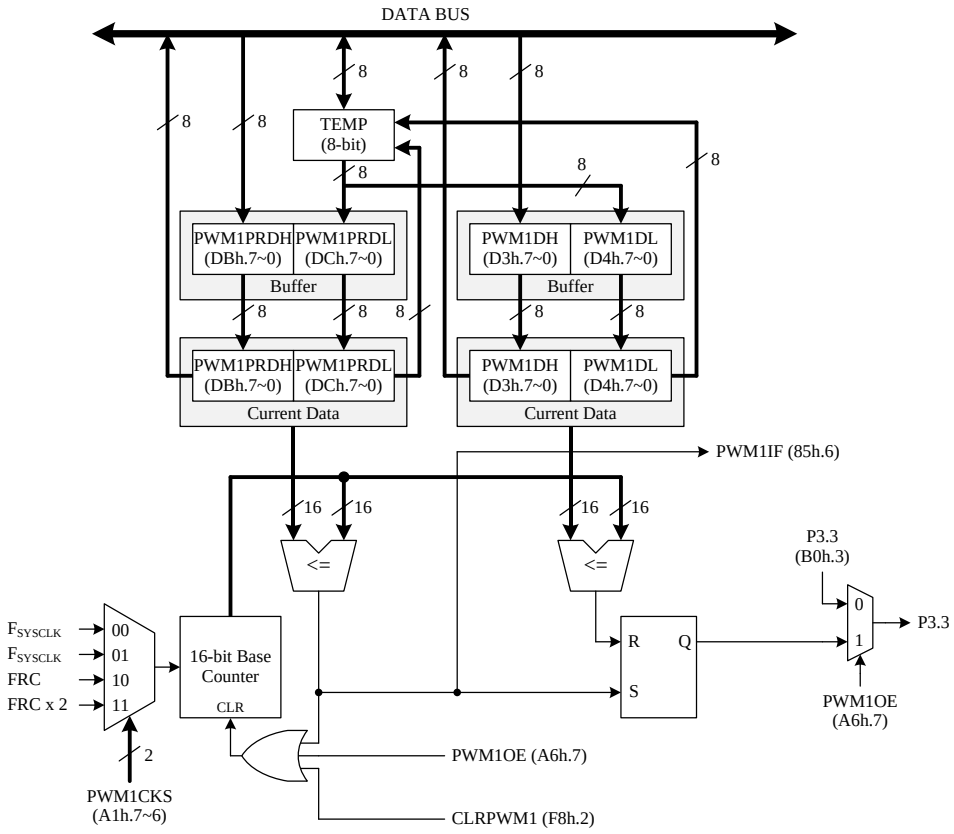
PWM0 half-bridge mode output waveform (PWM0OM=0, PWM0DZ=0)



PWM0 half-bridge mode output modes

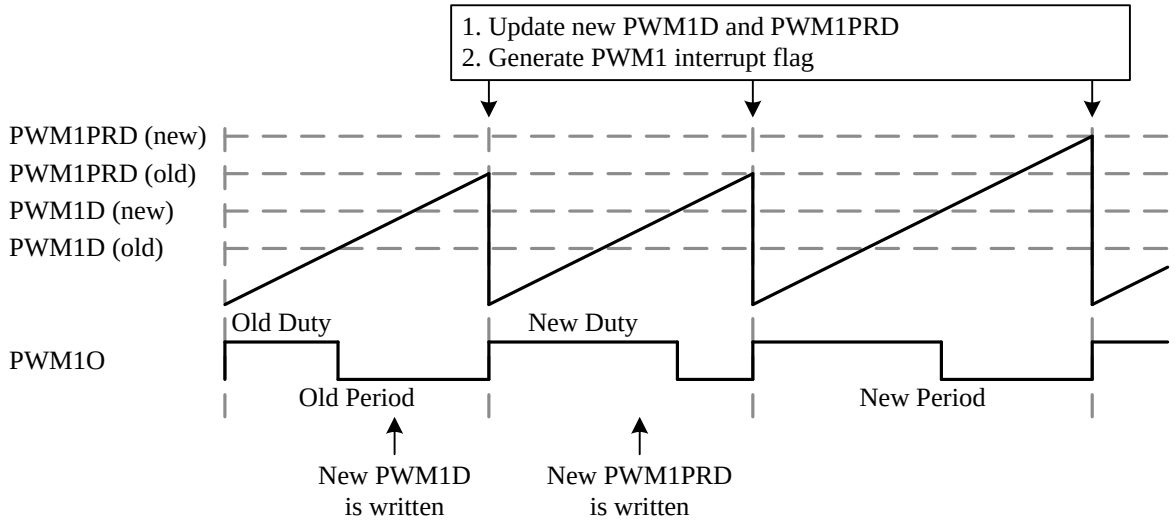
10.2 PWM1

The PWM1 is almost the same as the PWM0, except it has normal mode only and has only one output. The PWM1OE bit is used to select the output for PWM1O. This bit also can be PWM1 control bit. If this bit is cleared, the PWM1 will be cleared and stopped, otherwise the PWM1 is running. The CLRPWM1 bit has the same function. When CLRPWM1 bit is set, the PWM1 will be cleared and held, otherwise the PWM1 is running. The PWM1 structure is shown as follow.



PWM1 Structure

Same as the PWM0, the PWM1D and PWM1PRD have their own buffer. After writing the PWM1D or PWM1PRD register, the new values will immediately save to their own buffer. H/W will update these values at the end of current period or while PWM1 is cleared. At the end of current period, H/W will set the PWM1IF bit and generate an interrupt if a PWM1 interrupt is enabled. The output waveform is shown below.



PWM1 output waveform

SFR **84h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE2	–	PWM1IE	PWM0IE	CMP5IE	CMP4IE	CMP3IE	CMP2IE	CMP1IE
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	0	0	0	0	0	0	0

84h.6 **PWM1IE:** PWM1 interrupt enable
0: Disable PWM1 interrupt
1: Enable PWM1 interrupt

84h.5 **PWM0IE:** PWM0 interrupt enable
0: Disable PWM0 interrupt
1: Enable PWM0 interrupt

SFR **85h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG2	–	PWM1IF	PWM0IF	CMP5IF	CMP4IF	CMP3IF	CMP2IF	CMP1IF
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	0	0	0	0	0	0	0

85h.6 **PWM1IF:** PWM1 interrupt flag
Set by H/W at the end of PWM1 period, S/W writes BFh to INTFLG2 to clear this flag.

85h.5 **PWM0IF:** PWM0 interrupt enable
Set by H/W at the end of PWM0 period, S/W writes DFh to INTFLG2 to clear this flag.

SFR **A1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON	PWM1CKS		–	–	PWM0CKS		PWM0NMSK	PWM0PMSK
R/W	R/W		–	–	R/W		R/W	R/W
Reset	0	0	–	–	0	0	0	0

A1h.7~6 **PWM1CKS:** PWM1 clock source
00: F_{SYSCLK}
01: F_{SYSCLK}
10: FRC
11: FRCx2

A1h.3~2 **PWM0CKS:** PWM0 clock source

00: F_{SYSCLK}
01: F_{SYSCLK}
10: FRC
11: FRCx2

A1h.1 **PWM0NMSK:** PWM0N mask data while CLRPWM0=1 or PWM0OFFIF=1

A1h.0 **PWM0PMSK:** PWM0P mask data while CLRPWM0=1 or PWM0OFFIF=1

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1OE	PWM0POE	PWM0NOE	T2OE	T1OE	T0OE	P2MOD2	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	1

A6h.7 **PWM1OE:** PWM1 signal output enable
0: Disable PWM1 signal output to P3.3
1: Enable PWM1 signal output to P3.3

A6h.6 **PWM0POE:** PWM0P signal output enable
0: Disable PWM0P signal output to P3.5
1: Enable PWM0P signal output to P3.5

A6h.5 **PWM0NOE:** PWM0N signal output enable
0: Disable PWM0N signal output to P1.2
1: Enable PWM0N signal output to P1.2

SFR **A7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON2	PWM0MOD	PWM0MSKE	PWM0OM		PWM0DZ			
R/W	R/W	R/W	R/W		R/W			
Reset	0	0	0	0	0	0	0	0

A7h.7 **PWM0MOD:** PWM0 mode select
0: Normal mode
1: Half-bridge mode

A7h.6 **PWM0MSKE:** PWM0 mask output enable
0: Disable
1: Enable, PWM0P/PWM0N output data are set by PWM0PMSK/PWM0NMSK while CLRPWM0=1 or PWM0OFFIF=1

A7h.5~4 **PWM0OM:** PWM0 output mode select
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A7h.3~0 **PWM0DZ:** PWM0 dead zone
0000~1110: 0 x $T_{PWM0CLK}$ ~ 14 x $T_{PWM0CLK}$
1111: 16 x $T_{PWM0CLK}$

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	CMPIE	PPGDIE	I2CIE	ADIE	EX2	P1IE	TM3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.7 **PWMIE:** PWM0/1 interrupt enable
0: Disable PWM0/1 interrupt
1: Enable PWM0/1 interrupt

SFR **D1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DH	PWM0DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D1h.7~0 **PWM0DH:** PWM0 duty high byte

SFR **D2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

PWM0DL	PWM0DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D2h.7~0 **PWM0DL:** PWM0 duty low byte

SFR **D3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DH	PWM1DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D3h.7~0 **PWM1DH:** PWM1 duty high byte

SFR **D4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DL	PWM1DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D4h.7~0 **PWM1DL:** PWM1 duty low byte

SFR **D9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRDH	PWM0PRDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

D9h.7~0 **PWM0PRDH:** PWM0 period high byte

SFR **DAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRDL	PWM0PRDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DAh.7~0 **PWM0PRDL:** PWM0 period low byte

SFR **DBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRDH	PWM1PRDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DBh.7~0 **PWM1PRDH:** PWM1 period high byte

SFR **DCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRDL	PWM1PRDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DCh.7~0 **PWM1PRDL:** PWM1 period low byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W
Reset	0	0	–	0	0	0	–	0

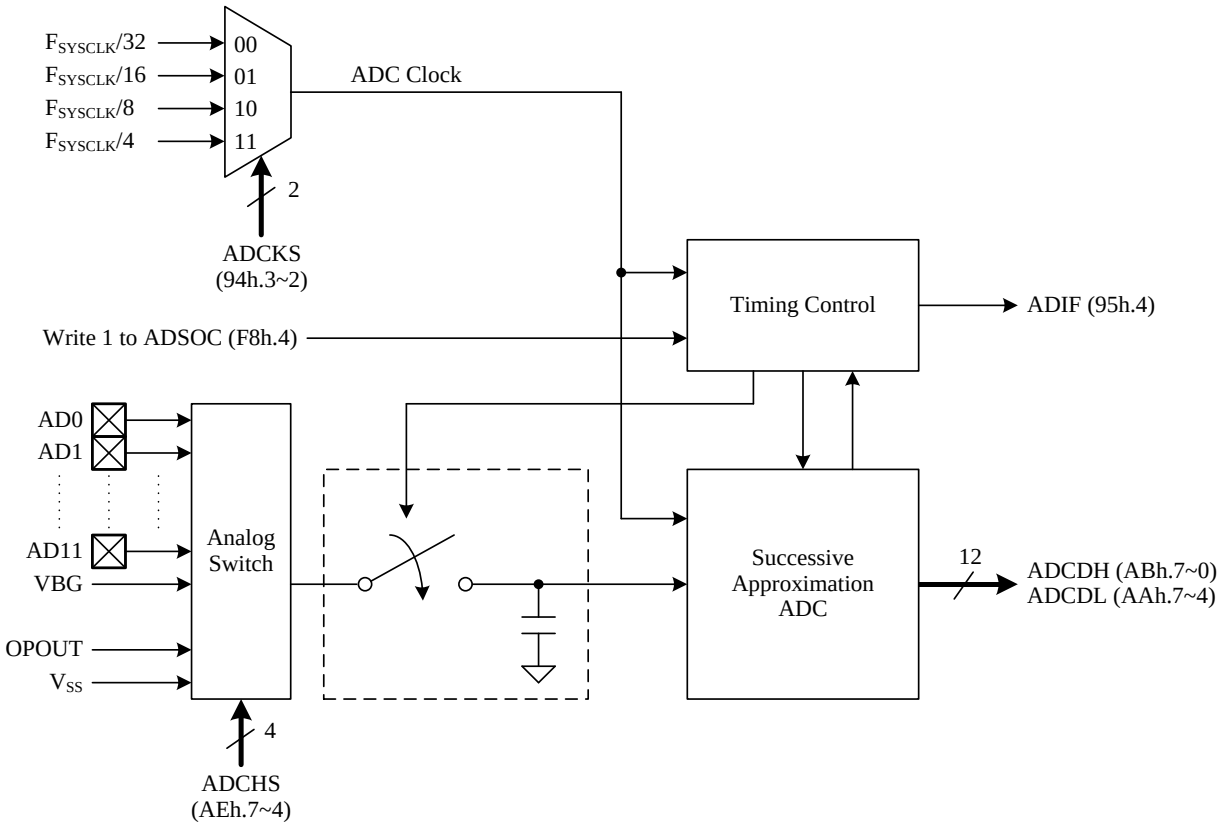
F8h.3 **CLRPWM0:** PWM0 clear enable
0: PWM0 is running
1: PWM0 is cleared and held

F8h.2 **CLRPWM1:** PWM1 clear enable
0: PWM1 is running
1: PWM1 is cleared and held

Note: also refer to Section 7 for more information about PWM pin output setting.

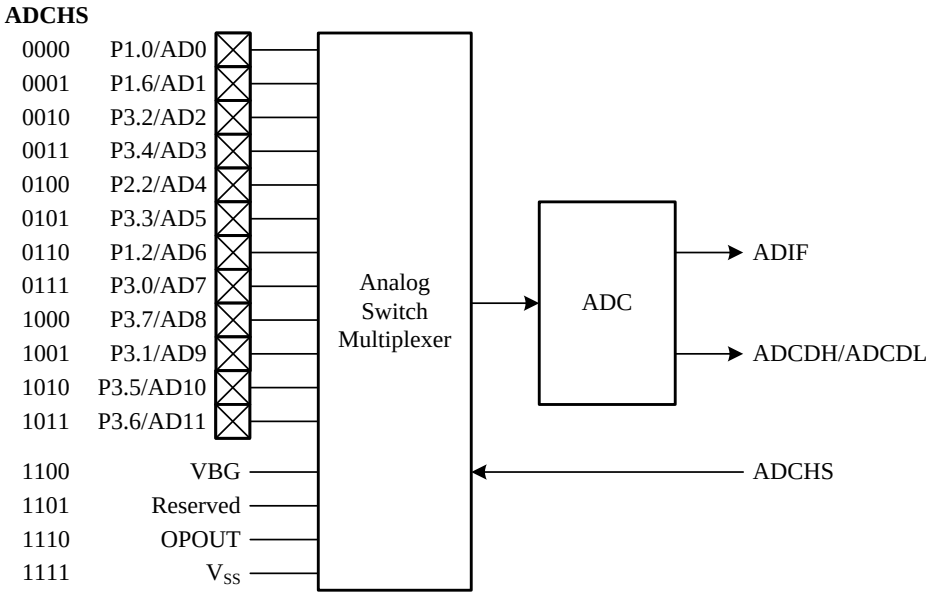
11. ADC

The Chip offers a 12-bit ADC consisting of a 15-channel analog input multiplexer, control register, clock generator, 12-bit successive approximation register, and output data register. To use the ADC, set the ADCKS bit first to choose a proper ADC clock frequency, which must be less than 1 MHz. Then, launch the ADC conversion by setting the ADSOC bit, and H/W will automatic clear it at the end of the conversion. After the end of the conversion, H/W will set the ADIF bit and generate an interrupt if an ADC interrupt is enabled. The ADIF bit can be cleared by writing 0 to this bit or 1 to the ADSOC bit. The analog input level must remain within the range from V_{SS} to V_{CC}.



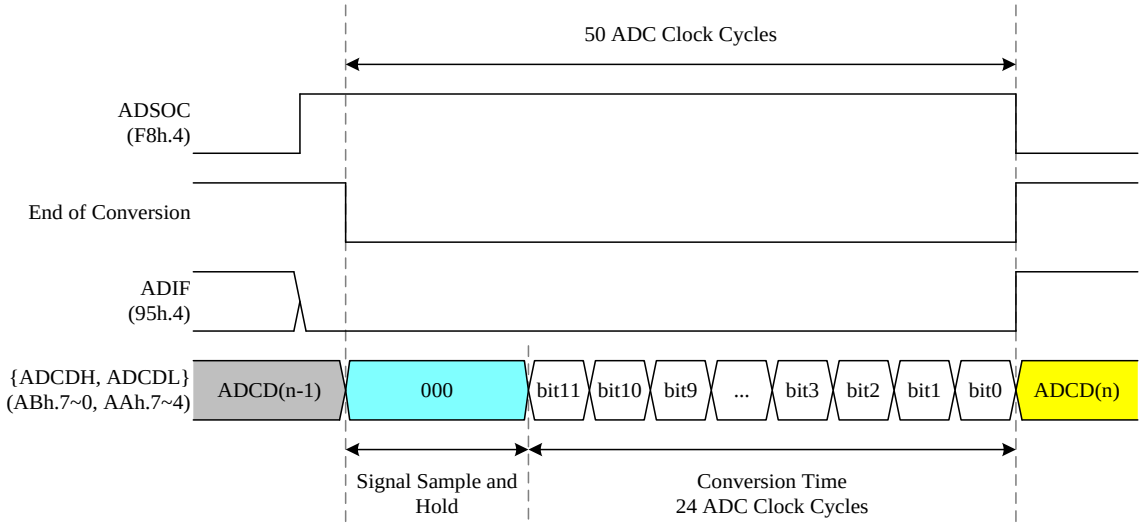
11.1 ADC Channels

The 12-bit ADC has a total of 15 channels, designated AD0~AD11, VBG, OPOUT and V_{SS}. The ADC channels are connected to the analog input pins via the analog switch multiplexer. The analog switch multiplexer is controlled by the ADCHS register. The Chip offers up to 12 analog input pins, designated AD0~AD11. In addition, there are three analog input pins for voltage reference connections. When ADCHS is set to 1100b, the analog input will connect to VBG, when ADCHS is set to 1110b, the analog input will connect to OPOUT, and when ADCHS is set to 1111b, the analog input will connect to V_{SS}. VBG is an internal voltage reference at 1.22V.



11.2 ADC Conversion Time

The conversion time is the time required for the ADC to convert the voltage. The ADC requires two ADC clock cycles to convert each bit and several clock cycles to sample and hold the input voltage. A total of 50 ADC clock cycles are required to perform the complete conversion. When the conversion time is complete, the ADIF interrupt flag is set by H/W, and the result is loaded into the ADCDH and ADCDL registers of the 12-bit A/D result.



SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	TM3CKS	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.3~2 **ADCKS:** ADC clock rate select
00: $F_{SYSCLK}/32$
01: $F_{SYSCLK}/16$
10: $F_{SYSCLK}/8$
11: $F_{SYSCLK}/4$

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	–	ADIF	–	IE2	P1IF	TF3
R/W	–	–	–	R/W	–	R/W	R/W	R/W
Reset	–	–	–	0	–	0	0	0

95h.4 **ADIF:** ADC interrupt flag
Set by H/W at the end of conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.

SFR **AAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDL	ADCDL				–	–	–	–
R/W	R				–	–	–	–
Reset	–	–	–	–	–	–	–	–

AAh.7~4 **ADCDL:** ADC data bit 3~0

SFR **ABh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDH	ADCDH							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ABh.7~0 **ADCDH:** ADC data bit 11~4

SFR **AEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHSEL	ADCHS				–	–	–	–
R/W	R/W				–	–	–	–
Reset	1	1	1	1	–	–	–	–1

AEh.7~4 **ADCHS:** ADC channel select
0000: AD0 (P1.0)
0001: AD1 (P1.6)
0010: AD2 (P3.2)
0011: AD3 (P3.4)
0100: AD4 (P2.2)
0101: AD5 (P3.3)
0110: AD6 (P1.2)
0111: AD7 (P3.0)
1000: AD8 (P3.7)
1001: AD9 (P3.1)
1010: AD10 (P3.5)
1011: AD11 (P3.6)
1100: VBG (internal Bandgap reference voltage)
1101: Reserved
1110: OPOUT
1111: V_{SS}

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W
Reset	0	0	–	0	0	0	–	0

F8h.4 **ADSOC:** Start ADC conversion

Set the ADSOC bit to start ADC conversion, and the ADSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.

Note: also refer to Section 6 for more information about ADC Interrupt enable and priority.
Note: also refer to Section 7 for more information about ADC pin input setting.

12. Multiplier and divider

The chip provide multiplier and divider have the following functions. The 8 bit operation is fully compatible with industry standard 8051.

- 8 bits × 8 bits = 16 bit (standard 8051)
- 8 bits ÷ 8 bits = 8 bits, 8 bits remainder (standard 8051)
- 16 bits × 16 bits = 32 bit
- 16 bits ÷ 16 bits = 16 bits, 16 bits remainder
- 32 bits ÷ 16 bits = 32 bits, 16 bits remainder

No matter 8bit / 16bit / 32bit operation, it's easy to execute by MUL AB and DIV AB instruction. There is extra SFR EXA/EXA2/EXA3/EXB for 16bit / 32bit multiply and divide operation.

For 8 bit multiplier/divider operation, be sure SFR bit MULDIV16=0 and DIV32=0.

For 16 bit multiplier operation, multiplicand, multiplier and product as follows. 16 bit multiplier takes 16 System clock cycles to execute.

Condition	**SFR bit MULDIV16=1 and DIV32=0**			
Multiplication	**Byte3**	**Byte2**	**Byte1**	**Byte0**
Multiplicand	-	-	EXA	A
Multiplier	-	-	EXB	B
Product	EXB	B	A	EXA
OV	Product (EXB or B) !=0		-	-

For 16 bit divider operation, dividend, divisor, quotient, remainder read as follows. 16 bit divider takes 16 System clock cycles to execute.

Condition	**SFR bit MULDIV16=1 and DIV32=0**			
Division	**Byte3**	**Byte2**	**Byte1**	**Byte0**
Dividend	-	-	EXA	A
Divisor	-	-	EXB	B
Quotient	-	-	A	EXA
Remainder	-	-	B	EXB
OV	Divisor EXB = B =0			

For 32 bits ÷ 16 bits operation, dividend, divisor, quotient, remainder read as follows. 32 bit divider takes 32 System clock cycles to execute.

Condition	**SFR bit MULDIV16=1 and DIV32=1**			
Division	**Byte3**	**Byte2**	**Byte1**	**Byte0**
Dividend	EXA3	EXA2	EXA	A
Divisor	-	-	EXB	B
Quotient	A	EXA	EXA2	EXA3
Remainder	-	-	B	EXB
OV	Divisor EXB=B =0			

SFR **CEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA2	EXA2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CEh.7~0 **EXA2:** Expansion accumulator 2

SFR **CFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA3	EXA3							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CFh.7~0 **EXA3:** Expansion accumulator 3

SFR **E6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA	EXA							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E6h.7~0 **EXA:** Expansion accumulator

SFR **E7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXB	EXB							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E7h.7~0 **EXB:** Expansion B register

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	0	0	0

F7h.3 **DIV32:**
only active when MULDVI16 =1
0: instruction DIV as 16/16 bit division operation
1: instruction DIV as 32/16 bit division operation

F7h.0 **MULDIV16:**
0: instruction MUL/DIV as 8*8, 8/8 operation
1: instruction MUL/DIV as 16*16, 16/16 or 32/16 operation

ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MUL AB	Multiply A by B	1	8/16	A4
DIV AB	Divide A by B	1	8/16/32	84

13. Operational Amplifier

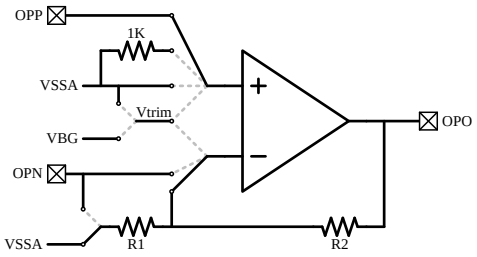
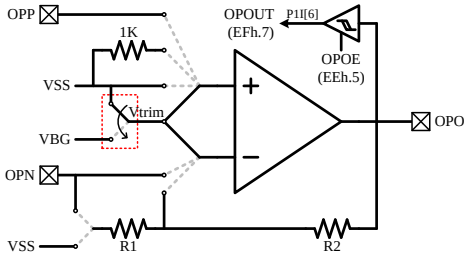
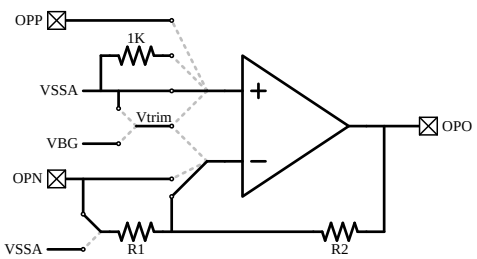
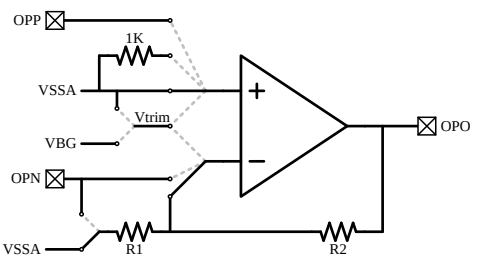
The on-chip OPA is a CMOS amplifier featuring high input impedance, extremely low offset voltage, high gain and high stability. It allows common mode input voltage range which extends 0V to V_{CC} -1.22V. This cost-effective device is suitable for high gain, low frequency and low offset voltage application. As the functional block diagram shown below, the OPA can be configured as four types by setting OPFUNC (EEh.4~3) bits. The OPA is off after IC reset. User can set OPAEN (EEh.7) bit to turn on the feature of OPA.

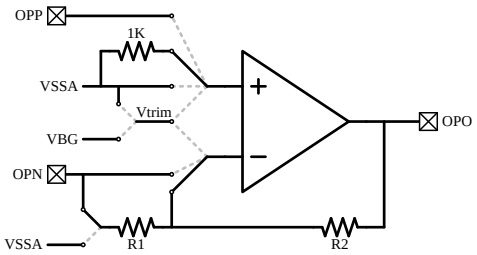
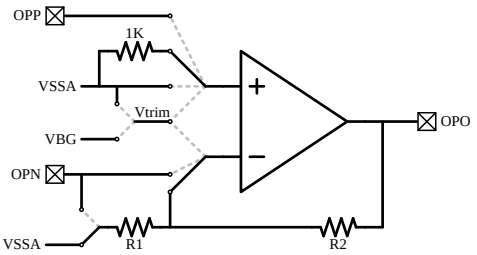
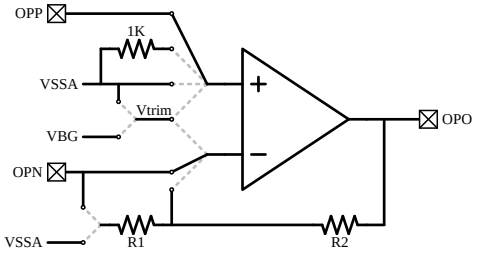
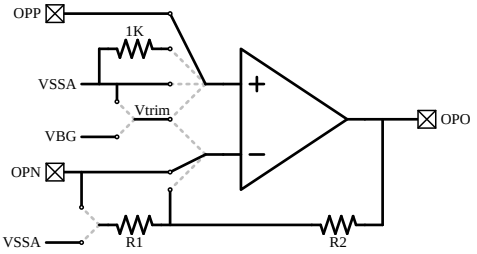
The Chip enter input offset voltage calibration mode by setting OPMOD (EFh.6) bit. The calibration mode has four types which correspond with normal mode four types. Two reference levels, VSS or VBG, can be selected by setting CVRFS (EFh.5) bit while OPFUNC=00. For the calibration procedure, change the OPADJ (EFh.4~0) value from 00h to 1Fh in turn and check OPOUT (EFh.7) bit for each value. Recode OPADJ value when OPOUT goes high. Similarly, change OPADJ value in appositive direction, from 1Fh to 00h in turn and check OPOUT bit for each value. We obtain another OPADJ value when OPOUT bit goes low. Choose one of these two values, or apply the average value as the calibrated OPADJ. Finally clear OPMOD bit to return to normal operation mode. Note that the OPADJ value only can be updated while in calibration mode and OPMOD=1. In additional, the state of OPOUT bit is valid and meaningful only in offset calibration mode with OPFUNC=00 and OPOE=1.

For any GPIO pin, analog I/O function always takes priority over digital functions. When OPA is turn on by setting OPAEN bit, digital paths of related GPIO pins are automatically disable to reduce power consumption.

Feature:

- Low offset voltage: ≤ 2 mV after calibration
- Wide Unity Gain Bandwidth: 2.1 MHz
- Open Loop Gain: 90 dB
- Slew Rate: 2 V/μs

OPFUNC	Normal Mode (OPMOD=0)	Calibration Mode (OPMOD=1)
00		
01		

10		
11		

SFR **EEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPCON	OPAEN	–	OPOE	OPFUNC		OPGAIN		
R/W	R/W	–	R/W	R/W		R/W		
Reset	0	–	0	0	0	0	0	0

EEh.7 **OPAEN:** OP-Amp enable
0: OP-Amp disable
1: OP-Amp enable

EEh.5 **OPOE:** OP-Amp output enable, active in offset calibration mode and OPFUNC=00
0: OP-Amp output disable
1: OP-Amp output enable

EEh.4~3 **OPFUNC:** OP-Amp function select
Normal Mode (OPMOD=0)
00: [IP]OPP, [IN]VSS with Inter-Gain
01: [IP]VSS, [IN]OPN with Inter-Gain
10: [IP]VSS with 1K Res., [IN]OPN with Inter-Gain
11: [IP]OPP, [IN]OPN
Calibration Mode (OPMOD=1)
00: [IP]Vtrim, [IN]Vtrim (Vtrim = VSS or VBG, defined by CVRFS)
01: [IP]VSS, [IN]VSS with Inter-Gain
10: [IP]VSS with 1K Res., [IN]VSS with Inter-Gain
11: [IP]OPP, [IN]OPN

EEh.2~0 **OPGAIN:** OP-Amp internal gain select
000: 20X
001: 25X
010: 30X
011: 35X
100: 100X
101: 105X
110: 110X
111: 115X

SFR **EFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPCAL	OPOUT	OPMOD	CVRFS	OPADJ				
R/W	R/W	R/W	R/W	R/W				
Reset	0	0	0	–	–	–	–	–

EFh.7 **OPOUT:** OPA output state in offset calibration mode and OPFUNC=00
0: $V_{IN+} < V_{IN-}$
1: $V_{IN+} > V_{IN-}$

EFh.6 **OPMOD:** OP-Amp operating mode
0: Normal mode
1: Calibration mode

EFh.5 **CVRFS:** Calibration mode reference level select when OPFUNC=00
0: Select VSS
1: Select VBG

EFh.4~0 **OPADJ:** OPA offset voltage adjustment
00000~11111: $-V_{OS\_MAX} \sim +V_{OS\_MAX}$
Offset calibration of each device has been done before delivery shipping.
User can obtain default value by read this registers after power on.

Note: also refer to Section 7 for more information about OPA pin input/output setting.

14. Analog Comparators

An analog comparator provides the interface between an analog circuit and a digital circuit. It compares magnitude of its non-inverting input V_{IN+} and the one of inverting input V_{IN-}, its output indicates the function of their relative levels. When the magnitude of V_{IN+} is higher than that of V_{IN-}, comparator output logic high. In contrast, comparator output logic low when the magnitude of V_{IN+} is lower than that of V_{IN-}.

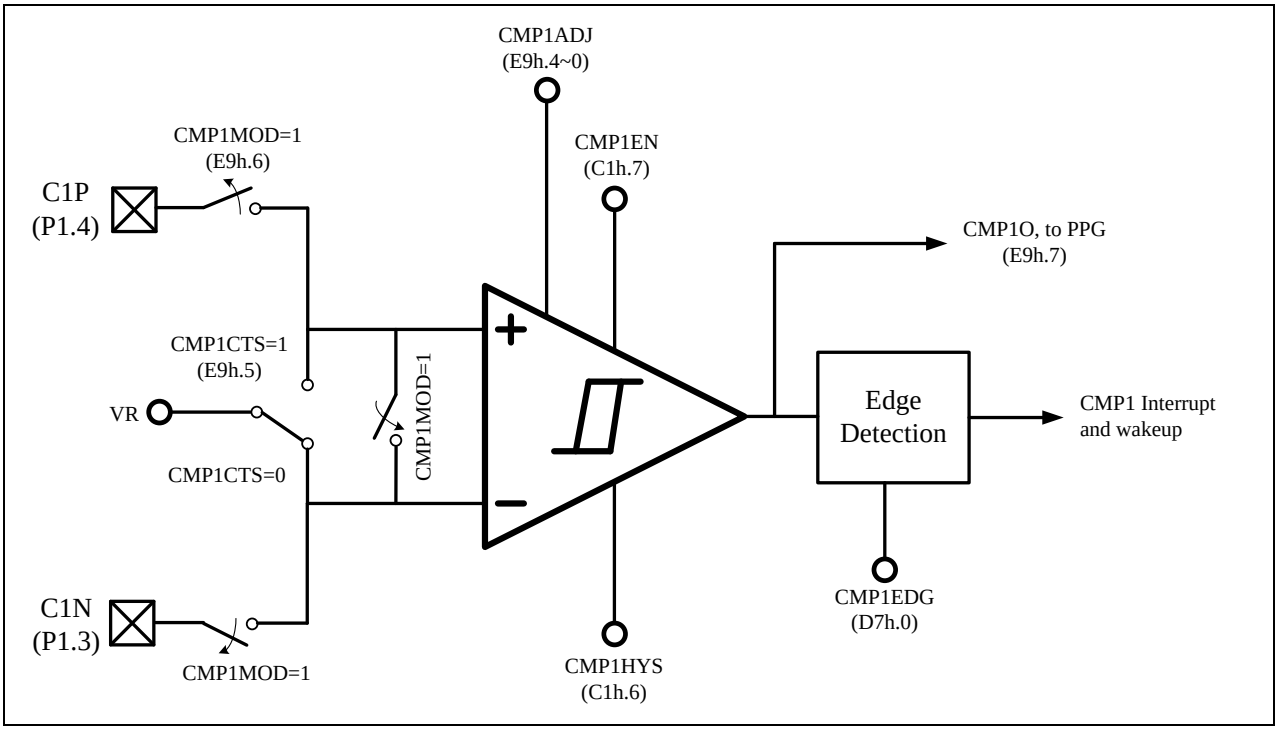
There are five analog comparators, named as CMP1, CMP2, CMP3, CMP4, and CMP5, built in the Chip. Function diagrams of five comparators are illustrated on next three pages. Each comparator can be controlled by setting three registers CMPxCON (C1h~C5h), CMPxCAL (E9h~EDh) and CMPIEDG (D7h), where x = 1~5. CMPx can be turn on by writting CMPxEN bit to 1. If CMPxEN=0, CMPx is turn off to save power consumption and the corresponding output CMPxO hold at logic low.

An amount of separation level can be added to inputs of a comparator to provide hysteresis characteristic to their operation. Hysteresis function of CMPx can be enabled/disabled by writing 1/0 to CMPxHYS bit. The output transition of a comparator may trigger interrupt event. CMPxEDG are used to determine the trigger edge of an interrupt event. IF CMPxEDG=1/0, an output rising-edge/falling-edge transition sets the corresponding interrupt flag CMPxIF (84h.4~0).

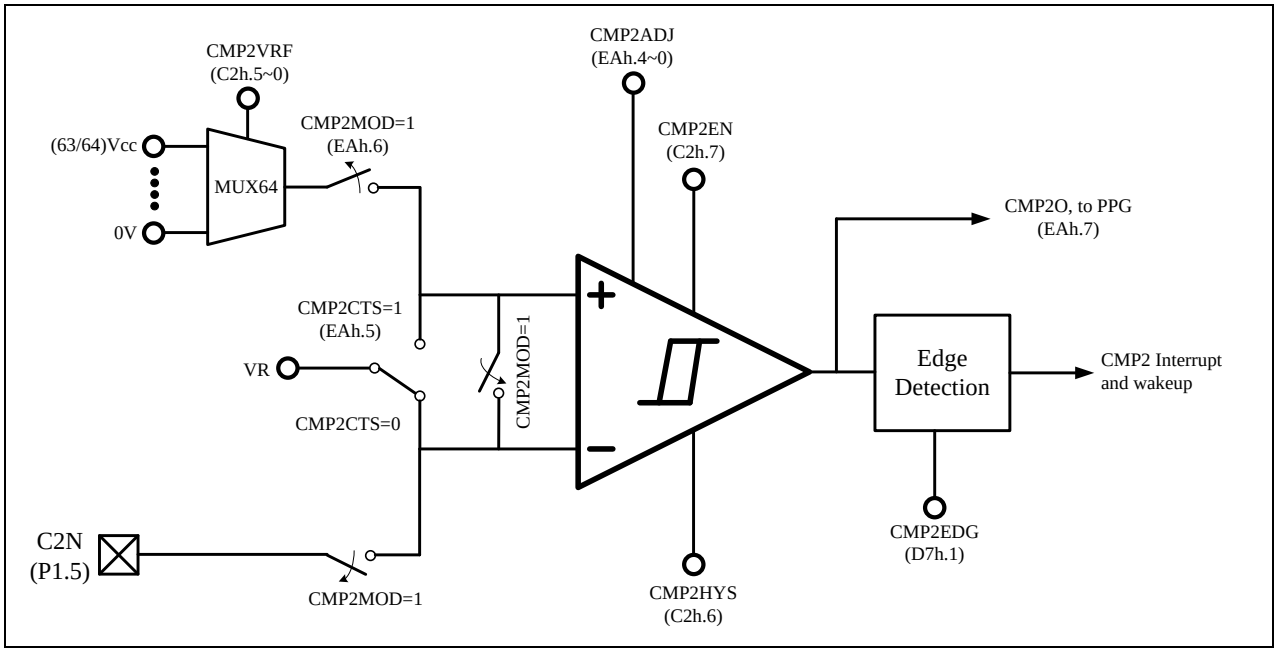
As illustrated function diagrams, inverting inputs C2N, C3N, C4N, and C5N are lead out to GPIO pin P1.5, P1.7, P1.6, and P3.2 respectively. Both non-inverting and inverting inputs of CMP1 are lead out to GPIO pin P1.4 and P1.3 respectively. The non-inverting compare voltage selection of CMP2, CMP3, CMP4, and CMP5 are built in device. A suitable level of V_{IN+} of CMP2, CMP3, CMP4, and CMP5 can be selected for proper operation of your application by setting CMP2VRF, CMP3VRF, CMP4VRF, and CMP5VRF respectively. The state of CMPxO can be obtained by reading CMPxO bit of CMPxCAL register.

The Chip enter input offset voltage calibration mode by setting CMPxMOD bit of CMPxCAL registers. As CMPxMOD is set to 1, both inputs of a comparator are tied together and an internal voltage source VR is fed to inputs at the same time. CMPxCTS bit of CMPxCAL register is used to select the major terminal in offset calibration mode. When CMPxCTS=1/0, the non-inverting/inverting input respectively will be the major terminal to which VR path is connected in calibration mode. Normally, the setting of CMPxCTS does not affect the calibration results. User can use default case in overall calibration procedure. For the calibration procedure, change CMPxADJ value from 00h to 1Fh in turn and check CMPxO for each CMPxADJ. Record the CMPxADJ value when CMPxO goes high. Similarly, change CMPxADJ value in appositive direction, from 1Fh to 00h in turn and check CMPxO for each CMPxADJ. It can obtain another CMPxADJ value when CMPxO goes low. Choose one of two values, or apply the average value as the calibrated CMPxADJ. Finally clear CMPxMOD bit to return to normal operation mode. Note that the CMPxADJ value only can be updated while in calibration mode and CMPxMOD=1.

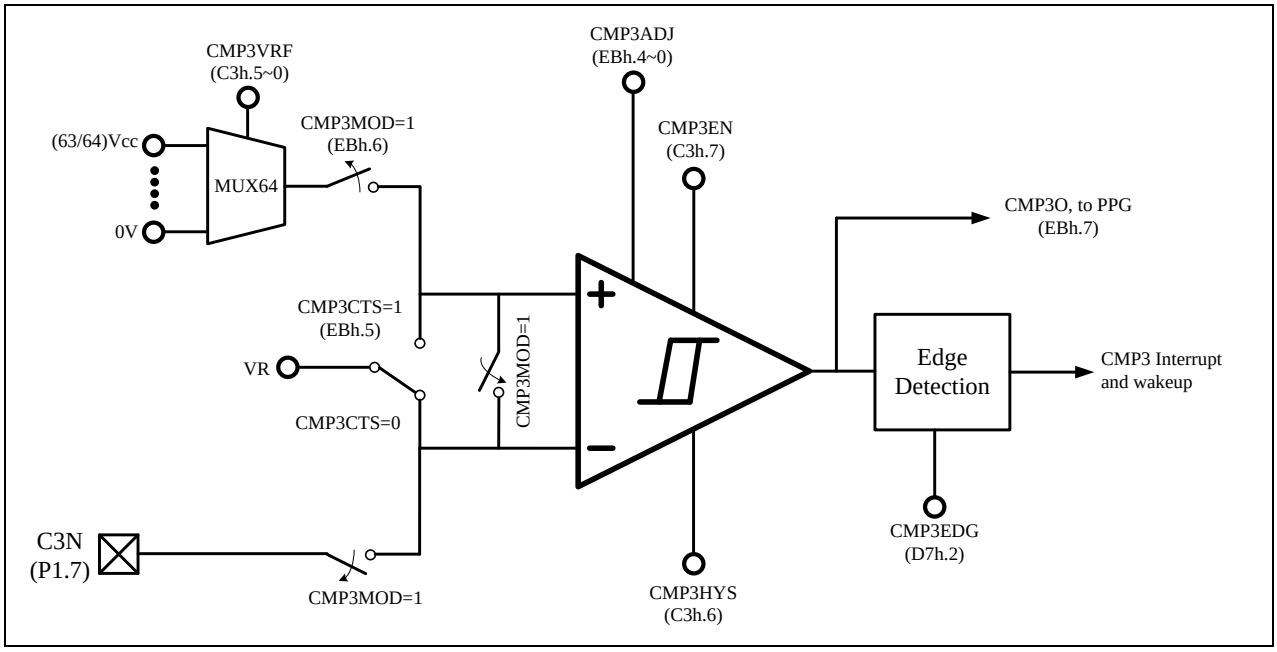
For any GPIO pin, analog function always takes priority over digital functions. When CMPx is turn on by setting CMPxEN bit, digital paths of related GPIO pins are automatically disable to reduce power consumption.



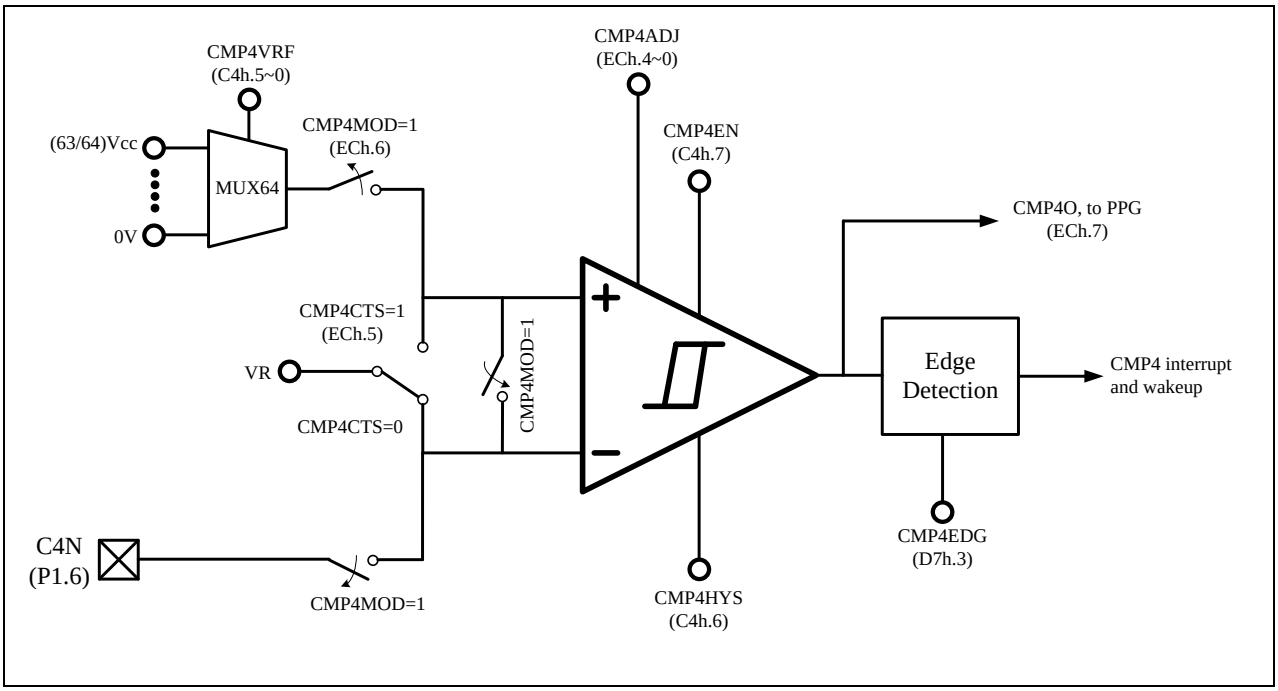
CMP1 Block Diagram



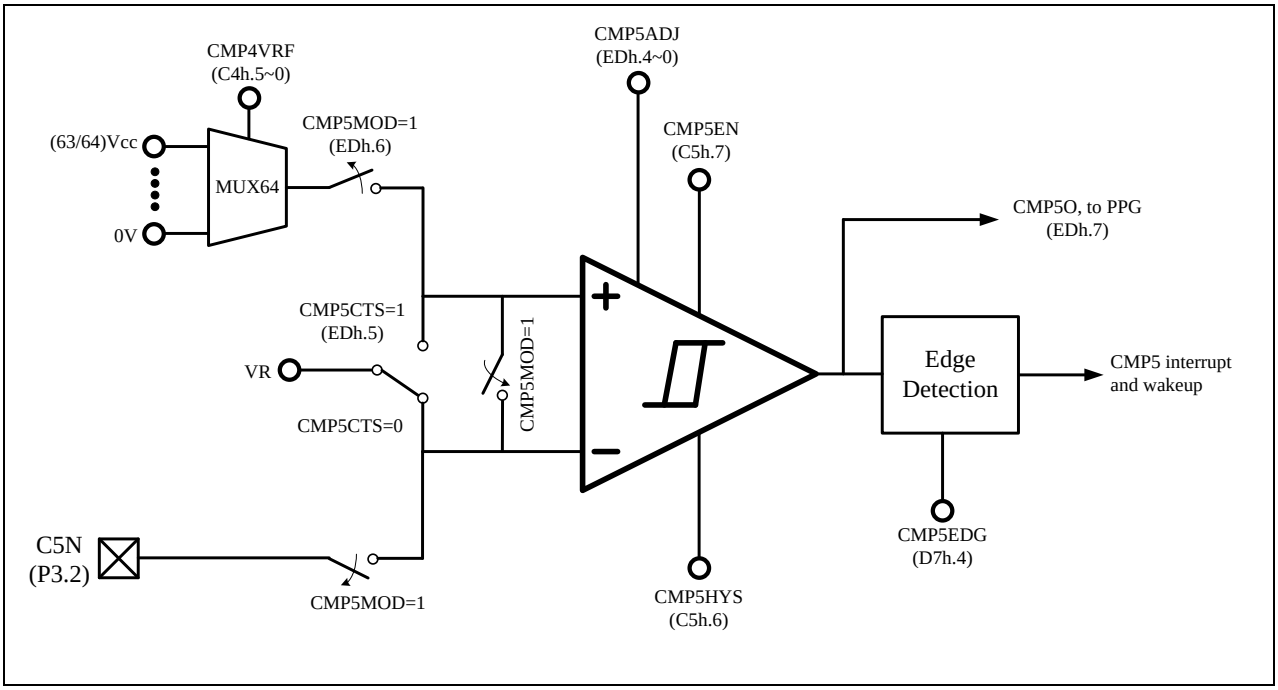
CMP2 Block Diagram



CMP3 Block Diagram



CMP4 Block Diagram



CMP5 Block Diagram

SFR **84h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE2	–	PWM1IE	PWM0IE	CMP5IE	CMP4IE	CMP3IE	CMP2IE	CMP1IE
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	0	0	0	0	0	0	0

84h.4 **CMP5IE:** CMP5 interrupt enable
0: Disable CMP5 interrupt
1: Enable CMP5 interrupt

84h.3 **CMP4IE:** CMP4 interrupt enable
0: Disable CMP4 interrupt
1: Enable CMP4 interrupt

84h.2 **CMP3IE:** CMP3 interrupt enable
0: Disable CMP3 interrupt
1: Enable CMP3 interrupt

84h.1 **CMP2IE:** CMP2 interrupt enable
0: Disable CMP2 interrupt
1: Enable CMP2 interrupt

84h.0 **CMP1IE:** CMP1 interrupt enable
0: Disable CMP1 interrupt
1: Enable CMP1 interrupt

SFR **85h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG2	–	PWM1IF	PWM0IF	CMP5IF	CMP4IF	CMP3IF	CMP2IF	CMP1IF
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	0	0	0	0	0	0	0

85h.4 **CMP5IF:** CMP5 interrupt flag
Set by H/W while CMP5 output rising/falling event occurred.
S/W writes EFh to INTFLG2 to clear this bit.

85h.3 **CMP4IF:** CMP4 interrupt enable
Set by H/W while CMP4 output rising/falling event occurred.
S/W writes F7h to INTFLG2 to clear this bit.

85h.2 **CMP3IF:** CMP3 interrupt enable
Set by H/W while CMP3 output rising/falling event occurred.
S/W writes FBh to INTFLG2 to clear this bit.

85h.1 **CMP2IF:** CMP2 interrupt enable
Set by H/W while CMP2 output rising/falling event occurred.
S/W writes FDh to INTFLG2 to clear this bit.

85h.0 **CMP1IF:** CMP1 interrupt enable
Set by H/W while CMP1 output rising/falling event occurred.
S/W writes FEh to INTFLG2 to clear this bit.

SFR **C1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP1CON	CMP1EN	CMP1HYS	–	SYNDBT				
R/W	R/W	R/W	–	R/W				
Reset	0	0	–	0	0	0	0	0

C1h.7 **CMP1EN:** CMP1 enable
0: CMP1 disable
1: CMP1 enable

C1h.6 **CMP1HYS:** CMP1 hysteresis characteristic enable
0: Disable
1: Enable

SFR **C2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2CON	CMP2EN	CMP2HYS	CMP2VRF					
R/W	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

C2h.7 **CMP2EN:** CMP2 enable
0: CMP2 disable
1: CMP2 enable

C2h.6 **CMP2HYS:** CMP2 hysteresis characteristic enable
0: Disable
1: Enable

C2h.5~0 **CMP2VRF:** CMP2 reference level select
000000~111111: 0V ~ V_{CC}
Reference level = (1/64 * CMP2VRF) * V_{CC}

SFR **C3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP3CON	CMP3EN	CMP3HYS	CMP3VRF					
R/W	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

C3h.7 **CMP3EN:** CMP3 enable
0: CMP3 disable
1: CMP3 enable

C3h.6 **CMP3HYS:** CMP3 hysteresis characteristic enable
0: Disable
1: Enable

C3h.5~0 **CMP3VRF:** CMP3reference level select
000000~111111: 0V ~ V_{CC}
Reference Level = (1/64 * CMP3VRF) * V_{CC}

SFR **C4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP4CON	CMP4EN	CMP4HYS	CMP4VRF					
R/W	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

C4h.7 **CMP4EN:** CMP4 enable
0: CMP4 disable
1: CMP4 enable

C4h.6 **CMP4HYS:** CMP4 hysteresis characteristic enable
0: Disable
1: Enable

C4h.5 **CMP4EDG:** CMP4 interrupt trigger edge select
0: falling edge trigger
1: Rising edge trigger

C4h.5~0 **CMP4VRF:** CMP4 reference level
000000~111111: 0V ~ V_{CC}
Reference level = (1/64 * CMP4VRF) * V_{CC}

SFR **C5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP5CON	CMP5EN	CMP5HYS	CMP5VRF					
R/W	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

C5h.7 **CMP5EN:** CMP5 enable
0: CMP5 disable
1: CMP5 enable

C5h.6 **CMP5HYS:** CMP5 hysteresis characteristic enable
0: Disable
1: Enable

C5h.5~0 **CMP5VRF:** CMP5 reference level
000000~111111: 0V ~ V_{CC}
Reference level = (1/64 * CMP5VRF) * V_{CC}

SFR **D7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIEDG	–	–	–	CMP5EDG	CMP4EDG	CMP3EDG	CMP2EDG	CMP1EDG
R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	0	0	0	0	0

D7h.4 **CMP5EDG:** CMP5 interrupt trigger edge select
0: falling edge trigger
1: Rising edge trigger

D7h.3 **CMP4EDG:** CMP4 interrupt trigger edge select
0: falling edge trigger
1: Rising edge trigger

D7h.2 **CMP3EDG:** CMP3 interrupt trigger edge select
0: falling edge trigger
1: Rising edge trigger

D7h.1 **CMP2EDG:** CMP2 interrupt trigger edge select
0: falling edge trigger
1: Rising edge trigger

D7h.0 **CMP1EDG:** CMP1 interrupt trigger edge select
0: falling edge trigger
1: Rising edge trigger

SFR **E9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP1CAL	CMP1O	CMP1MOD	CMP1CTS	CMP1ADJ				
R/W	R	R/W	R/W	R/W				
Reset	0	0	0	0	1	1	1	1

E9h.7 **CMP1O:** CMP1 output status
0: $V_{IN+} < V_{IN-}$
1: $V_{IN+} > V_{IN-}$

E9h.6 **CMP1MOD:** CMP1 operating mode
0: Normal mode
1: Calibration mode

E9h.5 **CMP1CTS:** CMP1 calibration terminal select
0: Select inverting input
1: Select non-inverting input

E9h.4~0 **CM1ADJ:** CMP1 offset voltage adjust
00000~11111: $-V_{OS\_MAX} \sim +V_{OS\_MAX}$
Offset calibration procedure must be performed to minimize the input offset voltage before use.

SFR **EAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2CAL	CMP2O	CMP2MOD	CMP2CTS	CMP2ADJ				
R/W	R	R/W	R/W	R/W				
Reset	0	0	0	0	1	1	1	1

EAh.7 **CMP2O:** CMP2 output status
0: $V_{IN+} < V_{IN-}$
1: $V_{IN+} > V_{IN-}$

EAh.6 **CMP2MOD:** CMP2 operating mode
0: Normal mode
1: Calibration mode

EAh.5 **CMP2CTS:** CMP2 calibration terminal select
0: Select inverting input
1: Select non-inverting input

EAh.4~0 **CMP2ADJ:** CMP2 offset voltage adjust
00000~11111: $-V_{OS\_MAX} \sim +V_{OS\_MAX}$
Offset calibration procedure must be performed to minimize the input offset voltage before use.

SFR **EBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP3CAL	CMP3O	CMP3MOD	CMP3CTS	CMP3ADJ				
R/W	R	R/W	R/W	R/W				
Reset	0	0	0	0	1	1	1	1

EBh.7 **CMP3O:** CMP3 output status
0: $V_{IN+} < V_{IN-}$
1: $V_{IN+} > V_{IN-}$

EBh.6 **CMP3MOD:** CMP3 operating mode
0: Normal mode
1: Calibration mode

EBh.5 **CMP3CTS:** CMP3 calibration terminal select
0: Select inverting input
1: Select non-inverting input

EBh.4~0 **CMP3ADJ:** CMP3 offset voltage adjust
00000~11111: $-V_{OS\_MAX} \sim +V_{OS\_MAX}$
Offset calibration procedure must be performed to minimize the input offset voltage before use.

SFR **ECh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP4CAL	CMP4O	CMP4MOD	CMP4CTS	CMP4ADJ				
R/W	R	R/W	R/W	R/W				
Reset	0	0	0	0	1	1	1	1

ECh.7 **CMP4O:** CMP4 output status
0: $V_{IN+} < V_{IN-}$
1: $V_{IN+} > V_{IN-}$

ECh.6 **CMP4MOD:** CMP4 operating mode
0: Normal mode
1: Calibration mode

ECh.5 **CMP4CTS:** CMP4 calibration terminal select
0: Select inverting input
1: Select non-inverting input

ECh.4~0 **CMP4ADJ:** CMP4 offset voltage adjust
00000~11111: $-V_{OS\_MAX} \sim +V_{OS\_MAX}$
Offset calibration procedure must be performed to minimize the input offset voltage before use.

SFR **EDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP5CAL	CMP5O	CMP5MOD	CMP5CTS	CMP5ADJ				
R/W	R	R/W	R/W	R/W				
Reset	0	0	0	0	1	1	1	1

EDh.7 **CMP5O:** CMP5 output status
0: $V_{IN+} < V_{IN-}$
1: $V_{IN+} > V_{IN-}$

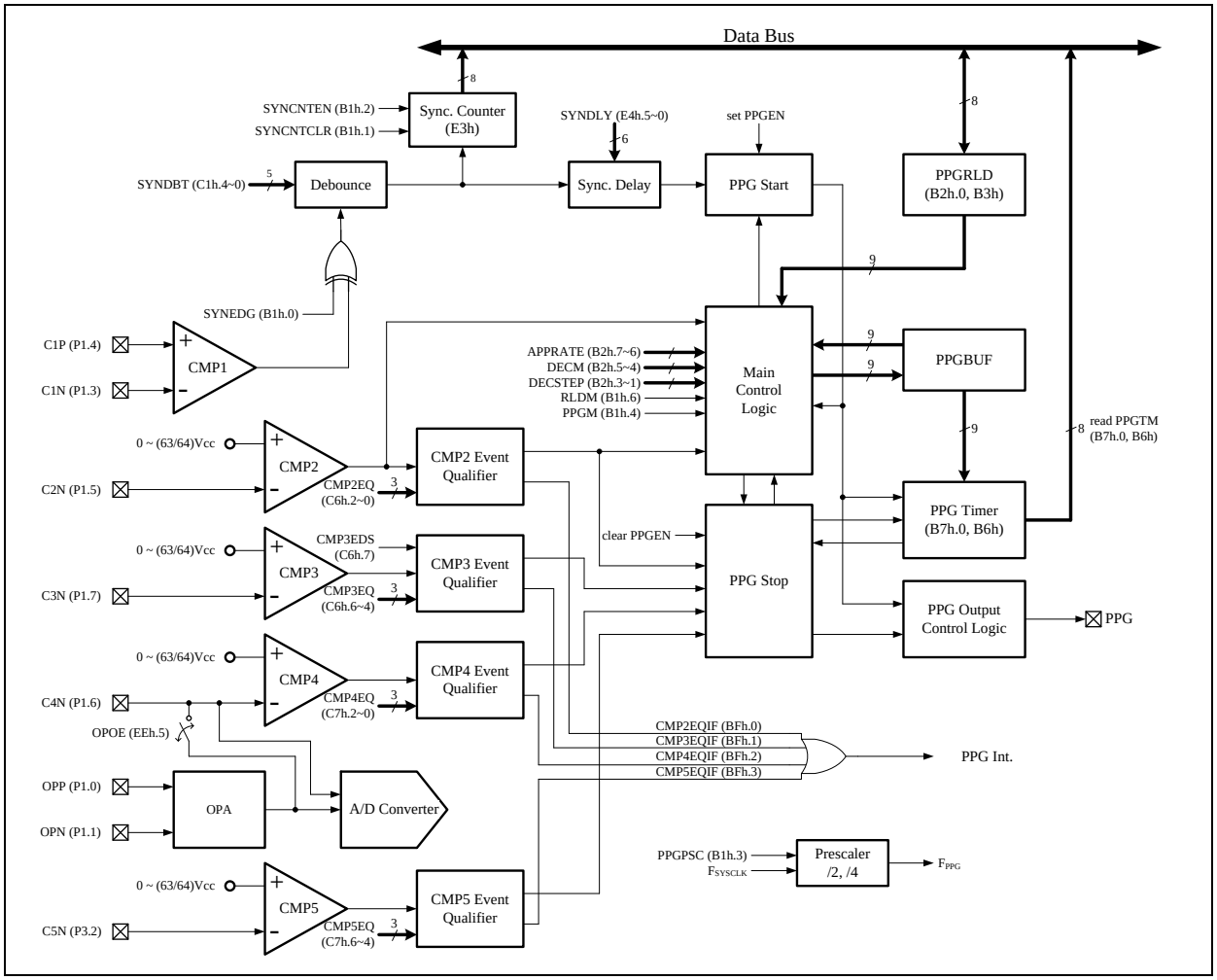
EDh.6 **CMP5MOD:** CMP5 operating mode
0: Normal mode
1: Calibration mode

EDh.5 **CMP5CTS:** CMP5 calibration terminal select
0: Select inverting input
1: Select non-inverting input

EDh.4~0 **CMP5ADJ:** CMP5 offset voltage adjust
00000~11111: $-V_{OS\_MAX} \sim +V_{OS\_MAX}$
Offset calibration procedure must be performed to minimize the input offset voltage before use.

15. Programmable Pulse Generator (PPG)

The Chip provides one 9-bit programmable pulse generator (PPG). PPG functional block diagram is shown as below. The module mainly consists of one 9-bit reloadable PPG timer, five analog comparators CMP1~CMP5, and one operational amplifier. The clock rate F_{PPG} for PPG timer may be one of F_{SYSCLK} divided by 2 and 4, selected by PPGPSC (B1h.3) bit of PPGCON0 register. Time unit T_{PPG} equals the reciprocal of clock frequency F_{PPG}. The input signal of CMP4 inverting input C4N can either come directly from P1.6 pin or driven by the output of on-chip OPA when OPOE (EEh.5) is set. Furthermore, input signal of C4N is also conducted to AD1 channel. See the contents of Analog-to-Digital in Section 11, Operational Amplifier in Section 12 and Analog Comparators in Section 13 for details in settings and operations of ADC, OPA, and CMPx respectively. Two pulsing modes: Single Pulse mode and Synchronous mode are provided for pulse generation. The overall PPG functions and operations are described in following subsections.

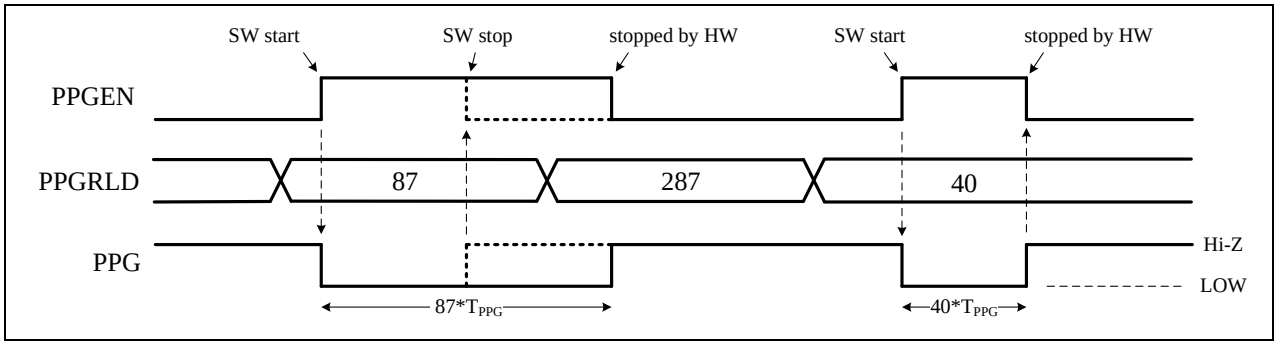


PPG Block Diagram

15.1 Single Pulse Mode

PPG module functions in single pulse mode by programming PPGM (B1h.4) to 0. A single pulse can easily be generated by Software Trigger which is the write 1 operation on PPGEN (B1h.7) bit. The PPG pin state changes from high-impedance (Hi-Z) to logic low. The pulse width to be generated is simply determined by the 9-bit reload buffer PPGRLD composed of PPGRLD8 (B2h.0) bit and 8-bit PPGRLDL (B3h.7~0) register. The pulse length is calculated as (PPGRLD * T_{PPG}). When PPGEN is at 0, updating PPGRLD also synchronously updates working buffer PPGBUF of PPG timer. Write 1 to PPGEN makes

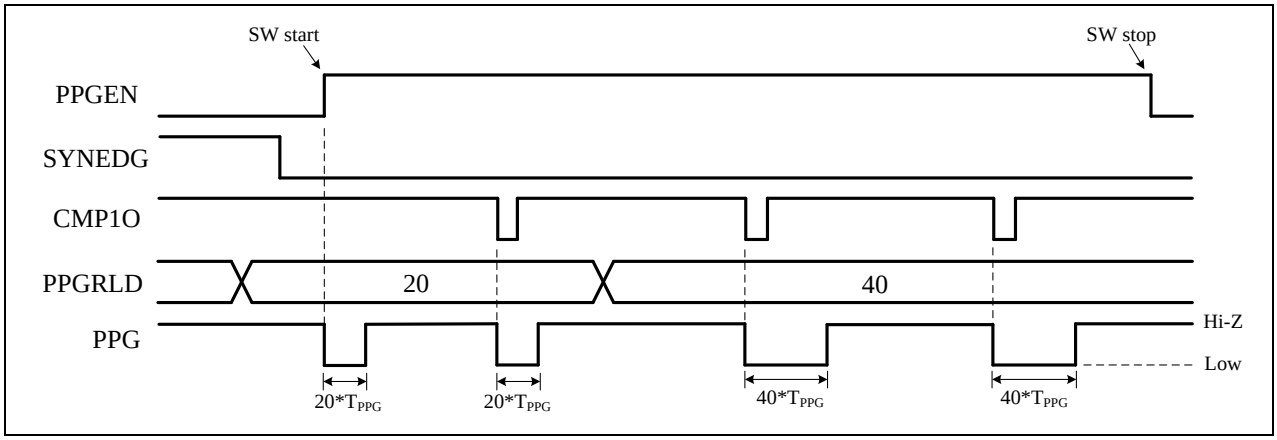
9-bit PPGBUF data be loaded onto PPG timer and PPG module starts pulsing. PPGEN bit keeps activation during the time interval of PPG pulsing till PPG timer times up, then PPGEN bit will be cleared by hardware and PPG will return from low to Hi-Z state. A single pulse generation is complete. Note that zero PPGRLD value makes PPG module keep silent even thought we can further do bit set operations on PPGEN bit which will also not be set exactly at all. That means no pulse shall be generated with zero PPGRLD value. Updating PPGRLD data during PPG pulsing does not affect the current pulsing in progress. The newly updated PPGRLD data will be applied to later issued generations after end of current pulsing.



Single pulse mode

15.2 Synchronous Mode

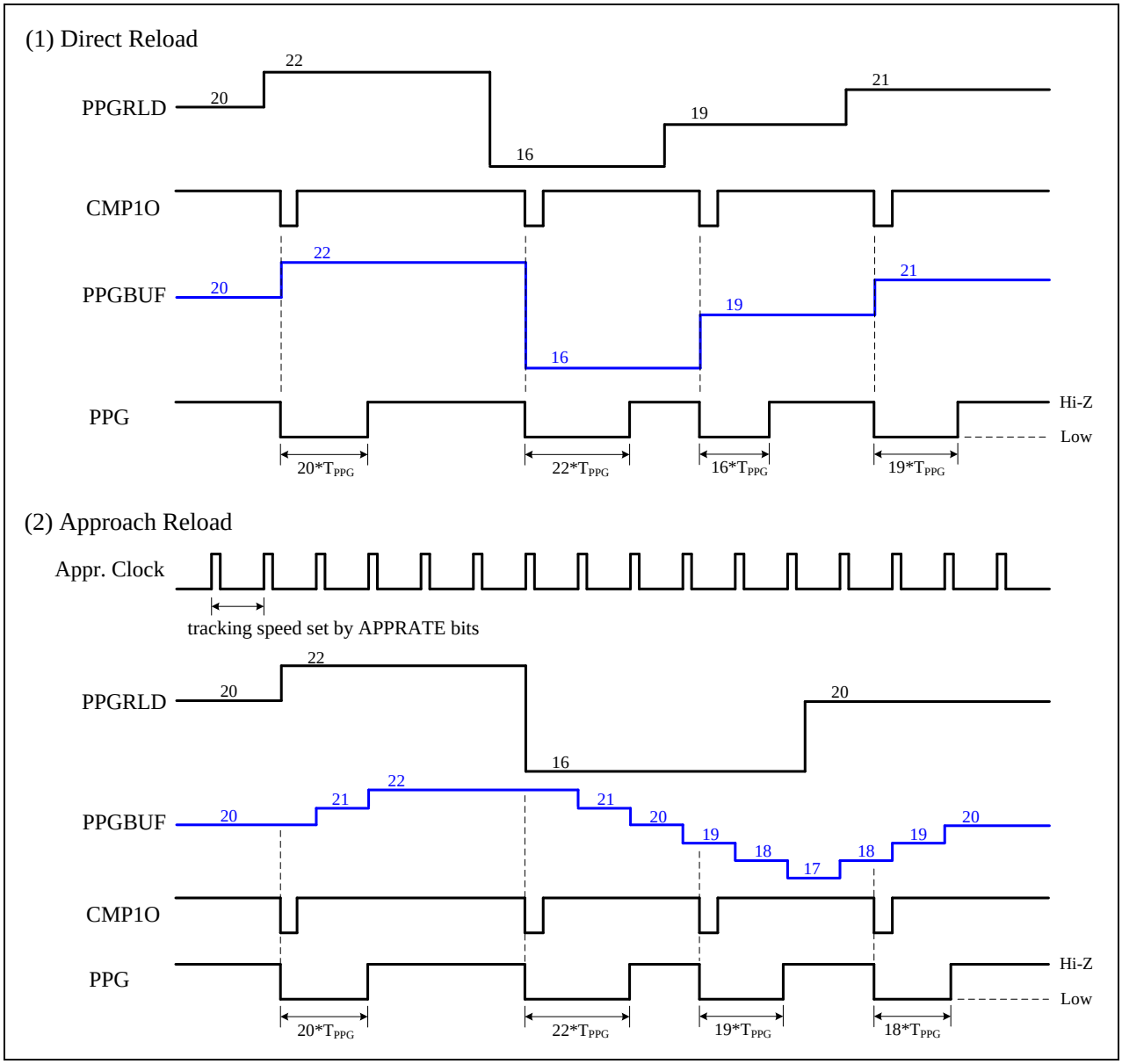
Synchronous mode is the mode the PPG pulsing responds to CMP1 output trigger event. PPG module functions in synchronous mode by programming PPGM (B1h.4) to 0. Setting the PPGEN bit from low to high generates a single pulse at first. After that the PPG module pulse generations synchronizes with each CMP1 trigger event. User can assign the trigger edge as the synchronous event by programming SYNEDG (B1h.0) bit of PPGCON0 register. Setting SYNEDG to 0 is for falling-edge trigger while setting SYNEDG to 1 is for rising-edge trigger. The figure shown below illustrates the basic operation of synchronous mode for the case of falling-edge trigger. PPG synchronous pulsing can be stop at any time by clearing the PPGEN bit.



Synchronous mode

The length of generated pulse can be controlled by the 9-bit PPGRLD register, which matches the data length with PPG timer register. Pulse length is calculated as (PPGRLD * T_{PPG}). PPG module supports two reload strategies; direct reload and approach reload, which can be selected by programming the RLDM (B1h.6) bit of PPGCON0, for loading the initial value of PPG timer. For direct reload the working reload buffer PPGBUF only can be updated at the moment of occurrence of valid synchronous event, means that the newly updated PPGRLD value will not be applied to the current pulsing in progress until the next trigger. The other reload strategy is that PPGBUF always traces the newest value of

PPGRLD gradually at a rate with cycle time [512*(1+APPRATE)*T_{PPG}] till it reaches the target. Once it captures the target, its value hold unchanged unless PPGRLD is changed again. Two-bit register APPRATE is located on bit7~6 of PPGCON1 (B2h) register. The figure below shows the operations of two reload modes. Notice that these two reload strategies described above are only available for synchronous mode.



Operations of direct and approach reloads

15.3 Comparator Events

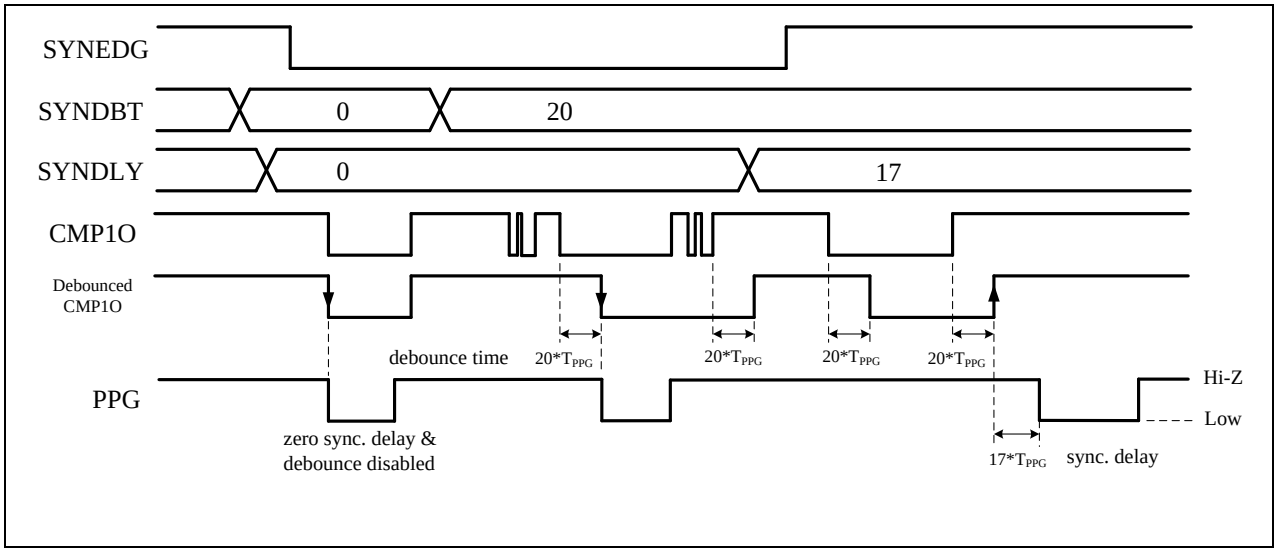
There are five build-in analog comparators CMP1~CMP5 applicable for synchronization detection, device over-voltage detection, power over-voltage detection, and over-current detection. Each of them is described in following subsections.

15.3.1 CMP1: Synchronization Detection

Synchronous comparator is provided to detect synchronous trigger events, which can be rising-edge or falling-edge event of CMP1 output transition selected by SYNEDG (B1h.0) bit of PPGCON0 register.

Setting SYNEDG=0/1 is for rising-edge/falling-edge trigger respectively. PPG module generates a pulse for each valid synchronous event.

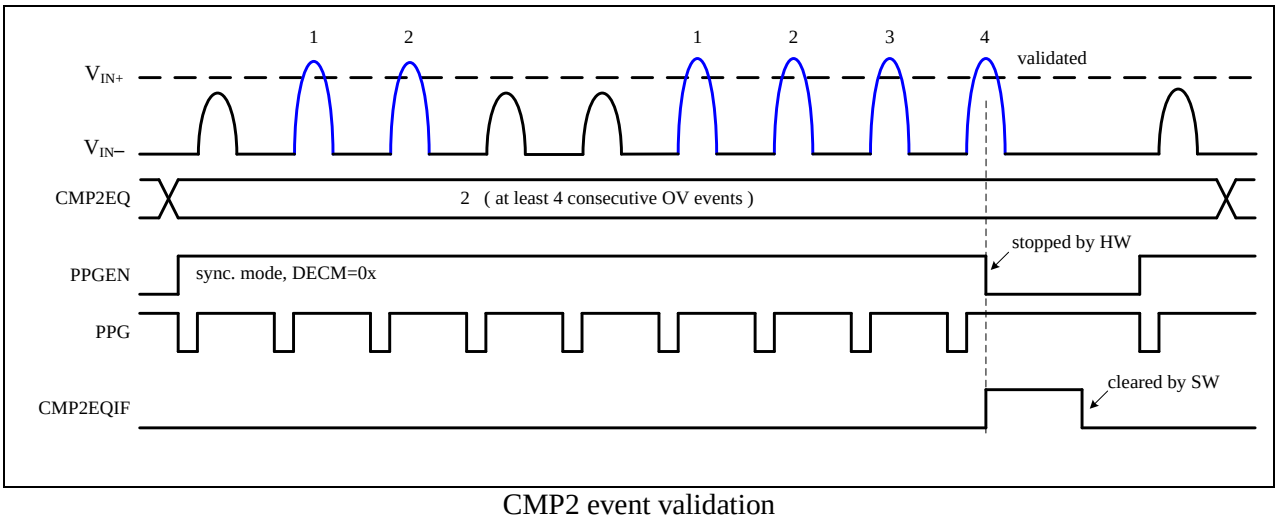
The output of CMP1 first passes through de-bounce circuit to prevent unexpected trigger happened. De-bounce time is in the range 0~31*T_{PPG} configured by setting SYNDBT (C1h.4~0) bits of CMP1CON register. Synchronous event can be delayed for a period of time before allowing PPG pulsing. The delay time is in the range 0~63*T_{PPG} configured by setting SYNDLY (E4h.5~0) register. By default the de-bounce function is disabled after any reset event. Programming a nonzero SYNDBT value automatically enables the function of de-bounce circuit.



De-bounce function and synchronous trigger delay

Synchronous events can also be counted by synchronous event counter. The counter increases by 1 every valid synchronous event. The counter can be enabled by writing 1 to SYNCNTEN (B1h.2) bit of PPGCON0 register. The maximum counter value is 128. Counter value can be obtained by reading SYNCNT (E3h) register. Counter value can also be cleared by writing 1 to SYNCNTCLR (B1h.0) bit.

15.3.2 CMP2: Device Over-Voltage Detection



CMP2 event validation

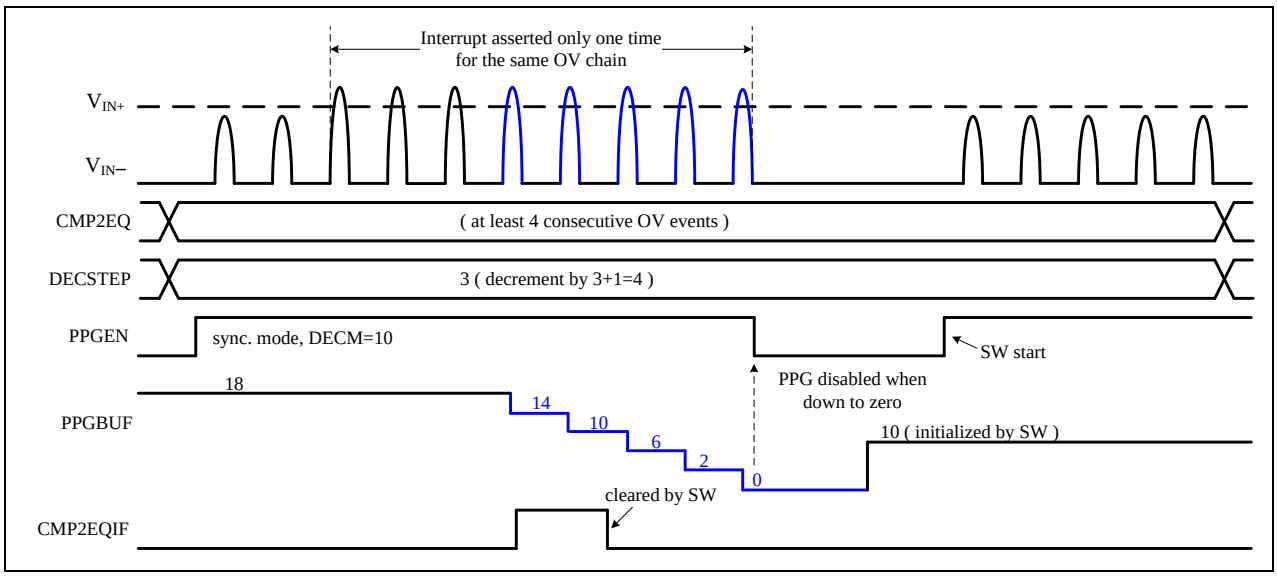
The build-in CMP2 is a component used to check whether the voltage on off-chip power device stressed over a specified level. A validated CMP2 event must meet at least a specific count of consecutive fallings detected on CMP2 output. The criteria of event validation could be one of 1, 2, 4, 8, 16, 32, 64, and 128

consecutive events selected by programming CMP2EQ (C6h.2~0) register.

If consecutive falling edges of CMP2 output reached user specified count, PPG module is either stopped by hardware cleared PPGEN (B1h.7) bit or decreases the length to be pulsed automatically for next coming synchronous triggers, which can be determined by DECM (B2h.5~4) bits of PPGCON1 register. In case of event validation the CMP2EQIF (BFh.0) flag will be asserted regardless of DECM settings. PPG interrupt service routine (ISR) will also be executed if PPG interrupt is enabled by setting PPGDIE (A9h.5) bit to 1. PPG module only can be resumed again by setting PPGEN bit when flags CMP2EQIF (BFh.0) at DECM=0x, CMP3EQIF (BFh.1), CMP4EQIF (BFh.2) and CMP5EQIF (BFh.3) all are cleared.

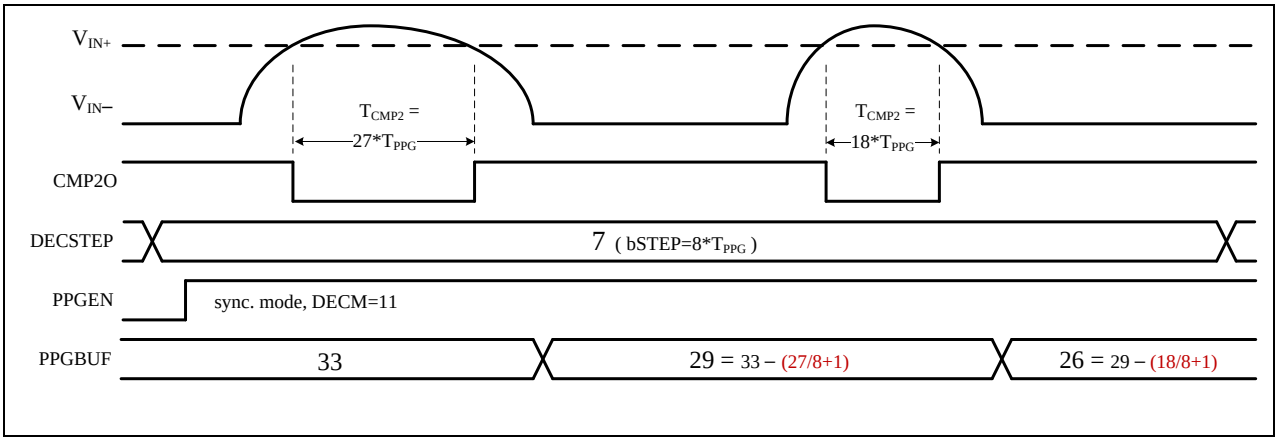
Now we further introduce to the scheme of pulse length auto-decrement. Instead of disabling PPG module when qualified event happened, PPGBUF could be decreased by main control logic to reduce driving power for both power component protection and consideration of industrial safety if DECM bits are programmed to 10 or 11. DECM=10/11 are for constant step decrement and variable step decrement respectively.

For the case of DECM=10, PPGBUF decreases its value with a constant step configured by DECSTEP (B2h.3~1) bits of PPGCTL1 register every validated event. The step size is (DECSTEP+1). PPG module is going to be disabled by hardware automatically if the value of PPGBUF goes further down to zero due to tail-chaining OV events after validation. Before the stillness of current validation the CMP2EQIF (BFh.0) is asserted only one time even if it will be cleared soon by software. It means that tailing-chaining OV evens do not lead to the second assertion of CMP2EQIF. The figure below illustrates the operation of constant step decrement.



Constant step decrement

If DECM is programmed to 11, variable step decrement is selected. Step size directly depends on the duration of CMP2 output low. The step size equation is going to be [1+ (T_{CMP2} / (bSTEP*T_{PPG}))]; where bSTEP is one of 8, 16, 32, and 64 selected by writing DECSTEP (B2h.3~1) bits of PPGCON1 register and T_{CMP2} is the length of CMP2 low pulse. Greater value of DECSTEP induces larger step size for a timed T_{CMP2}. However, the maximum step size will be limited to 15 for any T_{CMP2} which makes the calculated results greater than 15. The operation of variable step decrement is illustrated as below.



Variable step decrement

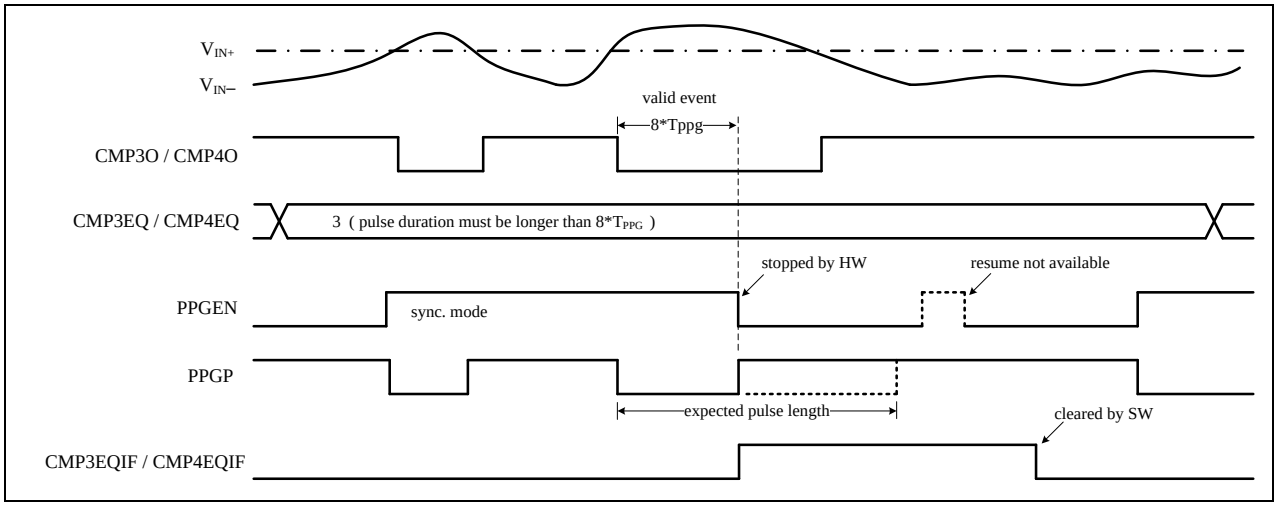
15.3.3 CMP3: Power Over-Voltage Detection

The build-in CMP3 is a component used to check whether the voltage of power line sourced over a specified level. A valid CMP3 event must at least satisfy the minimum LOW time criteria of CMP3 output, which is one of 1, 2, 4, 8, 16, 32, 64, and 128*T_{PPG} selected by programming CMP3EQ (C6h.6~4) bits of CMP23EQ register.

In addition to the validation criteria, user can also determine when a CMP3 event is detected and qualified. If CMP3EDS (C6h.7) bit is 1, an event is only qualified in duration of PPG pulsing. Otherwise CMP3EDS bit is 0, detections are performed at any time even if the PPG module is disabled (PPGEN=0).

If an over-voltage event is qualified as valid, PPGEN bit will be cleared and disabled the PPG module immediately regardless of PPG being pulsing or not. In addition the CMP3EQIF (BFh.1) flag will be asserted at that time. PPG interrupt service routine (ISR) will also be executed if PPG interrupt is enabled by programming PPGDIE (A9h.5) bit to 1. PPG module can be resumed by setting PPGEN bit only when flags CMP2EQIF (BFh.0) at DECM=0x, CMP3EQIF (BFh.1), CMP4EQIF (BFh.2) and CMP5EQIF (BFh.3) all are cleared.

15.3.4 CMP4: Over-Current Detection



CMP3/CMP4 event validation

The build-in CMP4 is a component used to check whether the amount of sensed current sourced or sank over a specified level. A valid CMP4 event must at least satisfy the minimum LOW time criteria of

CMP4 output, which is one of 1, 2, 4, 8, 16, 32, 64, and 128*T_{PPG} selected by programming CMP4EQ (C7h.2~0) bits of CMP45EQ register.

If an over-current event is qualified as valid, PPGEN bit will be cleared and disabled the PPG module immediately regardless of PPG being pulsing or not. In addition the CMP4EQIF (BFh.2) flag will be asserted at that time. PPG interrupt service routine (ISR) will also be executed if PPG interrupt is enabled by programming PPGDIE (A9h.5) bit to 1. PPG module can be resumed by setting PPGEN bit only when flags CMP2EQIF (BFh.0) at DECM=0x, CMP3EQIF (BFh.1), CMP4EQIF (BFh.2) and CMP5EQIF (BFh.3) all are cleared.

15.3.5 CMP5: Over-Current Detection

The build-in CMP5 is similar with the CMP4. A valid CMP5 event must at least satisfy the minimum LOW time criteria of CMP5 output, which is one of 1, 2, 4, 8, 16, 32, 64, and 128*T_{PPG} selected by programming CMP5EQ (C7h.6~4) bits of CMP45EQ register.

If an over-current event is qualified as valid, PPGEN bit will be cleared and disabled the PPG module immediately regardless of PPG being pulsing or not. In addition the CMP5EQIF (BFh.3) flag will be asserted at that time. PPG interrupt service routine (ISR) will also be executed if PPG interrupt is enabled by programming PPGDIE (A9h.5) bit to 1. PPG module can be resumed by setting PPGEN bit only when flags CMP2EQIF (BFh.0) at DECM=0x, CMP3EQIF (BFh.1), CMP4EQIF (BFh.2) and CMP5EQIF (BFh.3) all are cleared.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	CMPIE	PPGDIE	I2CIE	ADIE	EX2	P1IE	TM3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.5 **PPGDIE:** PPG/PPD interrupt enable
0: Disable PPG/PPD interrupt
1: Enable PPG/PPD interrupt

SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PPGCON0	PPGEN	RLDM	–	PPGM	PPGPSC	SYNCNTEN	SYNCNTCLR	SYNEDG
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W
Reset	0	0	–	0	0	0	0	0

B1h.7 **PPGEN:** PPG enable
0: PPG disable
1: PPG enable

B1h.6 **RLDM:** PPG reload mode
0: Direct reload, working buffer synchronizes with reload buffer
1: Approach reload, working buffer approach to reload buffer gradually at certain rate

B1h.4 **PPGM:** PPG output mode
0: Single Pulse mode
1: Synchronous mode

B1h.3 **PPGPSC:** PPG clock source prescaler
0: $F_{SYSCLK}/2$
1: $F_{SYSCLK}/4$

B1h.2 **SYNCNTEN:** CMP1 synchronous event counter enable
0: Disable
1: Enable

B1h.1 **SYNCNTCLR:** CMP1 synchronous event counter clear
Write 1 to this bit to clear synchronous event counter. Automatically cleared by H/W.

B1h.0 **SYNEDG:** CMP1 synchronous event trigger edge select
0: Falling-edge trigger
1: Rising-edge trigger

SFR **B2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PPGCON1	APPRATE		DECM		DECSTEP			PPGRLD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B2h.7~6 **APPRATE:** PPG reload buffer approach rate
00: every 512*T_{PPG} increase/decrease by 1
01: every 1024*T_{PPG} increase/decrease by 1
10: every 2048*T_{PPG} increase/decrease by 1
11: every 4096*T_{PPG} increase/decrease by 1

B2h.5~4 **DECM:** PPG pulse width decrement mode
0x: No decrement but clear PPGEN and stop PPG output when CMP2 event trigger
10: Constant step
11: Variable step

B2h.3~1 **DECSTEP:** PPG pulse width decrement step
Constant step mode
000~111: decrease by 1~8
Variable step mode, decrease by [1+(T_{CMP2}/(T_{PPG}*bSTEP))];
where T_{CMP2} is low time of CMP2 output timed in T_{PPG}
000~011: bSTEP=64, 32, 16, 8
100~111: bSTEP=8

B2h.0 **PPGRLD8:** The MSB (bit[8]) of PPG reload buffer

SFR **B3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PPGRLDL	PPGRLDL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B3h.7~0 **PPGRLDL:** Low-byte of PPG reload buffer (PPGRLD[7:0])
PPG output pulse width is PPGRLD[8:0] * T_{PPG}

SFR **B6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PPGTML	PPGTML							
R/W	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

B6h.7~0 **PPGTML:** Low-bye of 9-bit PPG pulse generation timer

SFR **B7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PPGTMH	–	–	–	–	–	–	–	PPGTMH
R/W	–	–	–	–	–	–	–	R
Reset	–	–	–	–	–	–	–	0

B7h.0 **PPGTMH:** MSB (bit[8]) of 9-bit PPG pulse generation timer

SFR **BFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPEQI	CMP5EQIE	CMP4EQIE	CMP3EQIE	CMP2EQIE	CMP5EQIF	CMP4EQIF	CMP3EQIF	CMP2EQIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

BFh.7 **CMP5EQIE:** CMP5 qualified event interrupt enable
0: Disable
1: Enable

BFh.6 **CMP4EQIE:** CMP4 qualified event interrupt enable
0: Disable
1: Enable

BFh.5 **CMP3EQIE:** CMP3 qualified event interrupt enable
0: Disable
1: Enable

BFh.4 **CMP2EQIE:** CMP2 qualified event interrupt enable
0: Disable
1: Enable

BFh.3 **CMP5EQIF:** CMP5 qualified event interrupt flag
This bit is set by H/W while CMP5 qualified event occurred, write 0 to this bit will clear this flag

BFh.2 **CMP4EQIF:** CMP4 qualified event interrupt flag
This bit is set by H/W while CMP4 qualified event occurred, write 0 to this bit will clear this flag

BFh.1 **CMP3EQIF:** CMP3 qualified event interrupt flag
This bit is set by H/W while CMP3 qualified event occurred, write 0 to this bit will clear this flag

BFh.0 **CMP2EQIF:** CMP2 qualified event interrupt flag
This bit is set by H/W while CMP2 qualified event occurred, write 0 to this bit will clear this flag

SFR **C1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP1CON	CMP1EN	CMP1HYS	CMP1EDG	SYNDBT				
R/W	R/W	R/W	R/W	R/W				
Reset	0	0	0	0	0	0	0	0

C1h.4~0 **SYNDBT:** PPG synchronous mode CMP1 output de-bounce time
De-bounce time = SYNDBT *T_{PPG}
If SYNDBT=0, CMP1 output is directly bypassed to the output of de-bounce circuit.

SFR **C6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP23EQ	CMP3EDS	CMP3EQ			–	CMP2EQ		
R/W	R/W	R/W	R/W	R/W	–	R/W	R/W	R/W
Reset	0	1	1	1	–	1	1	1

C6h.7 **CMP3EDS:** CMP3 event detect select
0: Always detect
1: Detect during PPG output is active

C6h.6~4 **CMP3EQ:** CMP3 output low event qualify
000~111: 1, 2, 4, 8, 16, 32, 64, 128*T_{PPG}

C6h.2~0 **CMP2EQ:** CMP2 output event qualify
000~111: 1, 2, 4, 8, 16, 32, 64, 128 consecutive falling events

SFR **C7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP45EQ	–	CMP5EQ			–	CMP4EQ		
R/W	–	R/W	R/W	R/W	–	R/W	R/W	R/W
Reset	–	1	1	1	–	1	1	1

C7h.6~4 **CMP5EQ:** CMP5 output low event qualify
000~111: 1, 2, 4, 8, 16, 32, 64, 128*T_{PPG}

C7h.2~0 **CMP4EQ:** CMP4 output low event qualify
000~111: 1, 2, 4, 8, 16, 32, 64, 128*T_{PPG}

SFR **E3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNCNT	SYNCNT							
R/W	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

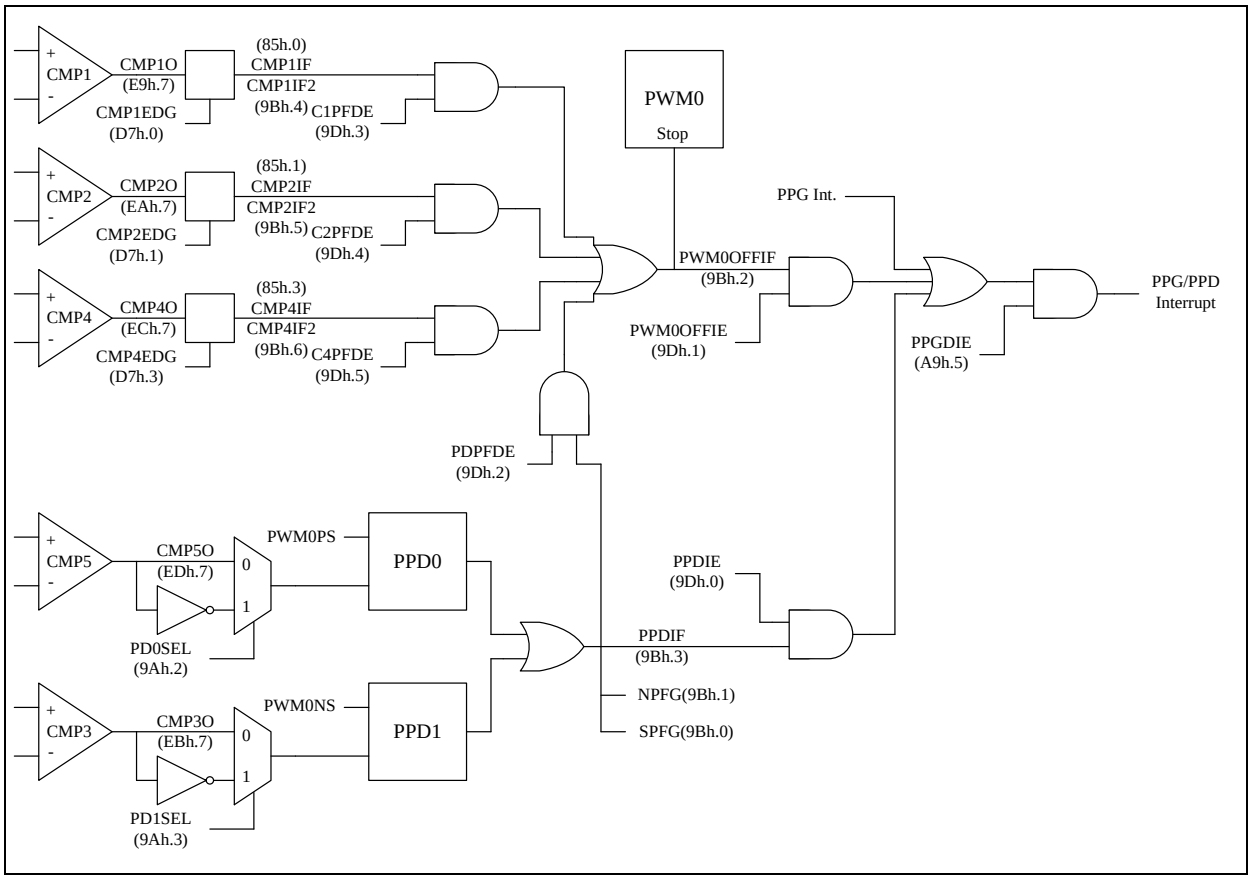
E3h.7~0 **SYNCNT:** Synchronous event counter
Bit7 of SYNCNT denotes
0: not overflow, counter runs
1: counter overflow, counter stop and hold
This register can be cleared by writing SYNCNTCLR bit (B1h.1) of PPGCON0.

SFR **E4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNDLY	–	–	SYNDLY					
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

E4h.5~0 **SYNDLY:** PPG output delay time
The PPG output delay time is calculated as following equation
Delay time = SYNDLY * T_{PPG}

16. Phase Protect Detector (PPD)

The Chip provides Phase Protect Detector (PPD). PPD functional block diagram is shown as below. The module mainly consists of two phase detectors and five analog comparators CMP1~CMP5. Each phase detector needs one PWM output and one CMP output as its input signals. Phase detector 0 uses PWM0PS and CMP5 as its inputs, and phase detector 1 uses PWM0NS and CMP3 as its inputs. The PWM0PS and PWM0NS is PWM0 Mode 0 output data in half-bridge mode. The CMP5 and CMP3 can select positive or negative output by setting PD0SEL (9Ah.2) and PD1SEL (9Ah.3) bits respectively. The functions of CMP1, CMP2, and CMP4 are the same as their functions in PPG module. The overall PPD functions and operations are described in following subsections.



16.1 Phase Detector

The phase detector detects the phase width form PWM input rising edge to CMP input rising edge. The PPDTH (9Ch) denotes the phase width threshold. When the phase width is smaller than the PPDTH setting value, the SPFG (9Bh.0) bit will be set. When the phase width is equal to zero, the NPFG (9Bh.1) bit will be set. The PPDIF (9Bh.3) will be set when SPFG bit or NPFG bit is set.

16.2 CMP

To avoid the damage the application circuit, CMP1, CMP2, and CMP4 also can force PWM0 turned off to protect the circuit. By setting C1PFDE (9Dh.3), C2PFDE (9Dh.4), and C4PFDE (9Dh.5) bits to enable CMP force PWM0 turned off function. The CMP1IF2 (9Bh.4), CMP2IF2 (9Bh.5), and CMP4IF2 (9Bh.6) bits are copied from SFR 85h, S/W can quick check the interrupt source while the PPD interrupt event occur.

16.3 PWM0 Force OFF

When PWM0OFFIF bit is set by H/W, the PWM0 will be force turned off and the CLRPWM0 bit will be set. After check and remove all problems, clear CLRPWM0 bit will restart phase detector.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	CMPIE	PPGDIE	I2CIE	ADIE	EX2	P1IE	TM3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.5 **PPGDIE:** PPG/PPD interrupt enable
0: Disable PPG/PPD interrupt
1: Enable PPG/PPD interrupt

SFR **9Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PPDCON	–	PPDENS			PD1SEL	PD0SEL	–	PPDEN
R/W	–	R/W	R/W	R/W	R/W	R/W	–	R/W
Reset	–	0	0	0	0	0	–	0

9Ah.6~4 **PPDENS:** Phase detector enable select
000: after CLRPWM0 bit changes to 0, do not wait before start detect
001: after CLRPWM0 bit changes to 0, wait 1 PWM period before start detect
010: after CLRPWM0 bit changes to 0, wait 2 PWM periods before start detect
011: after CLRPWM0 bit changes to 0, wait 3 PWM periods before start detect
100: after CLRPWM0 bit changes to 0, wait 4 PWM periods before start detect
101: after CLRPWM0 bit changes to 0, wait 5 PWM periods before start detect
110: after CLRPWM0 bit changes to 0, wait 6 PWM periods before start detect
111: after CLRPWM0 bit changes to 0, wait 7 PWM periods before start detect

9Ah.3 **PD1SEL:** Phase detector 0 input source select
0: CMP3
1: ~CMP3

9Ah.2 **PD0SEL:** Phase detector 1 input source select
0: CMP5
1: ~CMP5

9Ah.0 **PPDEN:** PPD enable
0: PPD disable
1: PPD enable

SFR **9Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PPDSTA	–	CMP4IF2	CMP2IF2	CMP1IF2	PPDIF	PWM0OFFIF	NPGF	SPGF
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	0	0	0	0	0	0	0

9Bh.6 **CMP4IF2:** CMP4 interrupt flag
This bit is same as the bit CMP4IF (85h.3).
Set by H/W while CMP4 output rising/falling event occurred.
S/W writes BFh to PPDSTA to clear this bit.

9Bh.5 **CMP2IF2:** CMP2 interrupt flag
This bit is same as the bit CMP2IF (85h.1).
Set by H/W while CMP2 output rising/falling event occurred.
S/W writes DFh to PPDSTA to clear this bit.

9Bh.4 **CMP1IF2:** CMP1 interrupt flag
This bit is same as the bit CMP1IF (85h.0).
Set by H/W while CMP1 output rising/falling event occurred.
S/W writes EFh to PPDSTA to clear this bit.

9Bh.3 **PPDIF:** PPD interrupt flag
Set by H/W while NPGF=1 or SPGF=1.
S/W writes F7h to PPDSTA to clear this bit.

9Bh.2 **PWM0OFFIF:** PWM0 turned off by PPD interrupt flag
0: PWM0 not turned off by PPD

1: PWM0 has been turned off by PPD
Set by H/W, S/W writes FBh to PPDSTA to clear this bit.

9Bh.1 **NPGF:** No phase interrupt flag
0: Phase width is detected
1: No phase width is detected
Set by H/W, S/W writes FDh to PPDSTA to clear this bit.

9Bh.0 **SPGF:** Small phase interrupt flag
0: Phase width ≥ PPDTH
1: Phase width < PPDTH
Set by H/W, S/W writes FEh to PPDSTA to clear this bit.

SFR **9Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PPDTH	PPDTH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

9Ch.7~0 **PPDTH:** PPD threshold

SFR **9Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PPDIE	–	–	C4PFDE	C2PFDE	C1PFDE	PDPFDE	PWM0OFFIE	PPDIE
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

9Dh.5 **C4PFDE:** CMP4 PWM0 force off enable
0: CMP4 PWM0 force off disable
1: CMP4 PWM0 force off enable

9Dh.4 **C2PFDE:** CMP2 PWM0 force off enable
0: CMP2 PWM0 force off disable
1: CMP2 PWM0 force off enable

9Dh.3 **C1PFDE:** CMP1 PWM0 force off enable
0: CMP1 PWM0 force off disable
1: CMP1 PWM0 force off enable

9Dh.2 **PDPFDE:** Phase detect PWM0 force off enable
0: Phase detect PWM0 force off disable
1: Phase detect PWM0 force off enable

9Dh.1 **PWM0OFFIE:** PWM0 turned off by PPD interrupt enable
0: PWM0 turned off by PPD interrupt disable
1: PWM0 turned off by PPD interrupt enable

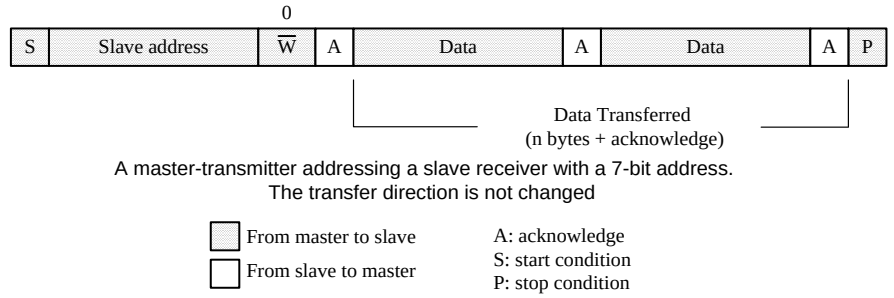
9Dh.0 **PPDIE:** PPD interrupt enable
0: PPD interrupt disable
1: PPD interrupt enable

17. Master I²C Interface

Master I²C interface Transmission mode:

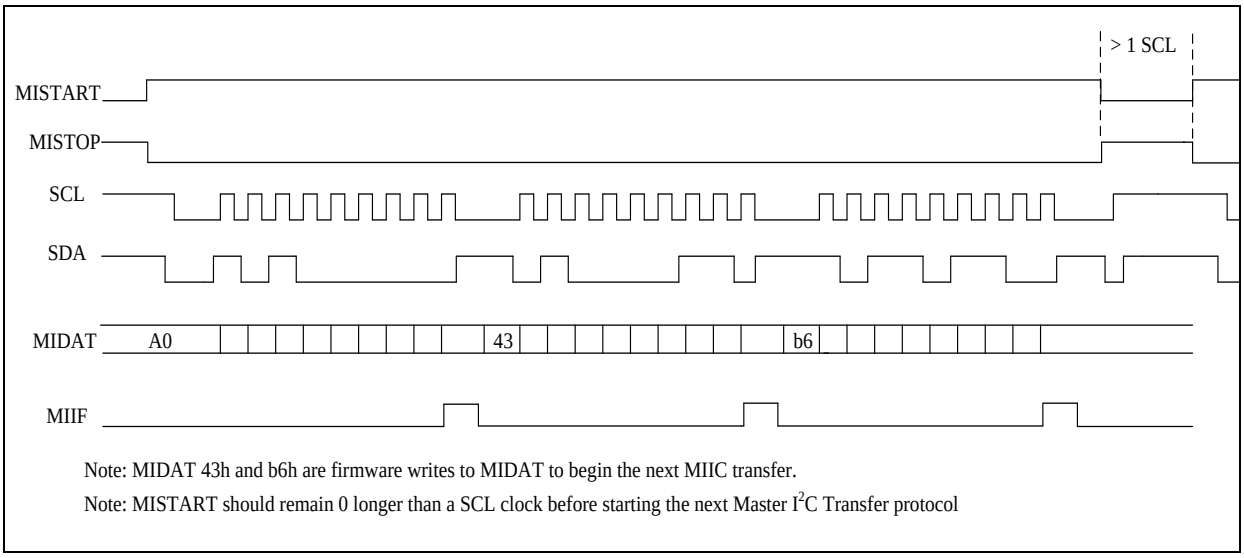
At the beginning write slave address and direction bit to MIDAT and set MISTART. After the START condition (MISTART), the 7 bits slave address and one bit direction bit are sent. When MIIF convert to 1, address and direction bit transmission was complete. After sending the address and direction bit, user should clear MIIF and write MIDAT to start first data transmission. When MIIF convert to 1, data transfer to slave was complete. User can write MIDAT again to transfer next data to slave. Set MISTOP to finish transmission mode.

MISTART must remain at 1 for the next transfer. After final data transmit/receive, set MISTOP to finish transmit/receive protocol. MISTART should remain 0 longer than a SCL clock before starting the next Master I^{2}C protocol. SCL clock can be adjusted via MICR.



Master I²C Transmit flow:

(1) Write slave address and direction bit to MIDAT
(2) Clear MISTOP and set MISTART to start I²C transmission
(3) Wait until MIIF convert to 1 (interrupt will be issued according to the user's request) and Clear MIIF
(4) Write data to MIDAT to start next transfer (MISTART must remain at 1)
(5) Wait until MIIF convert to 1 (interrupt will be issued according to the user's request) and Clear MIIF, Loop (4) ~ (5) for next transfer.
(6) Clear MISTART and set MISTOP to stop the I²C transfer



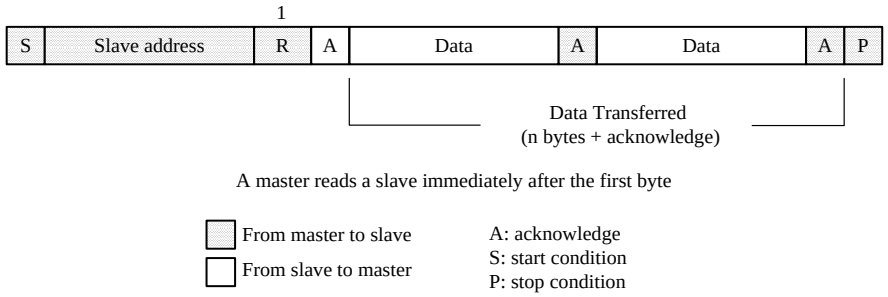
Master Transmit Timing

Note: MISTART should remain 0 longer than a SCL period before starting the next Master I^{2}C protocol.

Master I²C interface Receive mode:

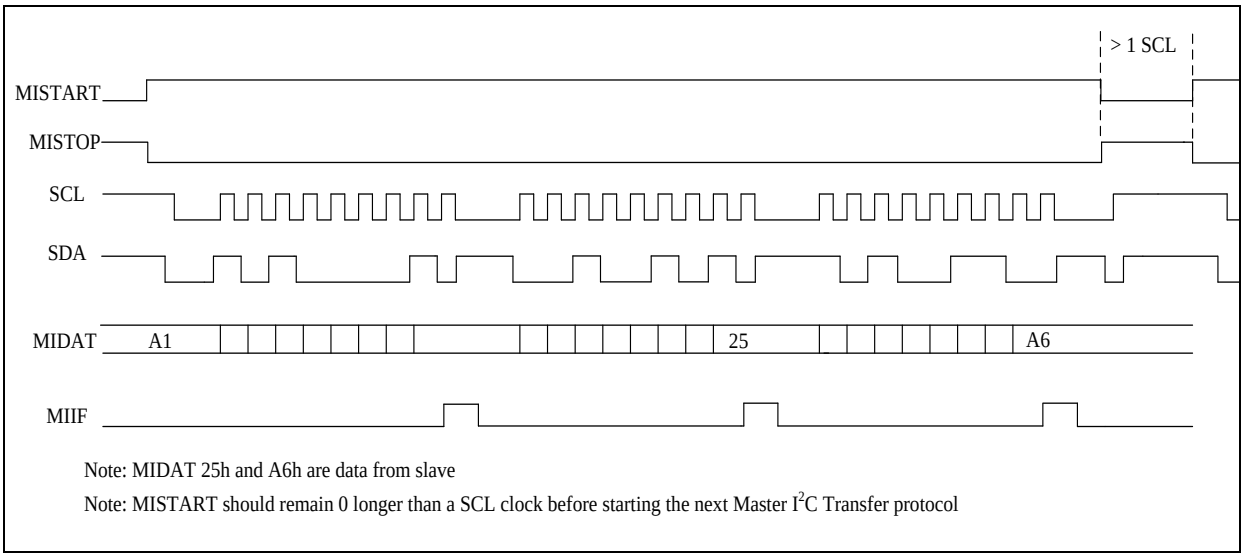
At the beginning write slave address and direction bit to MIDAT and set MISTART. After the START condition (MISTART), the 7 bits slave address and one bit direction bit are sent. When MIIF convert to 1, address and direction bit transmission was complete. After sending the address and direction bit, user should clear MIIF and read MIDAT to start first receive data (The first reading of MIDAT does not represent the data returned by the slave). When MIIF convert to 1, data receive from slave was complete. User can read MIDAT to get data from slave, and start next receive. Set MISTOP to finish receive mode.

MISTART must remain at 1 for the next transfer. After final data transmit/receive, set MISTOP to finish transmit/receive protocol. MISTART should remain 0 longer than a SCL clock before starting the next Master I^{2}C protocol. SCL clock can be adjusted via MICR.



Master I²C Receive flow:

(1) Write slave address and direction bit to MIDAT
(2) Clear MISTOP and set MISTART to start I²C transmission
(3) Wait until MIIF convert to 1 (interrupt will be issued according to the user's request) and Clear MIIF
(4) Read data from MIDAT to start first receive data (The first reading of MIDAT does not represent the data returned by the slave)
(5) Wait until MIIF convert to 1 (interrupt will be issued according to the user's request) and Clear MIIF
(6) Read receive data from MIDAT, Loop (5) ~ (6) for next receive
(7) Set MISTOP to stop the I²C transfer



Master Receive Timing

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	CMPIE	PPGDIE	I2CIE	ADIE	EX2	P1IE	TM3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.4 **I2CIE:** Master I^2C interrupt enable
0: Disable Master I^2C interrupt
1: Enable Master I^2C interrupt

SFR **E1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MICON	MIEN	MIACKO	MIIF	MIACKI	MISTART	MISTOP	MICR	
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	
Reset	0	0	0	0	0	1	0	0

E1h.7 **MIEN:** Master I^2C enable
0: Master I^2C disable
1: Master I^2C enable

E1h.6 **MIACKO:** When Master I^2C receive data, send acknowledge to I^2C Bus
0: ACK to slave device
1: NACK to slave device

E1h.5 **MIIF:** Master I^2C interrupt flag
Set by H/W when Master I^2C transmit or receive one byte complete. Write "0" to this bit will clear this flag.

E1h.4 **MIACKI:** When Master I^2C transmission, acknowledgement from I^2C Bus (read only)
0: ACK received
1: NACK received

E1h.3 **MISTART:** Master I^2C start bit
1: start I^2C bus transmit

E1h.2 **MISTOP:** Master I^2C stop bit
1: send STOP signal to stop I^2C bus

E1h.1~0 **MICR:** Master I^2C clock frequency selection
00: $F_{SYSCLK}/4$
01: $F_{SYSCLK}/16$
10: $F_{SYSCLK}/64$
11: $F_{SYSCLK}/256$

SFR E**2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MIDAT	MIDAT							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

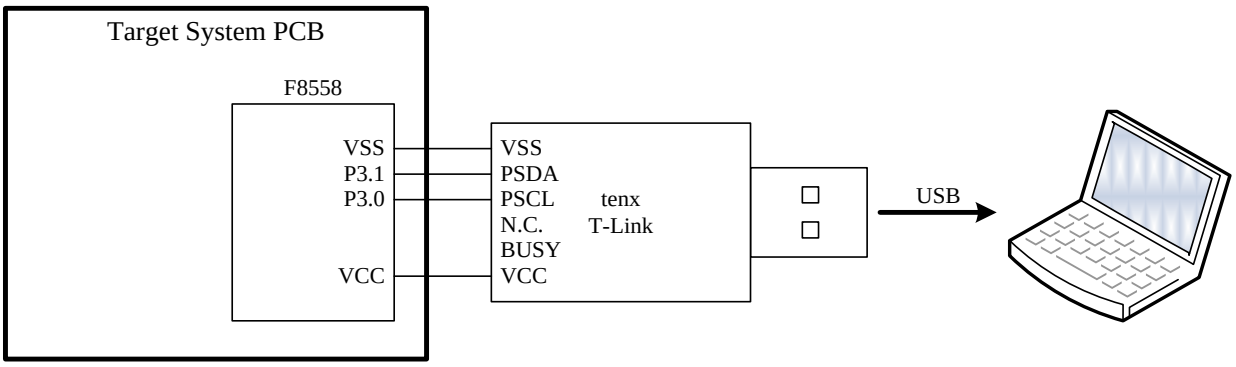
E2h.7~0 **MIDAT:** Master I^2C data shift register
(W): After Start and before Stop condition, write this register will resume transmission to I^2C bus
(R): After Start and before Stop condition, read this register will resume receiving from I^2C bus

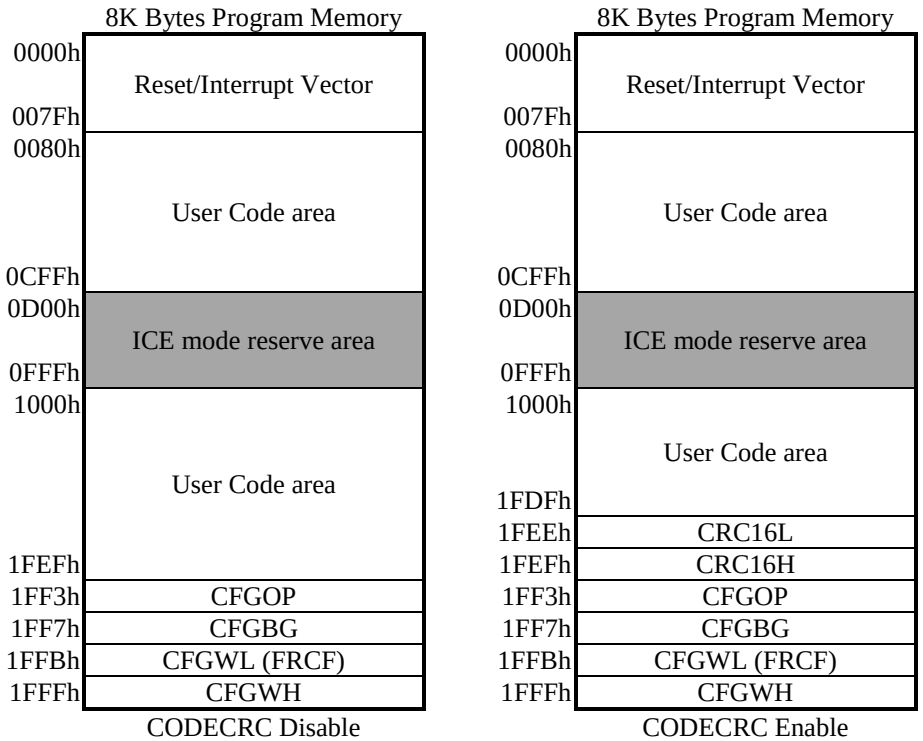
Note: also refer to Section 7 for more information about Master I^2C pin input/output setting.

18. In Circuit Emulation (ICE) Mode

This device can support the In Circuit Emulation Mode. To use the ICE Mode, user just needs to connect P3.0 and P3.1 pin to the tenx proprietary EV Module. The benefit is that user can emulate the whole system without changing the on board target device. But there are some limits for the ICE mode as below.

1. The device must be un-protect.
2. The device's P3.0 and P3.1 pins must work in input Mode (P3MOD0=0/1 and P3MOD1=0/1).
3. The Program Memory's addressing space 0D00h~0FFFh and 0033h~003Ah are occupied by tenx EV Module. So user Program cannot access these spaces.
4. The T-Link communication pin's function cannot be emulated.





SFR & CFGW MAP

Adr	Rst	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h	1111-1111	**P0**	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
81h	0000-0111	**SP**	SP							
82h	0000-0000	**DPL**	DPL							
83h	0000-0000	**DPH**	DPH							
84h	x000-0000	**INTE2**	–	PWM1IE	PWM0IE	CMP5IE	CMP4IE	CMP3IE	CMP2IE	CMP1IE
85h	x000-0000	**INTFLG2**	–	PWM1IF	PWM0IF	CMP5IF	CMP4IF	CMP4IF	CMP2IF	CMP1IF
87h	0xxx-0000	**PCON**	SMOD	–	–	–	GF1	GF0	PD	IDL
88h	0000-0000	**TCON**	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89h	0000-0000	**TMOD**	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
8Ah	0000-0000	**TL0**	TL0							
8Bh	0000-0000	**TL1**	TL1							
8Ch	0000-0000	**TH0**	TH0							
8Dh	0000-0000	**TH1**	TH1							
90h	1111-1111	**P1**	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
94h	0000-0000	**OPTION**	UART1W	TM3CKS	WDTPSC		ADCKS		TM3PSC	
95h	xxx0-x000	**INTFLG**	–	–	–	ADIF	–	IE2	P1IF	TF3
96h	0000-0000	**P1WKUP**	P1WKUP							
97h	xxxx-xxx0	**SWCMD**	SWRST							
98h	0000-0000	**SCON**	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99h	xxxx-xxxx	**SBUF**	SBUF							
9Ah	x000-00x0	**PPDCON**	–	PPDENS			PD1SEL	PD0SEL	–	PPDEN
9Bh	x000-0000	**PPDSTA**	–	CMP4IF2	CMP2IF2	CMP1IF2	PPDIF	PWM0OFFIF	NPGF	SPGF
9Ch	0000-0000	**PPDTH**	PPDTH							
9Dh	xx00-0000	**PPDIES**	–	–	C4PFDE	C2PFDE	C1PFDE	PDPFDE	PWM0OFFIE	PPDIE
A0h	1111-1111	**P2**	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
A1h	00xx-0000	**PWMCON**	PWM1CKS		–	–	PWM0CKS		PWM0NMSK	PWM0PMSK
A2h	0101-0101	**P1MODL**	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
A3h	0101-0101	**P1MODH**	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
A4h	0101-0101	**P3MODL**	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
A5h	0101-0101	**P3MODH**	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
A6h	0000-0001	**PINMOD**	PWM1OE	PWM0POE	PWM0NOE	T2OE	T1OE	T0OE	P2MOD2	
A7h	0000-0000	**PWMCON2**	PWM0MOD	PWM0MSKE	PWM0OM		PWM0DZ			
A8h	0x00-0000	**IE**	EA	–	ET2	ES	ET1	EX1	ET0	EX0
A9h	0000-0000	**INTE1**	PWMIE	CMPIE	PPGDIE	I2CIE	ADIE	EX2	P1IE	TM3IE
AAh	xxxx-xxxx	**ADCDL**	ADCDL				–	–	–	–
ABh	xxxx-xxxx	**ADCDH**	ADCDH							
AEh	1111-xxxx	**CHSEL**	ADCHS				–	–	–	–
B0h	1111-1111	**P3**	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
B1h	00x0-0000	**PPGCON0**	PPGEN	RLDM	–	PPGM	PPGPSC	SYNCNTEN	SYNCNTCLR	SYNEDG
B2h	0000-0000	**PPGCON1**	APPRATE		DECM		DECSTEP			PPGRLD8
B3h	0000-0000	**PPGRLDL**	PPGRLDL							
B6h	0000-0000	**PPGTML**	PPGTML							
B7h	xxxx-xxx0	**PPGTMH**	–	–	–	–	–	–	–	PPGTMH
B8h	xx00-0000	**IP**	–	–	PT2	PS	PT1	PX1	PT0	PX0
B9h	xx00-0000	**IPH**	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
BAh	0000-0000	**IP1**	PPWM	PCMP	PPPGD	PI2C	PADI	PX2	PP1	PT3

Adr	Rst	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BBh	0000-0000	**IP1H**	PPWMH	PCMPH	PPPGDH	PI2CH	PADIH	PX2H	PP1H	PT3H
BFh	0000-0000	**CMPEQI**	CMP5EQIE	CMP4EQIE	CMP3EQIE	CMP2EQIE	CMP5EQIF	CMP4EQIF	CMP3EQIF	CMP2EQIF
C1h	00x0-0000	**CMP1CON**	CMP1EN	CMP1HYS	–	SYNDBT				
C2h	0000-0000	**CMP2CON**	CMP2EN	CMP2HYS	CMP2VRF					
C3h	0000-0000	**CMP3CON**	CMP3EN	CMP3HYS	CMP3VRF					
C4h	0000-0000	**CMP4CON**	CMP4EN	CMP4HYS	CMP4VRF					
C5h	0000-0000	**CMP5CON**	CMP5EN	CMP5HYS	CMP5VRF					
C6h	0111-x111	**CMP23EQ**	CMP3EDS	CMP3EQ			–	CMP2EQ		
C7h	x111-x111	**CMP45EQ**	–	CMP5EQ			–	CMP4EQ		
C8h	0000-0000	**T2CON**	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
C9h	x00x-xxxx	**EEPWE**	EEPWE							
CAh	0000-0000	**RCP2L**	RCP2L							
CBh	0000-0000	**RCP2H**	RCP2H							
CCh	0000-0000	**TL2**	TL2							
CDh	0000-0000	**TH2**	TH2							
CEh	0000-0000	**EXA2**	EXA2							
CFh	0000-0000	**EXA3**	EXA3							
D0h	0000-0000	**PSW**	CY	AC	F0	RS1	RS0	OV	F1	P
D1h	0000-0000	**PWM0DH**	PWM0DH							
D2h	0000-0000	**PWM0DL**	PWM0DL							
D3h	0000-0000	**PWM1DH**	PWM1DH							
D4h	0000-0000	**PWM1DL**	PWM1DL							
D7h	xxx0-0000	**CMPIEDG**	–	–	–	CMP5EDG	CMP4EDG	CMP3EDG	CMP2EDG	CMP1EDG
D8h	xxx0-0011	**CLKCON**	–	–	–	STPPCK	STPFCK	SELFCK	CLKPSC	
D9h	1111-1111	**PWM0PRDH**	PWM0PRDH							
DAh	1111-1111	**PWM0PRDL**	PWM0PRDL							
DBh	1111-1111	**PWM1PRDH**	PWM1PRDH							
DCh	1111-1111	**PWM1PRDL**	PWM1PRDL							
E0h	0000-0000	**ACC**	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
E1h	0000-0100	**MICON**	MIEN	MIACKO	MIIF	MIACKI	MISTART	MISTOP	MICR	
E2h	0000-0000	**MIDAT**	MIDAT							
E3h	0000-0000	**SYNCNT**	SYNCNT							
E4h	xx00-0000	**SYNDLY**	–	–	SYNDLY					
E5h	xxxx-xxxx	**LVRPD**	LVRPD							
E6h	0000-0000	**EXA**	EXA							
E7h	0000-0000	**EXB**	EXB							
E9h	x000-1111	**CMP1CAL**	CMP1O	CMP1MOD	CMP1CTS	CMP1ADJ				
EAh	x000-1111	**CMP2CAL**	CMP2O	CMP2MOD	CMP2CTS	CMP2ADJ				
EBh	x000-1111	**CMP3CAL**	CMP3O	CMP3MOD	CMP3CTS	CMP3ADJ				
ECh	x000-1111	**CMP4CAL**	CMP4O	CMP4MOD	CMP4CTS	CMP4ADJ				
EDh	x000-1111	**CMP5CAL**	CMP5O	CMP5MOD	CMP5CTS	CMP5ADJ				
EEh	0x00-0000	**OPCON**	OPAEN	–	OPOE	OPFUNC		OPGAIN		
EFh	x00x-xxxx	**OPCAL**	OPOUT	OPMOD	CVRFS	OPADJ				
F0h	0000-0000	**B**	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
F1h	1111-1111	**CRCDL**	CRCDL							
F2h	1111-1111	**CRCDH**	CRCDH							
F3h	xxxx-xxxx	**CRCIN**	CRCIN							
F5h	xxxx-xxxx	**CFGBG**	–	–	–	–	BGTRIM			
F6h	xxxx-xxxx	**CFGWL**	–	FRCF						

Adr	Rst	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F7h	0000-0110	**AUX2**	WDTE		PWRSAV	VBGOUT	DIV32	EEPTE		MULDIV16
F8h	00x0-00x0	**AUX1**	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL

Flash Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1FF3h	**CFGOP**	–	–	–	OPTRIM				
1FF7h	**CFGBG**	–	–	–	–	BGTRIM			
1FFBh	**CFGWL**	–	FRCF						
1FFFh	**CFGWH**	PROT	XRSTE	LVRE		–	CODECRC	MVCLOCK	FRCPSC

SFR & CFGW DESCRIPTION

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
80h	P0	7~0	P0	R/W	FFh	Port0 data
81h	SP	7~0	SP	R/W	07h	Stack Point
82h	DPL	7~0	DPL	R/W	00h	Data Point low byte
83h	DPH	7~0	DPH	R/W	00h	Data Point high byte
84h	INTE2	6	PWM1IE	R/W	0	PWM1 interrupt enable 0: Disable PWM1 interrupt 1: Enable PWM1 interrupt
		5	PWM0IE	R/W	0	PWM0 interrupt enable 0: Disable PWM0 interrupt 1: Enable PWM0 interrupt
		4	CMP5IE	R/W	0	CMP5 interrupt enable 0: Disable CMP5 interrupt 1: Enable CMP5 interrupt
		3	CMP4IE	R/W	0	CMP4 interrupt enable 0: Disable CMP4 interrupt 1: Enable CMP4 interrupt
		2	CMP3IE	R/W	0	CMP3 interrupt enable 0: Disable CMP3 interrupt 1: Enable CMP3 interrupt
		1	CMP2IE	R/W	0	CMP2 interrupt enable 0: Disable CMP2 interrupt 1: Enable CMP2 interrupt
		0	CMP1IE	R/W	0	CMP1 interrupt enable 0: Disable CMP1 interrupt 1: Enable CMP1 interrupt
85h	INTFLG2	6	PWM1IF	R/W	0	PWM1 interrupt flag Set by H/W at the end of PWM1 period. S/W writes BFh to INTFLG2 to clear this flag.
		5	PWM0IF	R/W	0	PWM0 interrupt flag Set by H/W at the end of PWM0 period. S/W writes DFh to INTFLG2 to clear this flag.
		4	CMP5IF	R/W	0	CMP5 interrupt flag Set by H/W while CMP5 output rising/falling event occurred. S/W writes EFh to INTFLG2 to clear this flag.
		3	CMP4IF	R/W	0	CMP4 interrupt flag Set by H/W while CMP4 output rising/falling event occurred. S/W writes F7h to INTFLG2 to clear this flag.
		2	CMP3IF	R/W	0	CMP3 interrupt flag Set by H/W while CMP3 output rising/falling event occurred. S/W writes FBh to INTFLG2 to clear this flag.
		1	CMP2IF	R/W	0	CMP2 interrupt flag Set by H/W while CMP2 output rising/falling event occurred. S/W writes FDh to INTFLG2 to clear this flag.
		0	CMP1IF	R/W	0	CMP1 interrupt flag Set by H/W while CMP1 output rising/falling event occurred. S/W writes FEh to INTFLG2 to clear this flag.
87h	PCON	7	SMOD	R/W	0	UART double baud rate control bit 0: Disable UART double baud rate 1: Enable UART double baud rate
		3	GF1	R/W	0	General purpose flag bit
		2	GF0	R/W	0	General purpose flag bit

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
		1	PD	R/W	0	Stop bit. If 1 Stop mode is entered.
		0	IDL	R/W	0	Idle bit. If 1, Idle mode is entered.
88h	TCON	7	TF1	R/W	0	Timer1 overflow flag Set by H/W when Timer/Counter 1 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		6	TR1	R/W	0	Timer1 run control 0: Timer1 stops 1: Timer1 runs
		5	TF0	R/W	0	Timer0 overflow flag Set by H/W when Timer/Counter 0 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		4	TR0	R/W	0	Timer0 run control 0: Timer0 stops 1: Timer0 runs
		3	IE1	R/W	0	External Interrupt 1 (INT1 pin) edge flag Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine.
		2	IT1	R/W	0	External Interrupt 1 control bit 0: Low level active (level triggered) for INT1 pin 1: Falling edge active (edge triggered) for INT1 pin
		1	IE0	R/W	0	External Interrupt 0 (INT0 pin) edge flag Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine.
		0	IT0	R/W	0	External Interrupt 0 control bit 0: Low level active (level triggered) for INT0 pin 1: Falling edge active (edge triggered) for INT0 pin
89h	TMOD	7	GATE1	R/W	0	Timer1 gating control bit 0: Timer1 enable when TR1 bit is set 1: Timer1 enable only while the INT1 pin is high and TR1 bit is set
		6	CT1N	R/W	0	Timer1 Counter/Timer select bit 0: Timer mode, Timer1 data increases at 2 System clock cycle rate 1: Counter mode, Timer1 data increases at T1 pin's negative edge
		5~4	TMOD1	R/W	00	Timer1 mode select 00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 11: Timer1 stops
		3	GATE0	R/W	0	Timer0 gating control bit 0: Timer0 enable when TR0 bit is set 1: Timer0 enable only while the INT0 pin is high and TR0 bit is set
		2	CT0N	R/W	0	Timer0 Counter/Timer select bit 0: Timer mode, Timer0 data increases at 2 System clock cycle rate 1: Counter mode, Timer0 data increases at T0 pin's negative edge
		1~0	TMOD0	R/W	00	Timer0 mode select 00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0) 01: 16-bit timer/counter

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
						10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.
8Ah	TL0	7~0	TL0	R/W	00h	Timer0 data low byte
8Bh	TL1	7~0	TL1	R/W	00h	Timer1 data low byte
8Ch	TH0	7~0	TH0	R/W	00h	Timer0 data high byte
8Dh	TH1	7~0	TH1	R/W	00h	Timer1 data high byte
90h	P1	7~0	P1	R/W	FFh	Port1 data
94h	OPTION	7	UART1W	R/W	0	One wire UART mode enable, both TXD/RXD use P3.1 pin 0: Disable one wire UART mode 1: Enable one wire UART mode
		6	TM3CKS	R/W	0	Timer3 clock source select 0: SRC 1: FRC 16.5888 MHz/512 (32.4 KHz)
		5~4	WDTPSC	R/W	00	Watchdog Timer pre-scalar time select 00: 400ms WDT overflow rate 01: 200ms WDT overflow rate 10: 100ms WDT overflow rate 11: 50ms WDT overflow rate
		3~2	ADCKS	R/W	00	ADC clock rate select 00: $F_{SYSCLK}/32$ 01: $F_{SYSCLK}/16$ 10: $F_{SYSCLK}/8$ 11: $F_{SYSCLK}/4$
		1~0	TM3PSC	R/W	00	Timer3 interrupt rate control select 00: Interrupt rate is 32768 Slow clock cycle 01: Interrupt rate is 16384 Slow clock cycle 10: Interrupt rate is 8192 Slow clock cycle 11: Interrupt rate is 128 Slow clock cycle
95h	INTFLG	4	ADIF	R/W	0	ADC interrupt flag Set by H/W at the end of conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.
		2	IE2	R/W	0	External Interrupt 2 (INT2 pin) edge flag Set by H/W when a falling edge is detected on the INT2 pin state, no matter the EX2 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine. S/W writes FBh to INTFLG to clear this bit.
		1	P1IF	R/W	0	Port1 pin change interrupt flag Set by H/W when a P1 pin state change is detected, and its interrupt enable bit is set (P1WKUP). P1IE does not affect this flag's setting. It is cleared automatically when the program performs the interrupt service routine. S/W writes FDh to INTFLG to clear this bit.
		0	TF3	R/W	0	Timer 3 interrupt flag Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W writes FEh to INTFLG to clear this bit.
96h	P1WKUP	7~0	P1WKUP	R/W	00h	P1.7~P1.0 pin individual Wake up/Interrupt enable control 0: Disable 1: Enable

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
97h	SWCMD	7~0	SWRST	W	–	Write 56h to generate S/W Reset
		1	WDTO	R	0	WatchDog Time-Out flag
98h	SCON	7	SM0	R/W	0	Serial port mode select bit 0,1 00: Mode0: 8 bit shift register, Baud Rate = $F_{SYSCLK}/2$ 01: Mode1: 8 bit UART, Baud Rate is variable 10: Mode2: 9 bit UART, Baud Rate=$F_{SYSCLK}/32$ or /64 11: Mode3: 9 bit UART, Baud Rate is variable
		6	SM1	R/W	0	
		5	SM2	R/W	0	Serial port mode select bit 2 SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.
		4	REN	R/W	0	UART reception enable 0: Disable reception 1: Enable reception
		3	TB8	R/W	0	Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3
		2	RB8	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit in Mode 1 if SM2=0
		1	TI	R/W	0	Transmit interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.
		0	RI	R/W	0	Receive interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.
99h	SBUF	7~0	SBUF	R/W	–	UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
9Ah	PPDCON	6~4	PPDENS	R/W	000	PPD enable select. After CLRPWM0 bit changes to 0, 000: do not wait before start detect 001: wait 1 PWM period before detect 010: wait 2 PWM periods before detect 011: wait 3 PWM periods before detect 100: wait 4 PWM periods before detect 101: wait 5 PWM periods before detect 110: wait 6 PWM periods before detect 111: wait 7 PWM periods before detect
		3	PD1SEL	R/W	0	Phase Detector 1 input source select 0: CMP3O 1: ~CMP3O
		2	PD0SEL	R/W	0	Phase Detector 0 input source select 0: CMP5O 1: ~CMP5O
		0	PPDEN	R/W	0	PPD enable 0: Disable PPD 1: Enable PPD
9Bh	PPDSTA	6	CMP4IF2	R/W	0	CMP4 interrupt flag This bit is same as the bit CMP4IF (85h.3). Set by H/W while CMP4 output rising/falling event occurred. S/W writes BFh to PPDSTA to clear this bit.

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
		5	CMP2IF2	R/W	0	CMP2 interrupt flag This bit is same as the bit CMP2IF (85h.1). Set by H/W while CMP2 output rising/falling event occurred. S/W writes DFh to PPDSTA to clear this bit.
		4	CMP1IF2	R/W	0	CMP1 interrupt flag This bit is same as the bit CMP1IF (85h.0). Set by H/W while CMP1 output rising/falling event occurred. S/W writes EFh to PPDSTA to clear this bit.
		3	PPDIF	R/W	0	PPD interrupt flag Set by H/W while NPGF=1 or SPGF=1. S/W writes F7h to PPDSTA to clear this bit.
		2	PWM0OFFIF	R/W	0	PWM0 turned off by PPD interrupt flag 0: PWM0 not turned off by PPD 1: PWM0 has been turned off by PPD Set by H/W, S/W writes FBh to PPDSTA to clear this bit.
		1	NPGF	R/W	0	No phase flag 0: Phase width is detected 1: No phase width is detected Set by H/W, S/W writes FDh to PPDSTA to clear this bit.
		0	SPGF	R/W	0	Small phase flag 0: Phase width ≥ PPDTH 1: Phase width < PPDTH Set by H/W, S/W writes FEh to PPDSTA to clear this bit.
9Ch	PPDTH	7~0	PPDTH	R/W	00h	PPD phase width threshold
9Dh	PPDIE	5	C4PFDE	R/W	0	CMP4 PWM0 force off enable 0: CMP4 PWM0 force off disable 1: CMP4 PWM0 force off enable
		4	C2PFDE	R/W	0	CMP2 PWM0 force off enable 0: CMP2 PWM0 force off disable 1: CMP2 PWM0 force off enable
		3	C1PFDE	R/W	0	CMP1 PWM0 force off enable 0: CMP1 PWM0 force off disable 1: CMP1 PWM0 force off enable
		2	PDPFDE	R/W	0	Phase detector PWM0 force off enable 0: Phase detector PWM0 force off disable 1: Phase detector PWM0 force off enable
		1	PWM0OFFIE	R/W	0	PWM0 turned off by PPD interrupt enable 0: PWM0 turned off by PPD interrupt disable 1: PWM0 turned off by PPD interrupt enable
		0	PPDIE	R/W	0	PPD interrupt enable 0: PPD interrupt disable 1: PPD interrupt enable
A0h	P2	7~0	P2	R/W	FFh	Port2 data
A1h	PWMCON	7~6	PWM1CKS	R/W	00	PWM1 clock source 00: F_{SYSCLK} 01: F_{SYSCLK} 10: FRC (16.5888 MHz) 11: FRCx2 (33.1776 MHz)
		3~2	PWM0CKS	R/W	00	PWM0 clock source 00: F_{SYSCLK} 01: F_{SYSCLK} 10: FRC (16.5888 MHz) 11: FRCx2 (33.1776 MHz)
		1	PWM0NMSK	R/W	0	PWM0N mask data while CLRPWM0=1 or

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
						PWM0OFFIF=1
		0	PWM0PMSK	R/W	0	PWM0P mask data while CLRPWM0=1 or PWM0OFFIF=1
A2h	P1MODL	7~6	P1MOD3	R/W	01	P1.3 pin control
		5~4	P1MOD2	R/W	01	P1.2 pin control
		3~2	P1MOD1	R/W	01	P1.1 pin control
		1~0	P1MOD0	R/W	01	P1.0 pin control
A3h	P1MODH	7~6	P1MOD7	R/W	01	P1.7 pin control
		5~4	P1MOD6	R/W	01	P1.6 pin control
		3~2	P1MOD5	R/W	01	P1.5 pin control
		1~0	P1MOD4	R/W	01	P1.4 pin control
A4h	P3MODL	7~6	P3MOD3	R/W	01	P3.3 pin control
		5~4	P3MOD2	R/W	01	P3.2 pin control
		3~2	P3MOD1	R/W	01	P3.1 pin control
		1~0	P3MOD0	R/W	01	P3.0 pin control
A5h	P3MODH	7~6	P3MOD7	R/W	01	P3.7 pin control
		5~4	P3MOD6	R/W	01	P3.6 pin control
		3~2	P3MOD5	R/W	01	P3.5 pin control
		1~0	P3MOD4	R/W	01	P3.4 pin control
A6h	PINMOD	7	PWM1OE	R/W	0	PWM1 signal output enable 0: Disable PWM1 signal output to P3.3 1: Enable PWM1 signal output to P3.3
		6	PWM0POE	R/W	0	PWM0P signal output enable 0: Disable PWM0P signal output to P3.5 1: Enable PWM0P signal output to P3.5
		5	PWM0NOE	R/W	0	PWM0N signal output enable 0: Disable PWM0N signal output to P1.2 1: Enable PWM0N signal output to P1.2
		4	T2OE	R/W	0	Timer2 signal output enable 0: Disable Timer2 overflow divided by 2 output to P1.0 1: Enable Timer2 overflow divided by 2 output to P1.0
		3	T1OE	R/W	0	Timer1 signal output enable 0: Disable Timer1 overflow divided by 2 output to P3.5 1: Enable Timer1 overflow divided by 2 output to P3.5
		2	T0OE	R/W	0	Timer0 signal output enable 0: Disable Timer0 overflow divided by 64 output to P3.4 1: Enable Timer0 overflow divided by 64 output to P3.4
		1~0	P2MOD2	R/W	01	P2.2 pin control
A7h	PWMCON2	7	PWM0MOD	R/W	0	PWM0 mode select 0: Normal mode 1: Half-bridge mode
		6	PWM0MSKE	R/W	0	PWM0 output mask enable 0: Disable PWM0 output mask 1: Enable PWM0 output mask
		5~4	PWM0OM	R/W	00	PWM0 output mode 00~11: Mode0~Mode3
		3~0	PWM0DZ	R/W	0h	PWM0 dead zone 0000: Disable 0001: 1 T_{PWMCLK} 0010: 2 T_{PWMCLK} 0011: 3 T_{PWMCLK} 0100: 4 T_{PWMCLK}

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
						0101: 5 T_{PWMCLK} 0110: 6 T_{PWMCLK} 0111: 7 T_{PWMCLK} 1000: 8 T_{PWMCLK} 1001: 9 T_{PWMCLK} 1010: 10 T_{PWMCLK} 1011: 11 T_{PWMCLK} 1100: 12 T_{PWMCLK} 1101: 13 T_{PWMCLK} 1110: 14 T_{PWMCLK} 1111: 16 T_{PWMCLK}
A8h	IE	7	EA	R/W	0	Global interrupt enable 0: Disable all interrupts 1: Each interrupt is enabled or disabled by its individual interrupt control bit
		5	ET2	R/W	0	Timer2 interrupt enable 0: Disable Timer2 interrupt 1: Enable Timer2 interrupt
		4	ES	R/W	0	Serial Port (UART) interrupt enable 0: Disable Serial Port (UART) interrupt 1: Enable Serial Port (UART) interrupt
		3	ET1	R/W	0	Timer1 interrupt enable 0: Disable Timer1 interrupt 1: Enable Timer1 interrupt
		2	EX1	R/W	0	INT1 pin Interrupt enable and Stop mode wake up enable 0: Disable INT1 pin Interrupt and Stop mode wake up 1: Enable INT1 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.
		1	ET0	R/W	0	Timer0 interrupt enable 0: Disable Timer0 interrupt 1: Enable Timer0 interrupt
		0	EX0	R/W	0	INT0 pin Interrupt enable and Stop mode wake up enable 0: Disable INT0 pin Interrupt and Stop mode wake up 1: Enable INT0 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.
A9h	INTE1	7	PWMIE	R/W	0	PWM0/PWM1 interrupt enable 0: Disable PWM0/PWM1 interrupt 1: Enable PWM0/PWM1 interrupt
		6	CMPIE	R/W	0	CMP1~5 interrupt enable 0: Disable CMP1~5 interrupt 1: Enable CMP1~5 interrupt
		5	PPGDIE	R/W	0	PPG/PPD interrupt enable 0: Disable PPG/PPD interrupt 1: Enable PPG/PPD interrupt
		4	I2CIE	R/W	0	Master I^2C interrupt enable 0: Disable Master I^2C interrupt 1: Enable Master I^2C interrupt
		3	ADIE	R/W	0	ADC interrupt enable 0: Disable ADC interrupt 1: Enable ADC interrupt
		2	EX2	R/W	0	INT2 pin Interrupt enable and Stop mode wake up enable 0: Disable INT2 pin Interrupt and Stop mode wake up 1: Enable INT2 pin Interrupt and Stop mode wake up, it

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
						can wake up CPU from Stop mode no matter EA is 0 or 1.
		1	P1IE	R/W	0	Port1 pin change interrupt enable 0: Disable Port1 pin change interrupt 1: Enable Port1 pin change interrupt
		0	TM3IE	R/W	0	Timer3 interrupt enable 0: Disable Timer3 interrupt 1: Enable Timer3 interrupt
AAh	ADCDL	7~4	ADCDL	R	–	ADC data bit 3~0
ABh	ADCDH	7~0	ADCDH	R	–	ADC data bit 11~4
AEh	CHSEL	7~4	ADCHS	R/W	1111	ADC channel select 0000: AD0 (P1.0) 0001: AD1 (P1.6) 0010: AD2 (P3.2) 0011: AD3 (P3.4) 0100: AD4 (P2.2) 0101: AD5 (P3.3) 0110: AD6 (P1.2) 0111: AD7 (P3.0) 1000: AD8 (P3.7) 1001: AD9 (P3.1) 1010: AD10 (P3.5) 1011: AD11 (P3.6) 1100: VBG (internal Bandgap reference voltage) 1101: Reserved 1110: OPOUT 1111: V_{SS}
B0h	P3	7~0	P3	R/W	FFh	Port3 data
B1h	PPGCON0	7	PPGEN	R/W	0	PPG output enable Single pulse mode Write “1” to generate a single pulse. This bit is cleared automatically by H/W when PPGTMR time up. Synchronous mode When this bit is set, PPG module generates a pulse for each CMP1 trigger event.
		6	RLDM	R/W	0	PPG reload mode 0: Direct reload, working buffer synchronizes with reload buffer 1: Approach mode, working buffer approach to reload buffer gradually at certain rate
		4	PPGM	R/W	0	PPG output mode 0: Single pulse mode 1: Synchronous mode
		3	PPGPSC	R/W	0	PPG module clock source prescaler 0: $F_{SYSCLK}/2$ 1: $F_{SYSCLK}/4$
		2	SYNCNTEN	R/W	0	CMP1 synchronous event counter enable 0: Disable 1: Enable
		1	SYNCNTCLR	R/W	0	CMP1 synchronous event counter clear Write “1” to this bit to clear synchronous counter. Automatically cleared by H/W.
		0	SYNEDG	R/W	0	CMP1 synchronous event trigger edge select 0: Falling-edge trigger 1: Rising-edge trigger

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
B2h	PPGCON2	7~6	APPRATE	R/W	00	PPG reload buffer approach rate (Synchronous mode only) 00: every 512*T_{PPG} increase/decrease by 1 01: every 1024*T_{PPG} increase/decrease by 1 10: every 2048*T_{PPG} increase/decrease by 1 11: every 4096*T_{PPG} increase/decrease by 1
		5~4	DECM	R/W	00	PPG pulse width decrement mode (Synchronous mode only) 0x: No decrement but clear PPGEN and stop PPG output when CMP2 event triggered 10: Constant step decrement 11: Variable step decrement
		3~1	DECSTEP	R/W	000	PPG pulse width decrement step (Synchronous mode only) Constant step 000~111: decrease by 1~8 Variable step: decrease by 1 + (T_{CMP2}/T_{PPG}*bSTEP)) 000~011: bSTEP = 64, 32, 16, 8 100~111: bSTEP = 8
		0	PPGRLD8	R/W	0	PPG reload buffer bit 8
B3h	PPGRLDL	7~0	PPGRLDL	R//W	0	PPG reload buffer bit 7~0
B6h	PPGTML	7~0	PPGTML	R	00h	PPG timer bit 7~0
B7h	PPGTMH	0	PPGTMH	R	0	PPG timer bit 8
B8h	IP	5	PT2	R/W	0	Timer2 interrupt priority low bit
		4	PS	R/W	0	Serial Port interrupt priority low bit
		3	PT1	R/W	0	Timer1 interrupt priority low bit
		2	PX1	R/W	0	INT1 interrupt priority low bit
		1	PT0	R/W	0	Timer0 interrupt priority low bit
		0	PX0	R/W	0	INT0 interrupt priority low bit
B9h	IPH	5	PT2H	R/W	0	Timer2 interrupt priority high bit
		4	PSH	R/W	0	Serial Port interrupt priority high bit
		3	PT1H	R/W	0	Timer1 interrupt priority high bit
		2	PX1H	R/W	0	INT1 interrupt priority high bit
		1	PT0H	R/W	0	Timer0 interrupt priority high bit
		0	PX0H	R/W	0	INT0 interrupt priority high bit
BAh	IP1	7	PPWM	R/W	0	PWM0/PWM1 interrupt priority low bit
		6	PCMP	R/W	0	CMP1~5 interrupt priority low bit
		5	PPPGD	R/W	0	PPG/PPD interrupt priority low bit
		4	PI2C	R/W	0	Master I^2C interrupt priority low bit
		3	PAD	R/W	0	ADC interrupt priority low bit
		2	PX2	R/W	0	INT2 interrupt priority low bit
		1	PP1	R/W	0	Port1 pin change interrupt priority low bit
		0	PT3	R/W	0	Timer3 interrupt priority low bit
BBh	IP1H	7	PPWMH	R/W	0	PWM0/PWM1 interrupt priority high bit
		6	PCMPH	R/W	0	CMP1~5 interrupt priority high bit
		5	PPPGDH	R/W	0	PPG/PPD interrupt priority high bit
		4	PI2CH	R/W	0	Master I^2C interrupt priority high bit
		3	PADH	R/W	0	ADC interrupt priority high bit
		2	PX2H	R/W	0	INT2 interrupt priority high bit
		1	PP1H	R/W	0	Port1 interrupt priority high bit
		0	PT3H	R/W	0	Timer3 interrupt priority high bit
BFh	CMPEQI	7	CMP5EQIE	R/W	0	CMP5 qualified interrupt enable

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
						0: Disable CMP5EQ interrupt 1: Enable CMP5EQ interrupt
		6	CMP4EQIE	R/W	0	CMP4 qualified interrupt enable 0: Disable CMP4EQ interrupt 1: Enable CMP4EQ interrupt
		5	CMP3EQIE	R/W	0	CMP3 qualified interrupt enable 0: Disable CMP3EQ interrupt 1: Enable CMP3EQ interrupt
		4	CMP2EQIE	R/W	0	CMP2 qualified interrupt enable 0: Disable CMP2EQ interrupt 1: Enable CMP2EQ interrupt
		3	CMP5EQIF	R/W	0	CMP5 qualified event interrupt flag Set by H/W while CMP5 qualified event occurred. Write "0" to this bit will clear this flag.
		2	CMP4EQIF	R/W	0	CMP4 qualified event interrupt flag Set by H/W while CMP4 qualified event occurred. Write "0" to this bit will clear this flag.
		1	CMP3EQIF	R/W	0	CMP3 qualified event interrupt flag Set by H/W while CMP3 qualified event occurred. Write "0" to this bit will clear this flag.
		0	CMP2EQIF	R/W	0	CMP2 qualified event interrupt flag Set by H/W while CMP2 qualified event occurred. Write "0" to this bit will clear this flag.
C1h	CMP1CON	7	CMP1EN	R/W	0	CMP1 enable 0: CMP1 disable 1: CMP1 enable
		6	CMP1HYS	R/W	0	CMP1 hysteresis enable 0: Disable CMP1 hysteresis 1: Enable CMP1 hysteresis
		4~0	SYNDBT	R/W	00h	PPG synchornous mode CMP1 output debounce time Debounce time: SYNDBT*T_{PPG} If SYNDBT=0, CMP1 output is directly bypassed to output of debounce circuit
C2h	CMP2CON	7	CMP2EN	R/W	0	CMP2 enable 0: CMP2 disable 1: CMP2 enable
		6	CMP2HYS	R/W	0	CMP2 hysteresis enable 0: Disable CMP2 hysteresis 1: Enable CMP2 hysteresis
		5~0	CMP2VRF	R/W	00h	CMP2 reference level select 000000~111111: 0V ~ (63/64) * V_{CC} Reference level = (1/64) * CMP2VRF * V_{CC}
C3h	CMP3CON	7	CMP3EN	R/W	0	CMP3 enable 0: CMP3 disable 1: CMP3 enable
		6	CMP3HYS	R/W	0	CMP3 hysteresis enable 0: Disable CMP3 hysteresis 1: Enable CMP3 hysteresis
		5~0	CMP3VRF	R/W	00h	CMP3 reference level select 000000~111111: 0V ~ (63/64) * V_{CC} Reference level = (1/64) * CMP3VRF * V_{CC}
C4h	CMP4CON	7	CMP4EN	R/W	0	CMP4 enable 0: CMP4 disable 1: CMP4 enable
		6	CMP4HYS	R/W	0	CMP4 hysteresis enable

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
						0: Disable CMP4 hysteresis 1: Enable CMP4 hysteresis
		5~0	CMP4VRF	R/W	00h	CMP4 reference level select 000000~111111: 0V ~ (63/64) * V_{CC} Reference level = (1/64) * CMP4VRF * V_{CC}
C5h	CMP5CON	7	CMP5EN	R/W	0	CMP5 enable 0: CMP5 disable 1: CMP5 enable
		6	CMP5HYS	R/W	0	CMP5 hysteresis enable 0: Disable CMP5 hysteresis 1: Enable CMP5 hysteresis
		5~0	CMP5VRF	R/W	00h	CMP5 reference level select 000000~111111: 0V ~ (63/64) * V_{CC} Reference level = (1/64) * CMP5VRF * V_{CC}
C6h	CMP23EQ	7	CMP3EDS	R/W	0	CMP3 event detect select 0: always detect 1: detect during PPG output active
		6~4	CMP3EQ	R/W	111	CMP3 output low event qualification 000~111: 1, 2, 4, 8, 16, 32, 64, 128 * T_{PPG}
		2~0	CMP2EQ	R/W	111	CMP2 output falling event qualification 000~111: 1, 2, 4, 8, 16, 32, 64, 128 consecutive falling events
C7h	CMP45EQ	6~4	CMP5EQ	R/W	111	CMP5 output low event qualification 000~111: 1, 2, 4, 8, 16, 32, 64, 128 * T_{PPG}
		2~0	CMP4EQ	R/W	111	CMP4 output low event qualification 000~111: 1, 2, 4, 8, 16, 32, 64, 128 * T_{PPG}
C8h	T2CON	7	TF2	R/W	0	Timer2 overflow flag Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.
		6	EXF2	R/W	0	T2EX interrupt pin falling edge flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.
		5	RCLK	R/W	0	UART receive clock control bit 0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3 1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3
		4	TCLK	R/W	0	UART transmit clock control bit 0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3 1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3
		3	EXEN2	R/W	0	T2EX pin enable 0: T2EX pin disable 1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0
		2	TR2	R/W	0	Timer2 run control 0: Timer2 stops 1: Timer2 runs
		1	CT2N	R/W	0	Timer2 Counter/Timer select bit 0: Timer mode, Timer2 data increases at 2 System clock cycle rate 1: Counter mode, Timer2 data increases at T2 pin's

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
						negative edge
		0	CPRL2N	R/W	0	Timer2 Capture/Reload control bit 0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1 1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1 If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow
C9h	EEPWE	7~0	EEPWE	W	–	Write E2h to set EEPWE control flag; Write other value to clear EEPWE flag. It is recommended to clear it immediately after EEPROM write.
		6	EEPTO	R	0	EEPROM write time-out flag Set by H/W when EEPROM write time-out occurs. Cleared by H/W when EEPWE=0.
		5	EEPWE	R	0	Flag indicates EEPROM memory can be written or not 0: EEPROM write disable 1: EEPROM write enable
CAh	RCP2L	7~0	RCP2L	R/W	00h	Timer2 reload/capture data low byte
CBh	RCP2H	7~0	RCP2H	R/W	00h	Timer2 reload/capture data high byte
CCh	TL2	7~0	TL2	R/W	00h	Timer2 data low byte
CDh	TH2	7~0	TH2	R/W	00h	Timer2 data high byte
CEh	EXA2	7~0	EXA2	R/W	00h	Extra ACC for 32/16 bit division operation
CFh	EXA3	7~0	EXA3	R/W	00h	Extra ACC for 32/16 bit division operation
D0h	PSW	7	CY	R/W	0	ALU carry flag
		6	AC	R/W	0	ALU auxiliary carry flag
		5	F0	R/W	0	General purpose user-definable flag
		4	RS1	R/W	0	The contents of (RS1, RS0) enable the working register banks as: 00: Bank 0 (00h~07h) 01: Bank 1 (08h~0Fh) 10: Bank 2 (10h~17h) 11: Bank 3 (18h~1Fh)
		3	RS0	R/W	0	
		2	OV	R/W	0	ALU overflow flag
		1	F1	R/W	0	General purpose user-definable flag
		0	P	R/W	0	Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of “one” bits in the accumulator.
D1h	PWM0DH	7~0	PWM0DH	R/W	00h	PWM0 duty bit 15~8
D2h	PWM0DL	7~0	PWM0DL	R/W	00h	PWM0 duty bit 7~0
D3h	PWM1DH	7~0	PWM1DH	R/W	00h	PWM1 duty bit 15~8
D4h	PWM1DL	7~0	PWM1DL	R/W	00h	PWM1 duty bit 7~0
D7	CMPIEDG	4	CMP5EDG	R/W	0	CMP5 interrupt trigger edge 0: Falling edge 1: Rising edge
		3	CMP4EDG	R/W	0	CMP4 interrupt trigger edge 0: Falling edge 1: Rising edge
		2	CMP3EDG	R/W	0	CMP3 interrupt trigger edge 0: Falling edge 1: Rising edge
		1	CMP2EDG	R/W	0	CMP2 interrupt trigger edge 0: Falling edge 1: Rising edge

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
		0	CMP1EDG	R/W	0	CMP1 interrupt trigger edge 0: Falling edge 1: Rising edge
D8h	CLKCON	4	STPPCK	R/W	0	Set 1 to stop UART/Timer0/Timer1/Timer2/ADC clock in Idle mode
		3	STPFCK	R/W	0	Set 1 to stop Fast clock for power saving in Slow / Idle mode. This bit can be changed only in Slow mode.
		2	SELFCK	R/W	0	System clock source selection. This bit can be changed only when STPFCK=0. 0: Slow clock 1: Fast clock
		1~0	CLKPSC	R/W	11	System clock prescaler. 00: System clock is Fast/Slow clock divided by 16 01: System clock is Fast/Slow clock divided by 4 10: System clock is Fast/Slow clock divided by 2 11: System clock is Fast/Slow clock divided by 1
D9h	PWM0PRDH	7~0	PWM0PRDH	R/W	FFh	PWM0 period bit 15~8
DAh	PWM0PRDL	7~0	PWM0PRDL	R/W	FFh	PWM0 period bit 7~0
DBh	PWM1PRDH	7~0	PWM1PRDH	R/W	FFh	PWM1 period bit 15~8
DCh	PWM1PRDL	7~0	PWM1PRDL	R/W	FFh	PWM1 period bit 7~0
E0h	ACC	7~0	ACC	R/W	00h	Accumulator
E1h	MICON	7	MIEN	R/W	0	Master I^2C enable 0: Master I^2C disable 1: Master I^2C enable
		6	MIACKO	R/W	0	When Master I^2C receive data, send acknowledge to IIC bus 0: ACK to slave device 1: NACK to slave device
		5	MIIF	R/W	0	Master IIC interrupt flag Set by H/W when Master I^2C transmit or receive one byte complete. Write "0" to this bit will clear this flag.
		4	MIACKI	R	0	When Master I^2C transmission, acknowledgement from IIC bus (read only) 0: ACK received 1: NACK received
		3	MISTART	R/W	0	Master I^2C start bit
		2	MISTOP	R/W	1	Master I^2C stop bit
		1~0	MICR	R/W	00	Master I^2C clock frequency selection 00: $F_{SYSCLK}/4$ 01: $F_{SYSCLK}/16$ 10: $F_{SYSCLK}/64$ 11: $F_{SYSCLK}/256$
E2h	MIDAT	7~0	MIDAT	R/W	00h	Master I^2C data shift register W: After start and before stop condition, write this register will resume transmission to IIC bus R: After start and before stop condition, read this register will resume receiving from IIC bus
E3h	SYNCNT	7~0	SYNCNT	R	00h	CMP1 synchronous event counter. The value of this register is in range of 0`128. SYNCNT can be cleared by writing "1" to SYNCNTCLR bit of PPGCON0.
E4h	SYNDLY	5~0	SYNDLY	R/W	00h	PPG output delay time (Synchronous mode only) The PPG output delay time is calculated as following equation Delay time = SYNDLY * T_{PPG}

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
E5h	LVRPD	7~0	LVRPD	W	00h	LVR and POR power down option Write 0x37 to force LVR disable, POR disable Write 0x38 to force LVR disable, POR enable
E6h	EXA	7~0	EXA	R/W	00h	Extra ACC for 16 bits mul/div operation
E7h	EXB	7~0	EXB	R/W	00h	Extra B for 16 bits mul/div operation
E9h	CMP1CAL	7	CMP1O	R	–	CMP1 output status 0: $V_{IN+} < V_{IN-}$ 1: $V_{IN+} > V_{IN-}$
		6	CMP1MOD	R/W	0	CMP1 operating mode select 0: Normal mode 1: Calibration mode
		5	CMP1CTS	R/W	0	CMP1 calibration terminal select 0: Select inverting input 1: Select non-inverting input
		4~0	CMP1ADJ	R/W	00h	CMP1 offset voltage adjust 00000~11111: $-V_{OS\_MAX} \sim +V_{OS\_MAX}$
EAh	CMP2CAL	7	CMP2O	R	–	CMP2 output status 0: $V_{IN+} < V_{IN-}$ 1: $V_{IN+} > V_{IN-}$
		6	CMP2MOD	R/W	0	CMP2 operating mode select 0: Normal mode 1: Calibration mode
		5	CMP2CTS	R/W	0	CMP2 calibration terminal select 0: Select inverting input 1: Select non-inverting input
		4~0	CMP2ADJ	R/W	00h	CMP2 offset voltage adjust 00000~11111: $-V_{OS\_MAX} \sim +V_{OS\_MAX}$
EBh	CMP3CAL	7	CMP3O	R	–	CMP3 output status 0: $V_{IN+} < V_{IN-}$ 1: $V_{IN+} > V_{IN-}$
		6	CMP3MOD	R/W	0	CMP3 operating mode select 0: Normal mode 1: Calibration mode
		5	CMP3CTS	R/W	0	CMP3 calibration terminal select 0: Select inverting input 1: Select non-inverting input
		4~0	CMP3ADJ	R/W	00h	CMP3 offset voltage adjust 00000~11111: $-V_{OS\_MAX} \sim +V_{OS\_MAX}$
ECh	CMP4CAL	7	CMP4O	R	–	CMP4 output status 0: $V_{IN+} < V_{IN-}$ 1: $V_{IN+} > V_{IN-}$
		6	CMP4MOD	R/W	0	CMP4 operating mode select 0: Normal mode 1: Calibration mode
		5	CMP4CTS	R/W	0	CMP4 calibration terminal select 0: Select inverting input 1: Select non-inverting input
		4~0	CMP4ADJ	R/W	00h	CMP4 offset voltage adjust 00000~11111: $-V_{OS\_MAX} \sim +V_{OS\_MAX}$
EDh	CMP5CAL	7	CMP5O	R	–	CMP5 output status 0: $V_{IN+} < V_{IN-}$ 1: $V_{IN+} > V_{IN-}$
		6	CMP5MOD	R/W	0	CMP5 operating mode select 0: Normal mode

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
						1: Calibration mode
		5	CMP5CTS	R/W	0	CMP5 calibration terminal select 0: Select inverting input 1: Select non-inverting input
		4~0	CMP5ADJ	R/W	00h	CMP5 offset voltage adjust 00000~11111: $-V_{OS\_MAX}$ ~ $+V_{OS\_MAX}$
EEh	OPCON	7	OPAEN	R/W	0	OPAmp enable 0: OPAmp disable 1: OPAmp enable
		5	OPOE	R/W	0	OPAmp output to P1.6 enable 0: Disable OPAmp output to P1.6 1: Enable OPAmp output to P1.6
		4~3	OPFUNC	R/W	00	OPAmp function select Normal mode 00: [IP] OPP (P1.0), [IN] VSS with inter-gain 01: [IP] VSS, [IN] OPN (P1.1) with inter-gain 10: [IP] VSS with 1KR, [IN] OPN (P1.1) with inter-gain 11: [IP] OPP (P1.0), [IN] OPN (P1.1) Calibration mode 00: [IP] Vtrim, [IN] Vtrim (Vtrim = VSS or VBG, defineed by CVRFS) 01: [IP] VSS, [IN] VSS with inter-gain 10: [IP] VSS with 1KR, [IN] VSS with inter-gain 11: [IP] OPP (P1.0), [IN] OPN (P1.1)
		2~0	OPGAIN	R/W	000	OPAmp internal gain select 000~111: 20X, 25X, 30X, 35X, 100X, 105X, 110X, 115X
EFh	OPCAL	7	OPOUT	R	–	OPAmp output state in calibration mode 0: $V_{IN+} < V_{IN-}$ 1: $V_{IN+} > V_{IN-}$
		6	OPMOD	R/W	0	OPAmp operation mode select 0: Normal mode 1: Calibration mode
		5	CVRFS	R/W	0	Calibration mode reference level select 0: Select VSS 1: Select on-chip Bandgap reference voltage (VBG)
		4~0	OPADJ	R/W	–	OPAmp offset voltage adjust 00000~11111: $-V_{OS\_MAX}$ ~ $+V_{OS\_MAX}$ The offset voltage of devices has been calibrated before delivery. User can check the default (calibrated) value by reading this register before user's recalibrating process.
F0h	B	7~0	B	R/W	00h	B register
F1h	CRCDL	7~0	CRCDL	R/W	FFh	16-bit CRC data bit 7~0
F2h	CRCDH	7~0	CRCDH	R/W	FFh	16-bit CRC data bit 15~8
F3h	CRCIN	7~0	CRCIN	W	–	CRC input data
F5h	CFGBG	3~0	BGTRIM	R/W	–	VBG trimming value
F6h	CFGWL	6~0	FRCF	R/W	–	FRC frequency adjustment 00h: lowest frequency 7Fh: highest frequency The frequency range is about 13MHz (FRCF=00h) to 22MHz (FRCF=7Fh) with approaching linearity. Due to the chip process issue, the frequency range is different between each chip.

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
F7h	AUX2	7~6	WDTE	R/W	00	Watchdog Timer Reset control 0x: Watchdog Timer Reset disable 10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Stop mode 11: Watchdog Timer Reset always enable
		5	PWRSAV	R/W	0	Set “ to reduce the chip’s power consumption at Idle and Stop mode
		4	VBGOUT	R/W	0	Bandgap voltage output control 0: P3.2 as normal I/O 1: Bandgap voltage output to P3.2 pin, with ADCHS = 1100b
		3	DIV32	R/W	0	0:16/16 division operation 1: 32/16 division operation
		2~1	EEPTE	R/W	11	EEPROM write watchdog timer enable 00: Disable 01: wait 0.8mS trigger watchdog time-out flag 10: wait 3.1mS trigger watchdog time-out flag 11: wait 6.2mS trigger watchdog time-out flag
		0	MULDIV16	R/W	0	0: 8bit mul/div
F8h	AUX1	7	CLRWDT	R/W	0	Set to clear WDT, H/W auto clear it at next clock cycle
		6	CLRTM3	R/W	0	Set to clear Timer3, H/W auto clear it at next clock cycle
		4	ADSOC	R/W	0	Start ADC conversion Set the ADSOC bit to start ADC conversion, and the ADSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
		3	CLRPWM0	R/W	0	PWM0 clear enable 0: PWM0 is running 1: PWM0 is cleared and held
		2	CLRPWM1	R/W	0	PWM1 clear enable 0: PWM1 is running 1: PWM1 is cleared and held
		0	DPSEL	R/W	0	Active DPTR Select

Flash Adr	CFG Name	Bit #	Bit Name	Description
1FF3h	CFGOP	4~0	OPTRIM	OP-Amp offset voltage adjustment.
1FF7h	CFGBG	3~0	BGTRIM	Bandgap voltage adjustment. VBG is trimmed to 1.22V in chip manufacturing. BGTRIM records the adjustment data.
1FFBh	CFGWL	6~0	FRCF	FRC frequency adjustment. FRC is trimmed to 16.5888 MHz in chip manufacturing. FRCF records the adjustment data.
1FFFh	CFGWH	7	PROT	Flash Memory Code Protect 0: Disable protect 1: Enable protect
		6	XRSTE	External Pin Reset control 0: Disable External Pin Reset 1: Enable External Pin Reset
		5~4	LVRE	Low Voltage Reset function select 00: Set LVR at 4.3V 01: Set LVR at 3.8V 10: Set LVR at 3.2V 11: Set LVR at 2.7V
		2	CODECRC	User Code CRC16 Verification 0: Disable (Valid User Code Range is 0000h~1FEFh) 1: Enable (Valid User Code Range is 0000h~1FDFh)
		1	MVCLOCK	If 1, the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited.
		0	FRCPSC	FRC Prescaler 0: FRC/1 (16.5888MHz) 1: FRC/2 (8.2944MHz)

INSTRUCTION SET

Instructions are 1, 2 or 3 Bytes long as listed in the 'byte' column below. Each instruction takes 2~8 System clock cycles to execute as listed in the 'cycle' column below.

ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ADD A, Rn	Add register to A	1	2	28-2F
ADD A, dir	Add direct byte to A	2	2	25
ADD A, @Ri	Add indirect memory to A	1	2	26-27
ADD A, #data	Add immediate to A	2	2	24
ADDC A, Rn	Add register to A with carry	1	2	38-3F
ADDC A, dir	Add direct byte to A with carry	2	2	35
ADDC A, @Ri	Add indirect memory to A with carry	1	2	36-37
ADDC A, #data	Add immediate to A with carry	2	2	34
SUBB A, Rn	Subtract register from A with borrow	1	2	98-9F
SUBB A, dir	Subtract direct byte from A with borrow	2	2	95
SUBB A, @Ri	Subtract indirect memory from A with borrow	1	2	96-97
SUBB A, #data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	2	04
INC Rn	Increment register	1	2	08-0F
INC dir	Increment direct byte	2	2	05
INC @Ri	Increment indirect memory	1	2	06-07
DEC A	Decrement A	1	2	14
DEC Rn	Decrement register	1	2	18-1F
DEC dir	Decrement direct byte	2	2	15
DEC @Ri	Decrement indirect memory	1	2	16-17
INC DPTR	Increment data pointer	1	4	A3
MUL AB	Multiply A by B	1	8	A4
DIV AB	Divide A by B	1	8	84
DA A	Decimal Adjust A	1	2	D4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ANL A, Rn	AND register to A	1	2	58-5F
ANL A, dir	AND direct byte to A	2	2	55
ANL A, @Ri	AND indirect memory to A	1	2	56-57
ANL A, #data	AND immediate to A	2	2	54
ANL dir, A	AND A to direct byte	2	2	52
ANL dir, #data	AND immediate to direct byte	3	4	53
ORL A, Rn	OR register to A	1	2	48-4F
ORL A, dir	OR direct byte to A	2	2	45
ORL A, @Ri	OR indirect memory to A	1	2	46-47
ORL A, #data	OR immediate to A	2	2	44
ORL dir, A	OR A to direct byte	2	2	42
ORL dir, #data	OR immediate to direct byte	3	4	43
XRL A, Rn	Exclusive-OR register to A	1	2	68-6F
XRL A, dir	Exclusive-OR direct byte to A	2	2	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	2	66-67
XRL A, #data	Exclusive-OR immediate to A	2	2	64
XRL dir, A	Exclusive-OR A to direct byte	2	2	62
XRL dir, #data	Exclusive-OR immediate to direct byte	3	4	63
CLR A	Clear A	1	2	E4
CPL A	Complement A	1	2	F4
SWAP A	Swap Nibbles of A	1	2	C4
RL A	Rotate A left	1	2	23

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
RLC A	Rotate A left through carry	1	2	33
RR A	Rotate A right	1	2	03
RRC A	Rotate A right through carry	1	2	13

DATA TRANSFER				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MOV A, Rn	Move register to A	1	2	E8-EF
MOV A, dir	Move direct byte to A	2	2	E5
MOV A, @Ri	Move indirect memory to A	1	2	E6-E7
MOV A, #data	Move immediate to A	2	2	74
MOV Rn, A	Move A to register	1	2	F8-FF
MOV Rn, dir	Move direct byte to register	2	4	A8-AF
MOV Rn, #data	Move immediate to register	2	2	78-7F
MOV dir, A	Move A to direct byte	2	2	F5
MOV dir, Rn	Move register to direct byte	2	4	88-8F
MOV dir, dir	Move direct byte to direct byte	3	4	85
MOV dir, @Ri	Move indirect memory to direct byte	2	4	86-87
MOV dir, #data	Move immediate to direct byte	3	4	75
MOV @Ri, A	Move A to indirect memory	1	2	F6-F7
MOV @Ri, dir	Move direct byte to indirect memory	2	4	A6-A7
MOV @Ri, #data	Move immediate to indirect memory	2	2	76-77
MOV DPTR, #data	Move immediate to data pointer	3	4	90
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	4	93
MOVC A, @A+PC	Move code byte relative PC to A	1	4	83
MOVX A, @Ri	Move external data (A8) to A	1	4	E2-E3
MOVX A, @DPTR	Move external data (A16) to A	1	4	E0
MOVX @Ri, A	Move A to external data (A8)	1	4	F2-F3
MOVX @DPTR, A	Move A to external data (A16)	1	4	F0
PUSH dir	Push direct byte onto stack	2	4	C0
POP dir	Pop direct byte from stack	2	4	D0
XCH A, Rn	Exchange A and register	1	2	C8-CF
XCH A, dir	Exchange A and direct byte	2	2	C5
XCH A, @Ri	Exchange A and indirect memory	1	2	C6-C7
XCHD A, @Ri	Exchange A and indirect memory nibble	1	2	D6-D7

BOOLEAN				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
CLR C	Clear carry	1	2	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	2	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	2	B3
CPL bit	Complement direct bit	2	2	B2
ANL C, bit	AND direct bit to carry	2	4	82
ANL C, /bit	AND direct bit inverse to carry	2	4	B0
ORL C, bit	OR direct bit to carry	2	4	72
ORL C, /bit	OR direct bit inverse to carry	2	4	A0
MOV C, bit	Move direct bit to carry	2	2	A2
MOV bit, C	Move carry to direct bit	2	4	92

BRANCHING				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ACALL addr 11	Absolute jump to subroutine	2	4	11-F1
LCALL addr 16	Long jump to subroutine	3	4	12
RET	Return from subroutine	1	4	22
RETI	Return from interrupt	1	4	32
AJMP addr 11	Absolute jump unconditional	2	4	01-E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	4	80
JC rel	Jump on carry=1	2	4	40
JNC rel	Jump on carry=0	2	4	50
JB bit, rel	Jump on direct bit=1	3	4	20
JNB bit, rel	Jump on direct bit=0	3	4	30
JBC bit, rel	Jump on direct bit=1 and clear	3	4	10
JMP @A+DPTR	Jump indirect relative DPTR	1	4	73
JZ rel	Jump on accumulator=0	2	4	60
JNZ rel	Jump on accumulator≠0	2	4	70
CJNE A, dir,rel	Compare A,direct, jump not equal relative	3	4	B5
CJNE A, #data, rel	Compare A,immediate, jump not equal relative	3	4	B4
CJNE Rn, #data, rel	Compare register,immediate, jump not equal relative	3	4	B8-BF
CJNE @Ri, #data, rel	Compare indirect,immediate, jump not equal relative	3	4	B6-B7
DJNZ Rn, rel	Decrement register, jump not zero relative	2	4	D8-DF
DJNZ dir, rel	Decrement direct byte, jump not zero relative	3	4	D5

MISCELLANEOUS				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
NOP	No operation	1	2	00

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11-F1 (for example), are used for absolute jumps and calls with the top 3 bits of the code being used to store the top three bits of the destination address.

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (T_A=25°C)

Parameter	Rating	Unit
Supply voltage	V_{SS} –0.3 ~ V_{SS} +5.5	V
Input voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output current high per 1 PIN	–25	mA
Output current high per all PIN	–80	
Output current low per 1 PIN	+30	
Output current low per all PIN	+150	
Maximum Operating Voltage	5.5	V
Operating temperature	–40 ~ +85	°C
Storage temperature	–65 ~ +150	

2. DC Characteristics (T_A=25°C, V_{CC}=1.7V ~ 5.5V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Operating Voltage	V_{CC}	Fast mode, F_{SYSCLK}=16.5888 MHz		3.2	–	5.5	V
		Fast mode, F_{SYSCLK}=8.2944 MHz		2.4	–	5.5	
		Fast mode, F_{SYSCLK}=4.1472 MHz		2.4	–	5.5	
		Fast mode, F_{SYSCLK}=1.0368 MHz		2.4	–	5.5	
		Slow mode, SRC		1.7	–	5.5	
Input High Voltage	V_{IH}	All Input	V_{CC}=5V	0.6V_{CC}	–	–	V
			V_{CC}=3V	0.6V_{CC}	–	–	
Input Low Voltage	V_{IL}	All Input	V_{CC}=5V	–	–	0.2V_{CC}	V
			V_{CC}=3V	–	–	0.2V_{CC}	
I/O Port Source Current	I_{OH}	All Output	V_{CC}=5V V_{OH}=0.9V_{CC}	6	12	–	mA
			V_{CC}=3V V_{OH}=0.9V_{CC}	2	4	–	
I/O Port Sink Current	I_{OL}	All Output	V_{CC}=5V V_{OL}=0.1V_{CC}	20	40	–	mA
			V_{CC}=3V V_{OL}=0.1V_{CC}	8	16	–	
Input Leakage Current (pin high)	I_{ILH}	All Input	V_{in}=V_{CC}	–	–	1	µA
Input Leakage Current (pin low)	I_{ILL}	All Input	V_{in}=0V	–	–	–1	

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply Current	I_{CC}	Fast, V_{CC}=5V LVR enable	FRC=16.5888 MHz	–	9.0	–	mA
			FRC=8.2944 MHz	–	6.3	–	
			FRC=4.1472 MHz	–	5.0	–	
		Fast, V_{CC}=3V LVR enable	FRC=8.2944 MHz	–	4.1	–	
			FRC=4.1472 MHz	–	3.4	–	
		Slow, V_{CC}=5V LVR enable	SRC=80 KHz	–	2.6	–	
		Slow, V_{CC}=3V LVR enable	SRC=80 KHz	–	2.0	–	
		Idle, V_{CC}=5V PWRSAV=0	SRC=80 KHz	–	76	–	µA
		Idle, V_{CC}=3V PWRSAV=0	SRC=80 KHz	–	58	–	
		Idle, V_{CC}=5V PWRSAV=1	SRC=80 KHz	–	24	–	
		Idle, V_{CC}=3V PWRSAV=1	SRC=80 KHz	–	11	–	
		Stop, V_{CC}=5V	PWRSAV=0	–	52	–	
			PWRSAV=1	–	–	0.1	
		Stop, V_{CC}=3V	PWRSAV=0	–	47	–	
			PWRSAV=1	–	–	0.1	
System Clock Frequency	F_{SYSCLK}	V_{CC}>LVR_{th}	V_{CC}=4.3V	–	–	16.5888	MHz
			V_{CC}=3.8V	–	–	8.2944	
			V_{CC}=3.2V	–	–	8.2944	
			V_{CC}=2.7V	–	–	8.2944	
LVR Reference Voltage	V_{LVR}	T_A=25°C		–	4.3	–	V
				–	3.8	–	
				–	3.2	–	
				–	2.7	–	
LVR Hysteresis Voltage	V_{HYST}	T_A=25°C		–	±0.1	–	V
Low Voltage Detection time	t_{LVR}	T_A=25°C		100	–	–	µs
Pull-Up Resistor	R_P	V_{IN}=0V	V_{CC}=5V	–	30	–	KΩ
			V_{CC}=3V		60		

3. Clock Timing (T_A= –40°C ~ +85°C, V_{CC}=3.0V ~ 5.5V)

Parameter	Conditions	Min.	Typ.	Max.	Unit
FRC Frequency	25°C, V_{CC}=5.0V	–1%	16.5888	+1%	MHz
	–20°C~ 50°C, V_{CC}=5.0V	–1.5%	16.5888	+1.5%	
	–40°C ~ 85°C, V_{CC}=3.0 ~ 5.5V	–6%	16.5888	+3.0%	

4. Reset Timing Characteristics (T_A= –40°C ~ +85°C, V_{CC}=3.0V ~ 5.0V)

Parameter	Conditions	Min.	Typ.	Max.	Unit
RESET Input Low width	Input V_{CC}=5.0V ±10 %	30	–	–	µs
WDT wakeup time	V_{CC}=5.0V, WDTPSC=11	–	53	–	ms
	V_{CC}=3.0V, WDTPSC=11	–	58	–	

5. ADC Electrical Characteristics (T_A=25°C, V_{CC}=3.0V ~ 5.5V, V_{SS}=0V)

Parameter	Conditions		Min.	Typ.	Max.	Unit
Total Accuracy	V_{CC}=5.12V, V_{SS}=0V		–	±2.5	±4	LSB
Integral Non-Linearity			–	±3.2	±5	
Max Input Clock (f_{ADC})	Source impedance (Rs < 10K omh)		–	–	2	MHz
	Source impedance (Rs < 20K omh)		–	–	1	
	Source impedance (Rs < 50K omh)		–	–	0.5	
	Source is VBG (ADCHS=b)		–	–	1.2	
Conversion Time	F_{ADC}=1MHz		–	50	–	µs
Bandgap Reference Voltage (V_{BG})	–	V_{CC}=2.5V~5.5V 25°C	–1.2%	1.22	+1.2%	V
		V_{CC}=2.5V~5.5V –40°C ~ 85°C	–1.8%	1.22	+1.8%	
Input Voltage	–		V_{SS}	–	V_{CC}	V

Note: also refer to AP-TM52XXXXX_05S for using ADC to trim BandGap.

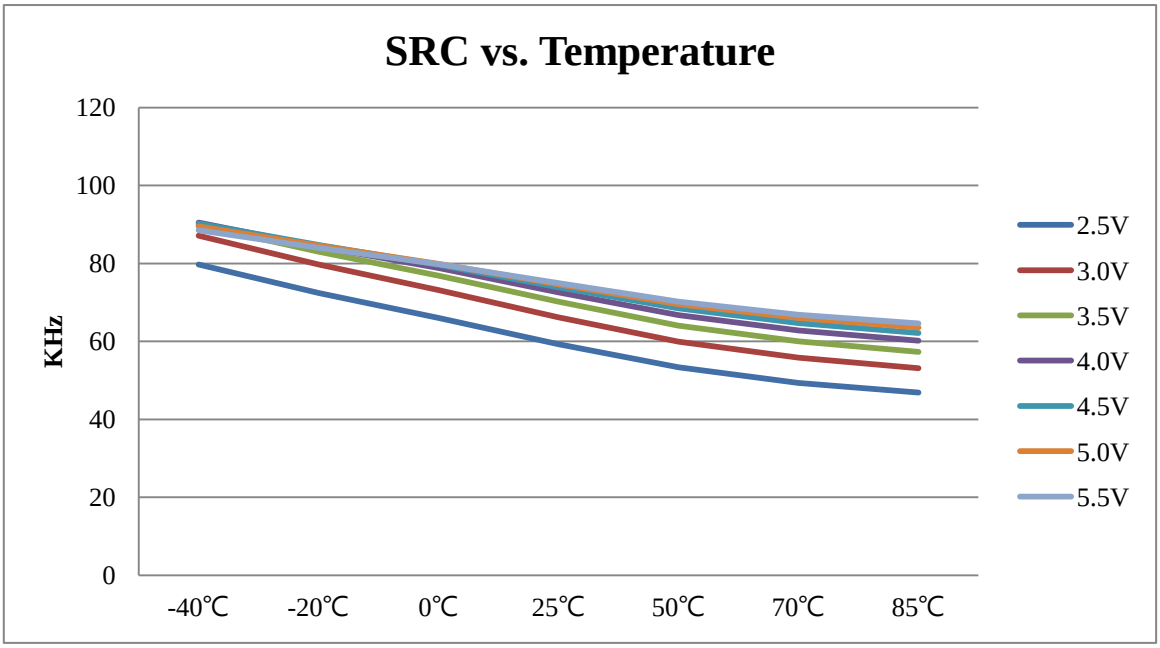
6. OPA Characteristics (T_A=25°C, V_{CC}=2.2V ~ 5.5V, R_L=1MΩ, C_L=100pf)

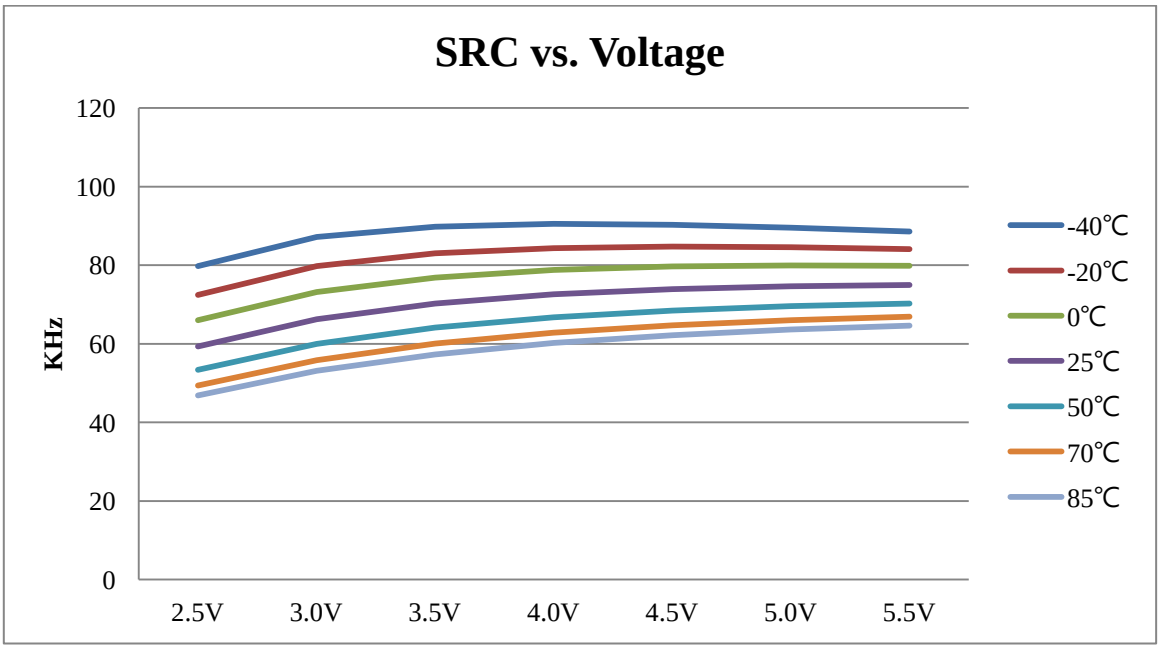
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage	–	2.2	–	5.5	V
Vcm	Input Common Voltage	–	0	–	V_{CC} –1.22	V
V_{OS}	Input Offset Voltage	V_O=2.0V after calibration	–2	–	2	mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}	V_O =2.0V	–	–	5	µV/°C
A_{VOL}	Open Loop Voltage Gain	R_L = 1 MΩ C_L = 100pF Vi = 0.1 to 4V V_O = 1 to 4V	–	90	–	dB
GBW	Gain Band Width Product	R_L = 1MΩ C_L = 100pF	–	2.1	–	MHz
CMRR	Common Mode Rejection Ratio	V_O =2.0V	–	80	–	dB
PSRR	Power Supply Rejection Ratio	V_O =2.0V	–	80	–	dB
I_{CC}	Supply Current Per Single Amplifier	A_V = 1 V_O = 2.0V No load	–	300	–	uA
SR	Slew Rate at Unity Gain	No load	–	2	–	V/µs
Φm	Phase Margin at Unity Gain	R_L =1 MΩ C_L =60 pF	–	60	–	Degree
IOH	Output Source Current	V_{IN+} -V_{IN-} ≥ 10mV V_{CC} = 5.0V	–	3	–	mA
IOL	Output Sink Current	V_{IN+} -V_{IN-} ≥ 10mV V_{CC} = 5.0V	–	3	–	mA

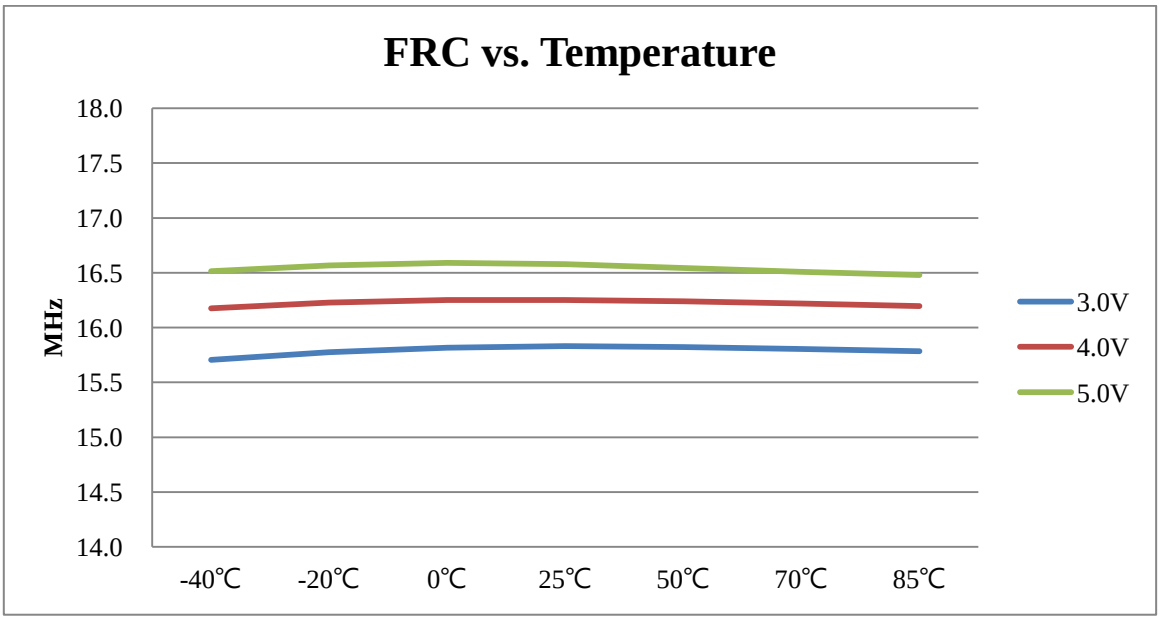
7. Analog Comparator Characteristics (T_A=25°C, V_{CC}=3.0V ~ 5.5V)

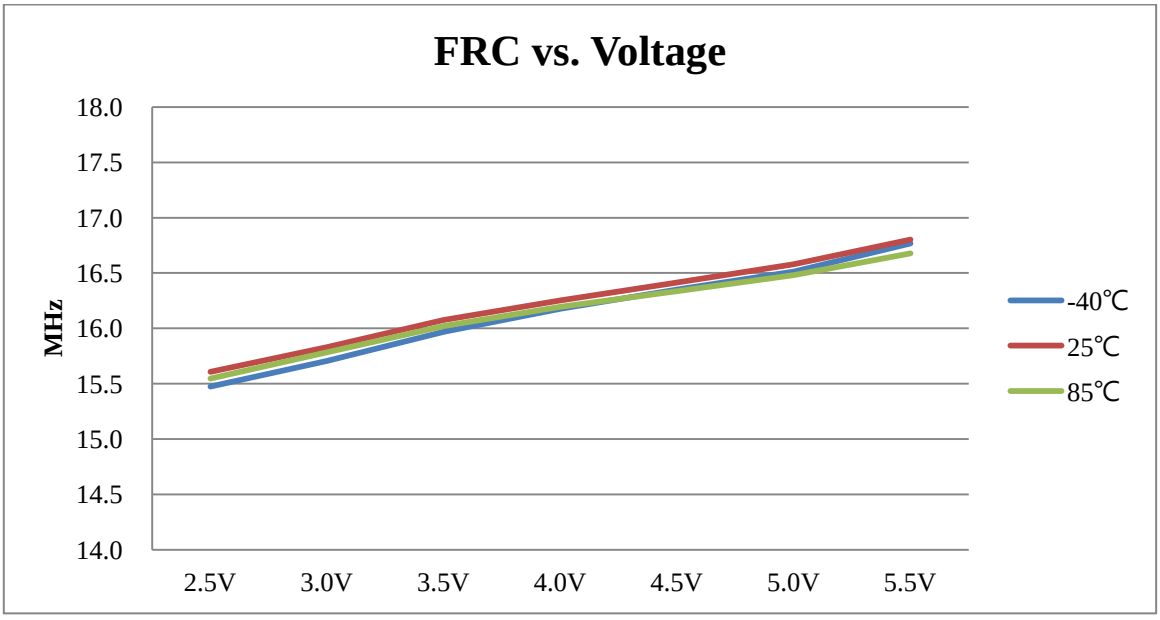
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage	–	3.0	–	5.5	V
Vcm	Input Common Voltage	–	0	–	V_{CC} –1	V
V_{OS}	Input Offset Voltage	before calibration	–15	–	15	mV
		after calibration	–2	–	2	
ΔV_{RF}	Variation of CMP2~CMP5 V_{IN+} reference voltage	T_A = –40°C ~ +85°C V_{CC} = 3.0 ~5.0V	–5	–	+5	%
t_{PD}	Response Time	Hysteresis disabled 10mV input overdrive	–	–	2	µs
V_{HYS}	Hysteresis Voltage	–	–	40	–	mV
I_{CC}	Current Consumption per Comparator	–	–	160	–	uA

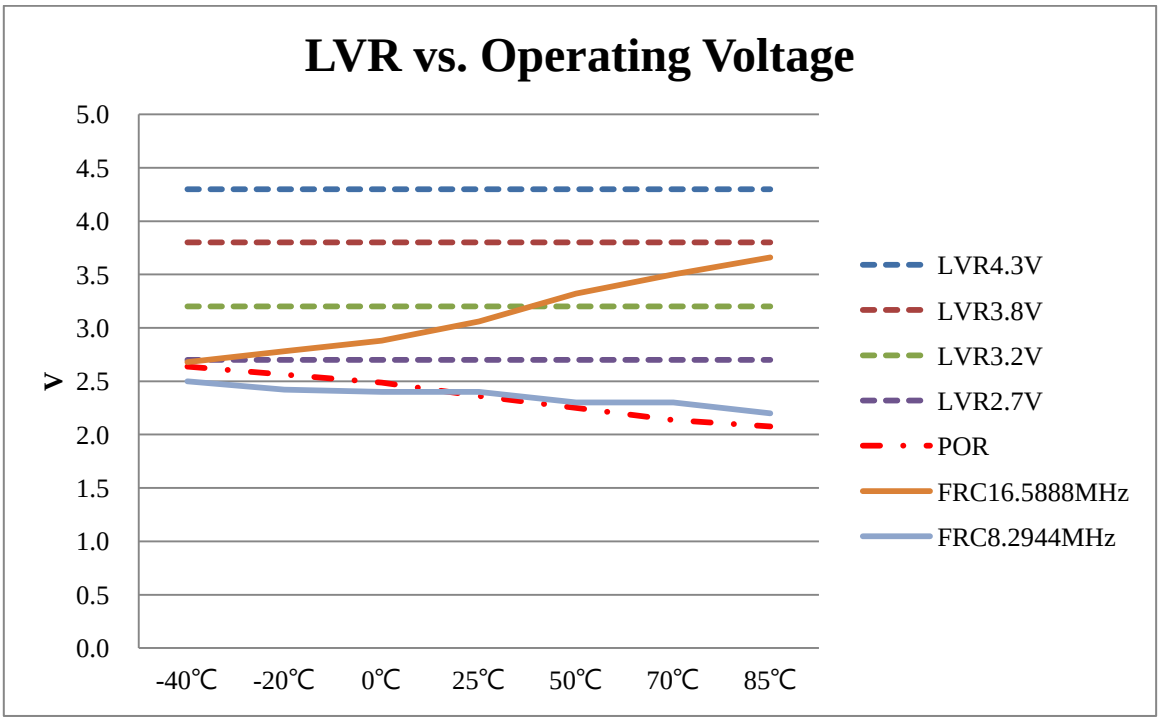
8. Characteristics Graphs

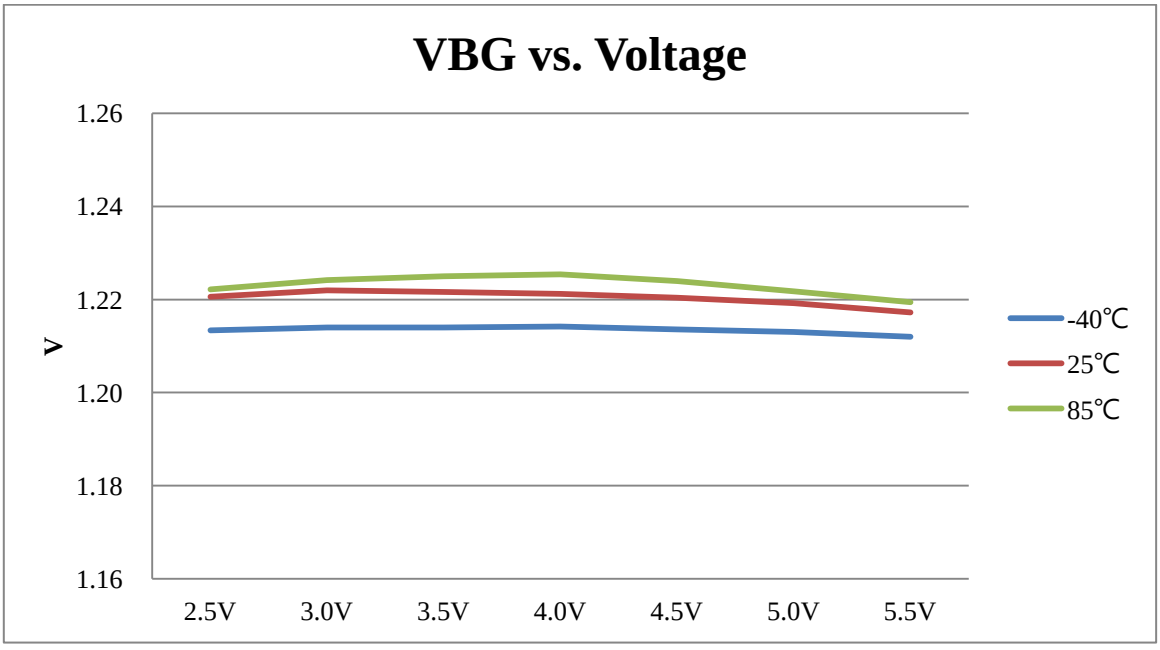





FRC vs. Temperature
18.0
17.5
17.0
16.5
16.0
15.5
15.0
14.5
14.0
MHz
-40℃
-20℃
0℃
25℃
50℃
70℃
85℃
3.0V
4.0V
5.0V


FRC vs. Voltage
18.0
17.5
17.0
16.5
16.0
15.5
15.0
14.5
14.0
MHz
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
5.5V
-40℃
25℃
85℃


LVR vs. Operating Voltage
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
V
-40℃
-20℃
0℃
25℃
50℃
70℃
85℃
LVR4.3V
LVR3.8V
LVR3.2V
LVR2.7V
POR
FRC16.5888MHz
FRC8.2944MHz


VBG vs. Voltage
1.26
1.24
1.22
1.20
1.18
1.16
V
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
5.5V
-40℃
25℃
85℃

PACKAGE INFORMATION

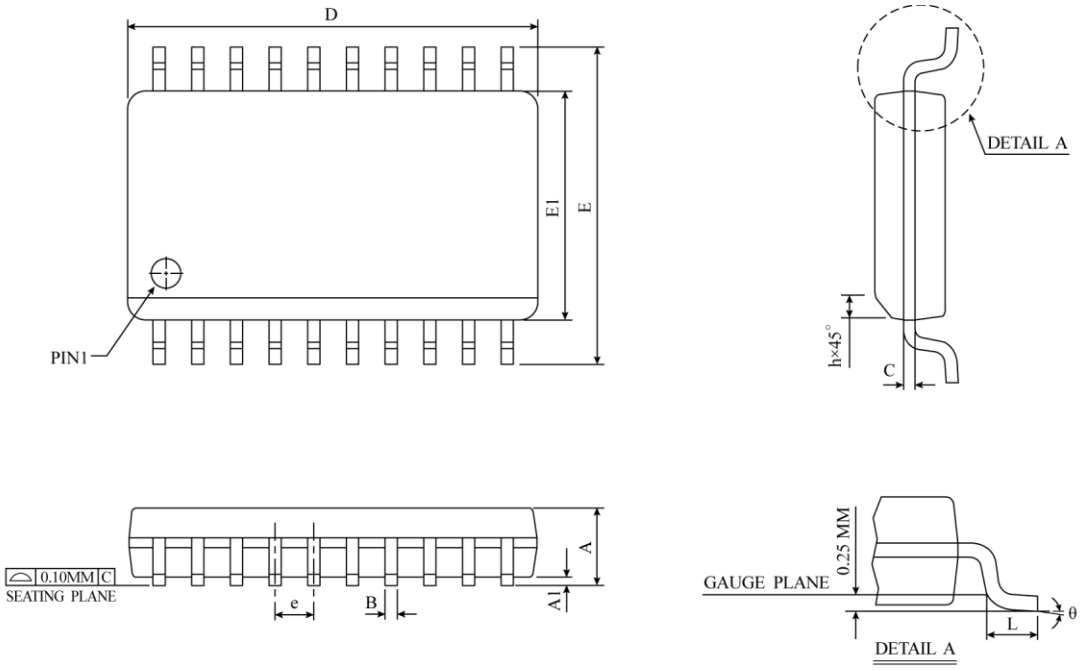
Please note that the package information provided is for reference only. Since this information is frequently updated, users can contact Sales to consult the latest package information and stocks.

Ordering Information

Ordering Number	Package
TM52F8658-MTP	Wafer/Dice blank chip
TM52F8658-COD	Wafer/Dice with code
TM52F8658-MTP-21	SOP 20-pin (300 mil)
TM52F8658-MTP-16	SOP 16-pin (150 mil)

Package Information

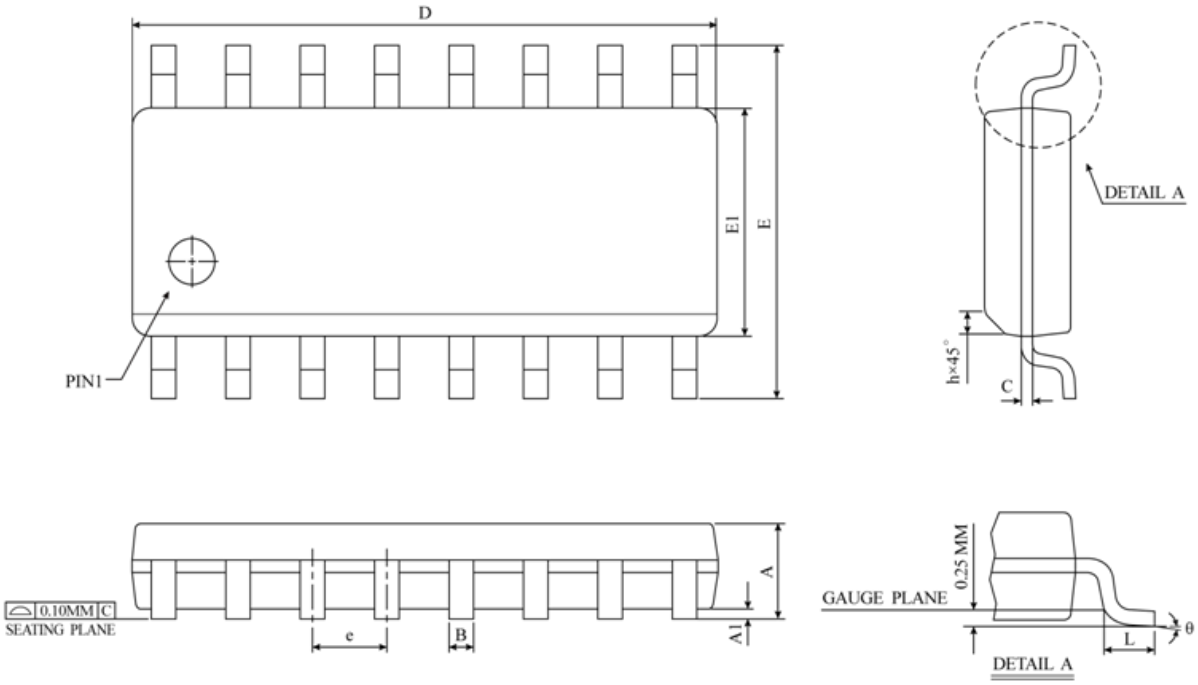
SOP 20-pin (300 mil) Package Dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	12.60	12.80	13.00	0.4961	0.5040	0.5118
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AC)					

△ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

SOP 16-pin (150 mil) Package Dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	9.80	9.90	10.00	0.3859	0.3898	0.3937
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AC)					

△ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.