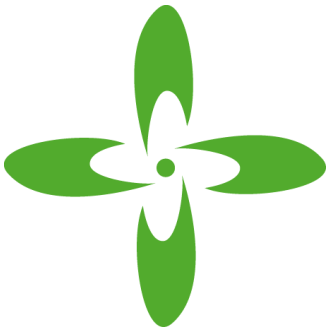

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TM52FN8273/76

TM52FN8274/78

DATA SHEET Rev 0.92

AMENDMENT HISTORY

Version	Date	Description
V0.90	Dec, 2021	New Release.
V0.91	Aug, 2022	1. Relax the operating temperature range to 105℃. 2. Raise the IAP Write voltage to 4.0V. 3. Add source current of LED pins. 4. Added the description about Halt mode. 5. Modify branch instruction cycle description in the instruction set. 6. Modify the package direction of 28-pin QFN and 20-pin QFN. 7. Disable the second programming pins P0.0 and P0.1 of the tenx proprietary writer (TWR98/TWR99). 8. Some error correction.
V0.92	Jul, 2024	1. Modify LED Matrix mode to only support 4Cx4S or 4Cx6S. 2. Remove LCDC20 and LCDC21 1/2 bias output. 3. Some error correction.

CONTENTS

TM52 F82xx FAMILY

Common Feature

CPU	MTP/Flash Program memory	RAM bytes	Dual Clock	Operation Mode	Timer0 Timer1 Timer2	UART	Real-time Timer3	LVD	LVR
Fast 8051 (2T)	4K~32K with IAP, ISP, ICP	256 ~ 1024	SXT SRC FXT FRC	Fast Slow Idle Stop Halt	8051 Standard		15-bit	16 Level	8 ~ 16 Level

Note: *IAP, ISP only for Flash type program memory*

Note: *TM52FE8273/76/74/78 and TM52FN8273/76/74/78 without LVD function*

Family Members Features

P/N	Program Memory	Data Memory	RAM Bytes	IO Pin	PWM	SAR ADC	Touch Key	LCD	LED	SPI	Others
TM52-M8254	MTP 4K Bytes	–	512	18	(8+2)-bit x2	12-bit 12-ch	–	4com	–	–	–
TM52-M8258							15-ch				
TM52-M8264	MTP 8K Bytes	–	512	18	(8+2)-bit x2	12-bit 12-ch	–	4com	–	–	–
TM52-M8268							15-ch				
TM52-F8274	Flash 8K Bytes	EEPROM 128 Bytes	1024	26	(8+2)-bit x3	12-bit 14-ch	–	8com	4Cx6S	Yes	UART2
TM52-F8278							16-ch				
TM52-F8273	Flash 16K Bytes	EEPROM 128 Bytes	1024	26	(8+2)-bit x3	12-bit 14-ch	–	8com	4Cx6S	Yes	UART2
TM52-F8276							16-ch				
TM52-FE8274	Flash 8K Bytes	EEPROM 128 Bytes	1024	26	(8+2)-bit x3	12-bit 14-ch	–	26com	4Cx6S	Yes	UART2
TM52-FE8278							15-ch				
TM52-FE8273	Flash 16K Bytes	EEPROM 128 Bytes	1024	26	(8+2)-bit x3	12-bit 14-ch	–	26com	4Cx6S	Yes	UART2
TM52-FE8276							15-ch				
TM52-FN8274	Flash 8K Bytes	EEPROM 128 Bytes	1024	26	(8+2)-bit x3	12-bit 14-ch	–	24com	4Cx6S	Yes	UART2
TM52-FN8278							19-ch				
TM52-FN8273	Flash 16K Bytes	EEPROM 128 Bytes	1024	26	(8+2)-bit x3	12-bit 14-ch	–	24com	4Cx6S	Yes	UART2
TM52-FN8276							19-ch				

P/N	Operation Voltage	Operation Current					Max. System Clock (Hz)			
		Fast FRC	Slow SRC	Idle SRC	Stop	Halt	SXT	SRC	FXT	FRC
TM52-M8254	2.3~5.5V	4.0mA	1.3mA	18μA	0.1μA	-	32K	68K	8M	12.28M/2
TM52-M8258										
TM52-M8264	2.3~5.5V	4.0mA	1.3mA	18μA	0.1μA	-	32K	68K	8M	12.28M/2
TM52-M8268										
TM52-F8274	2.3~5.5V	5.3mA	1.3mA	20μA	0.1μA	-	32K	68K	12M	12.902M
TM52-F8278										
TM52-F8273	2.3~5.5V	5.3mA	1.3mA	20μA	0.1μA	-	32K	68K	12M	12.902M
TM52-F8276										
TM52-FE8274	2.3~5.5V	5.9mA	1.8mA	20μA	0.1μA	5μA	32K	68K	16M	14.746M
TM52-FE8278										
TM52-FE8273	2.3~5.5V	5.9mA	1.8mA	20μA	0.1μA	5μA	32K	68K	16M	14.746M
TM52-FE8276										
TM52-FN8274	2.2~5.5V	8mA	2.6mA	40μA	0.4μA@5V 0.1μA@3V	23uA@5V 5.5uA@3V	32K	80K	16M	14.746M
TM52-FN8278										
TM52-FN8273	2.2~5.5V	8mA	2.6mA	40μA	0.4μA@5V 0.1μA@3V	23uA@5V 5.5uA@3V	32K	80K	16M	14.746M
TM52-FN8276										

Compare Table:

	TM52FE8276/78	TM52FE73/74	TM52FN8276/78	TM52FN73/74
ROM	Flash 16K/8K		Flash 16K/8K	
EEPROM	128 bytes		128 bytes	
IRAM	256 bytes		256 bytes	
XRAM	768 bytes		768 bytes	
GPIO	26		26	
Interrupt	12		12	
FRC	14.7456 MHz		14.7456 MHz	
SRC	68 KHz		80 KHz	
Timer	16-bit Timer0/1/2 15-bit Timer3		16-bit Timer0/1/2 15-bit Timer3	
UART	UART1 UART2 (mode1/3)		UART1 UART2 (mode1/3)	
PWM	(8+2)-bit PWM0/1/2		(8+2)-bit PWM0/1/2	
SPI	Yes		Yes	
Touch Key	12-bit TKDATA 15 channel 1 Reference key	-	14-bit TKDATA 19 channel 1 Reference key	-
ADC	12-bit ADC 14 channel ADCVREFS = V_{CC}/2.5V/3V/4V		12-bit ADC 14 channel ADCVREFS = V_{CC}/2.5V	
LCD	26 COM 1/2 bias		24 COM 1/2 bias	
LED	4C x 4S / 4C x 5S / 4C x 6S		4C x 4S / 4C x 6S	
POR	2.3V		2.2V (power on) 1.9V (power off)	
LVR	2.4V/2.7V/2.9V/3.2V 3.5V/3.8V/4.0V/4.3V		2.2V/2.5V/2.8V/3.1V 3.4V/3.7V/4.0V/4.3V	
VBG	1.22V		1.20V	
P1WKUP	P1.7~P1.0		P1.3~P1.0	
IAPTE	Disable/0.9ms/3.6ms/7.2ms		Disable/1.5ms/5.8ms/11.7ms	
WDTPSC	60ms/120ms/240ms/480ms		50ms/100ms/200ms/400ms	
EFTCON	-		Yes	

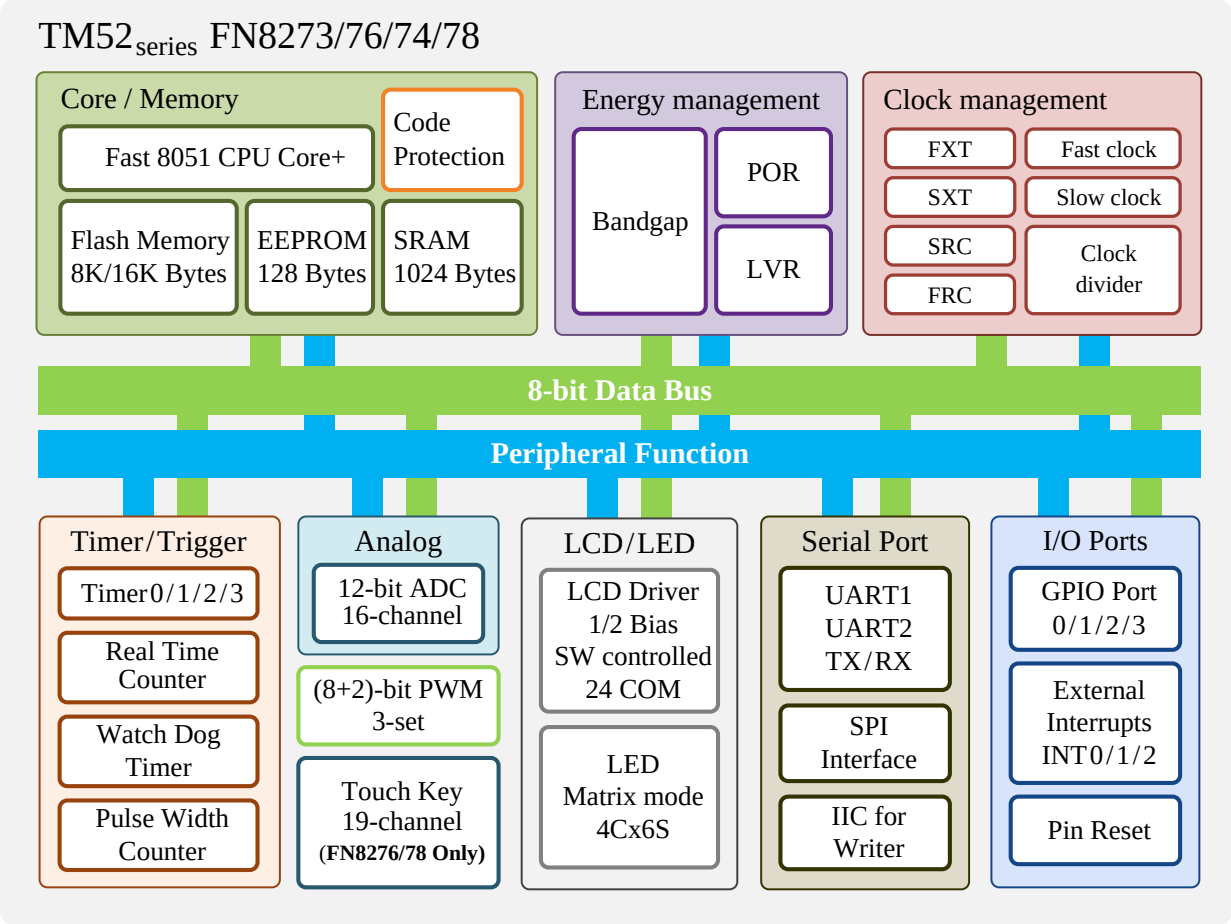
Note:
P1WKUP *(SFR 96h): pin individual Wake-up / Interrupt enable control.*
IAPTE *(SFR F7h.2~1): IAP (or EEPROM) write watchdog timer enable.*
WDTPSC *(SFR 94h.5~4): Watchdog Timer pre-scalar time select.*
EFTCON *(SFR E5h): EFT Detector related control.*

GENERAL DESCRIPTION

TM52 series FN8273/76/74/78 are versions of a new, fast 8051 architecture for an 8-bit microcontroller single chip with an instruction set fully compatible with industry standard 8051, and retains most 8051 peripheral's functional block. Typically, the **TM52** executes instructions six times faster than the standard 8051 architecture.

The **TM52-FN8273/76/74/78** provides improved performance, lower cost and fast time-to-market by integrating features on the chip, including 8K/16K Bytes Flash program memory, 128 Bytes EEPROM data memory, 1024 Bytes SRAM, Low Voltage Reset (LVR), dual clock power saving operation mode, 8051 standard UART and Timer0/1/2, real time clock Timer3, LCD/LED driver, 3 set (8+2)-bit PWMs, 14 channels 12-bit A/D Convertor, 19 channels Touch Key (FN8276/78 only) and Watch Dog Timer. It's a high reliability and low power consumption feature can be widely applied in consumer and home appliance products.

BLOCK DIAGRAM



Note: *8K Bytes Flash program memory (TM52FN8274/78)*
16K Bytes Flash program memory (TM52FN8273/76)

FEATURES

1. **Standard 8051 Instruction set, fast machine cycle**
   - Executes instructions six times faster than the standard 8051.
2. **Flash Program Memory**
   - 8K Bytes (TM52FN8274/78)
   - 16K Bytes (TM52FN8273/76)
   - Support “In Circuit Programming” (ICP) or “In System Programming” (ISP) for the Flash code
   - Byte Write “In Application Programming” (IAP) mode is convenient as Data EEPROM access
   - Code Protection Capability
   - Built-in Watchdog Timer for escape the write fail state
   - 10K erase times at least
   - 10 years data retention at least
3. **128 Bytes EEPROM Memory**
   - 50K erase times at least
   - 10 years data retention at least
4. **Total 1024 Bytes SRAM (IRAM + XRAM)**
   - 256 Bytes IRAM in the 8051 internal data memory area
   - 768 Bytes XRAM in the 8051 external data memory area (accessed by MOVX Instruction)
5. **Four System Clock type selections**
   - Fast clock from 1~16MHz Crystal (FXT)
   - Fast clock from Internal RC (FRC, 14.7456 MHz)
   - Slow clock from 32768Hz Crystal (SXT)
   - Slow clock from Internal RC (SRC, 80 KHz)
   - System Clock can be divided by 1/2/4/16 option
6. **8051 Standard Timer – Timer0/1/2**
   - 16-bit Timer0, also supports T0O clock output for Buzzer application
   - 16-bit Timer1
   - 16-bit Timer2, also supports T2O clock output for Buzzer application
7. **15-bit Timer3**
   - Clock source is Slow clock
   - Interrupt period can be clock divided by 32768/16384/8192/4096/2048/1024/512/256 option
8. **UARTs**
   - UART1, 8051 standard UART, One Wire UART option can be used for ISP or other application
   - UART2, the second UART, supports only mode1 and mode3

9. Three independent "8+2" bits PWMs with prescaler/ period-adjustment

10. SPI Interface

- Master or Slave mode selectable
- Programmable transmit bit rate
- Serial clock phase and polarity options
- MSB-first or LSB-first selectable

11. 19-Channel Touch Key (FN8276/78 only)

- Internal reference key
- Touch Key clock Auto-change

12. 12-bit ADC with 14 channels External Pin Input and 2 channels Internal Reference Voltage

- Internal Reference Voltage (V_{BG}): 1.20V±1%@V_{CC}=5V~3V, 25℃
- Internal Reference Voltage: Vcc/4
- ADC reference voltage = 2.5V / V_{CC}

13. LCD Driver

- Software controlled COM00~07, COM10~17, COM30~37 (Max. 24 pins)
- 1/2 LCD Bias

14. LED Controller/Driver

- New Matrix mode function
- Max. 10 pins (4 COM x 4 SEG or 4 COM x 6 SEG)
- COM with Dead Time
- 3groups, 8-level Brightness with smooth option
- LED hold function

15. 12 Sources, 4-level priority Interrupt

- Timer0/Timer1/Timer2/Timer3 Interrupt
- INT0/INT1 pin Falling-Edge/Low-Level Interrupt
- P1.0~P1.3 Pin Change Interrupt
- UART1/UART2 TX/RX Interrupt
- P3.7 (INT2) pin Interrupt
- ADC/Touch Key Interrupt
- SPI Interrupt

16. Pin Interrupt can Wake up CPU from Halt/Stop mode

- P3.2/P3.3 (INT0/INT1) Interrupt & Wake-up
- P3.7 (INT2) Interrupt & Wake-up
- P1.0~P1.3 pin can be defined as Interrupt & Wake-up pin (by pin change)

Note: *Chip cannot enter Halt/Stop mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0~2)*

17. Max. 26 Programmable I/O pins

- CMOS Output
- Pseudo-Open-Drain, or Open-Drain Output
- Schmitt Trigger Input
- Pin Pull-up can be Enabled or Disabled
- All pin with High sink (80mA@V_{CC}=5V，V_{OL}=0.1V_{CC})

18. Independent RC Oscillating Watch Dog Timer

- 400ms/200ms/100ms/50ms selectable WDT timeout options

19. Five types Reset

- Power on Reset
- Selectable External Pin Reset
- Selectable Watch Dog Reset
- Software Command Reset
- Selectable Low Voltage Reset

20. 8-level Low Voltage Reset

- 2.2V/2.5V/2.8V/3.1V/3.4V/3.7V/4.0V/4.3V (can be disabled)

21. Five Power Operation Modes

- Fast/Slow/Idle/Halt/Stop mode

22. Integrated 16-bit Cyclic Redundancy Check function

23. On-chip Debug/ICE interface

- Use P3.0/P3.1 pin or P0.0/P0.1 pin
- Share with ICP programming pin

24. Operating Voltage and Current

- V_{CC} = 2.2V ~ 5.5V @F_{SYSCLK}=14.7456 MHz (-40℃ ~ +105℃)
- I_{CC} = 0.1μA @Stop mode, PWRSAV=1, V_{CC}=3V
- I_{CC} = 5.5μA @Halt mode, PWRSAV=1, V_{CC}=3V
- I_{CC} = 16μA @Idle mode, PWRSAV=1, V_{CC}=3V

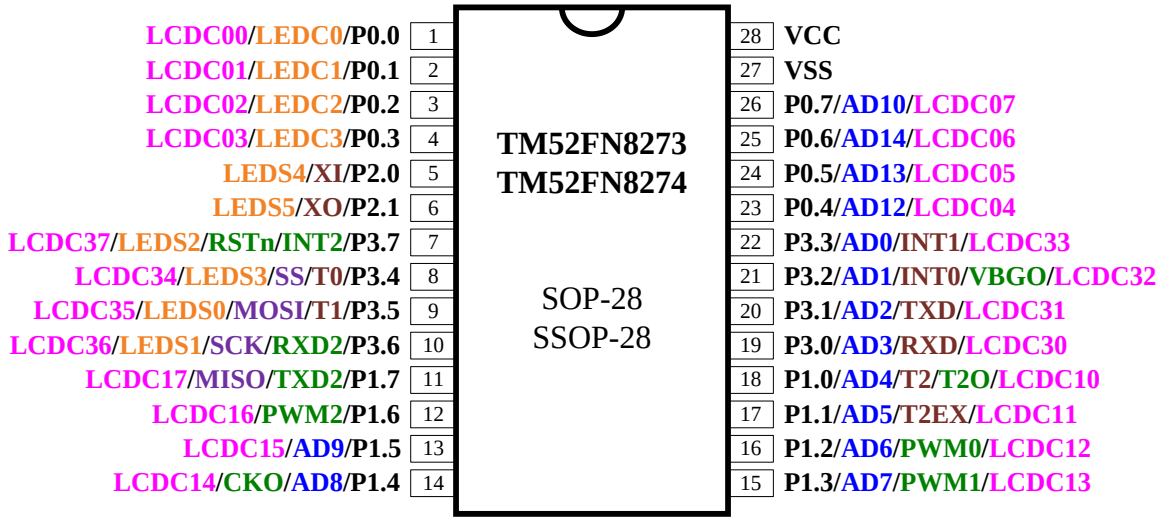
25. Operating Temperature Range

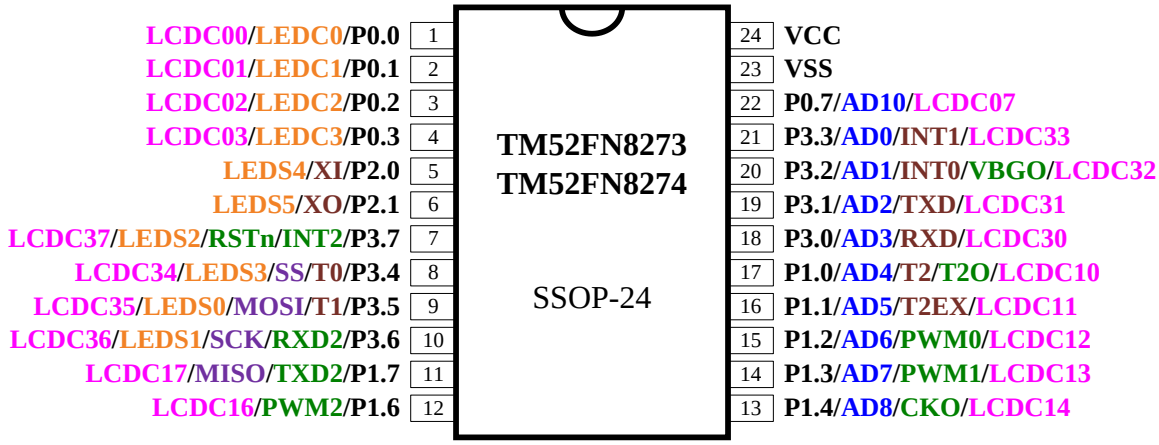
- –40℃ ~ +105℃

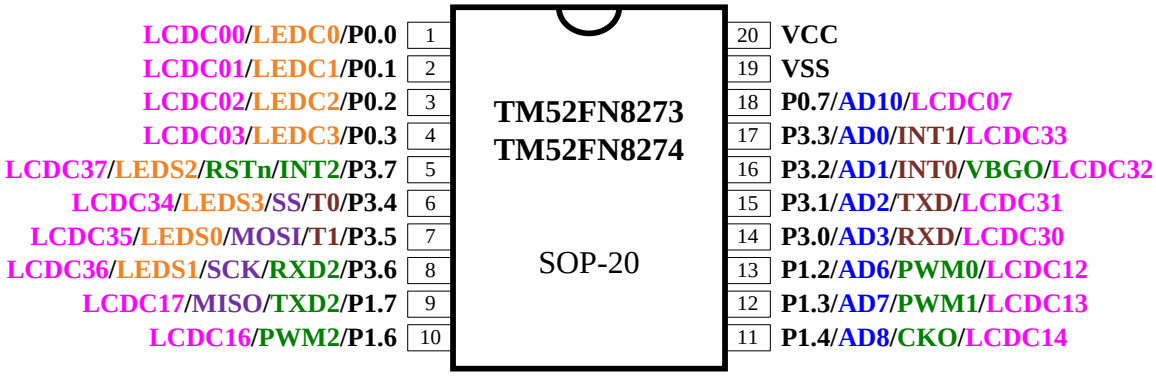
26. Package Types

- 28-pin SOP (300 mil)
- 28-pin SSOP（150 mil）
- 28-pin QFN (4x4x0.75-0.4mm)
- 24-pin SSOP (150 mil)
- 20-pin SOP (300 mil)
- 20-pin QFN (3x3x0.75-0.4mm) (L=0.25mm)
- 16-pin SOP (150 mil)

PIN ASSIGNMENT



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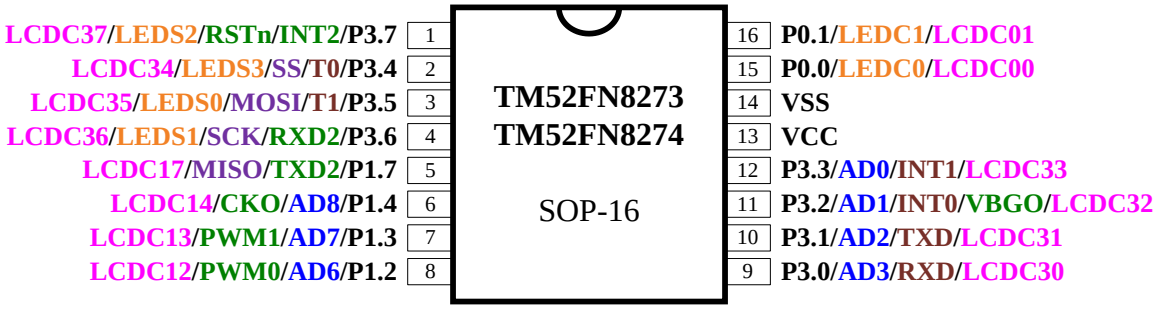
LCDC01/LEDC1/P0.1 2
LCDC02/LEDC2/P0.2 3
LCDC03/LEDC3/P0.3 4
LCDC37/LEDS2/RSTn/INT2/P3.7 5
LCDC34/LEDS3/SS/T0/P3.4 6
LCDC35/LEDS0/MOSI/T1/P3.5 7
LCDC36/LEDS1/SCK/RXD2/P3.6 8
LCDC17/MISO/TXD2/P1.7 9
LCDC16/PWM2/P1.6 10
TM52FN8273
TM52FN8274
SOP-20
20 VCC
19 VSS
18 P0.7/AD10/LCDC07
17 P3.3/AD0/INT1/LCDC33
16 P3.2/AD1/INT0/VBGO/LCDC32
15 P3.1/AD2/TXD/LCDC31
14 P3.0/AD3/RXD/LCDC30
13 P1.2/AD6/PWM0/LCDC12
12 P1.3/AD7/PWM1/LCDC13
11 P1.4/AD8/CKO/LCDC14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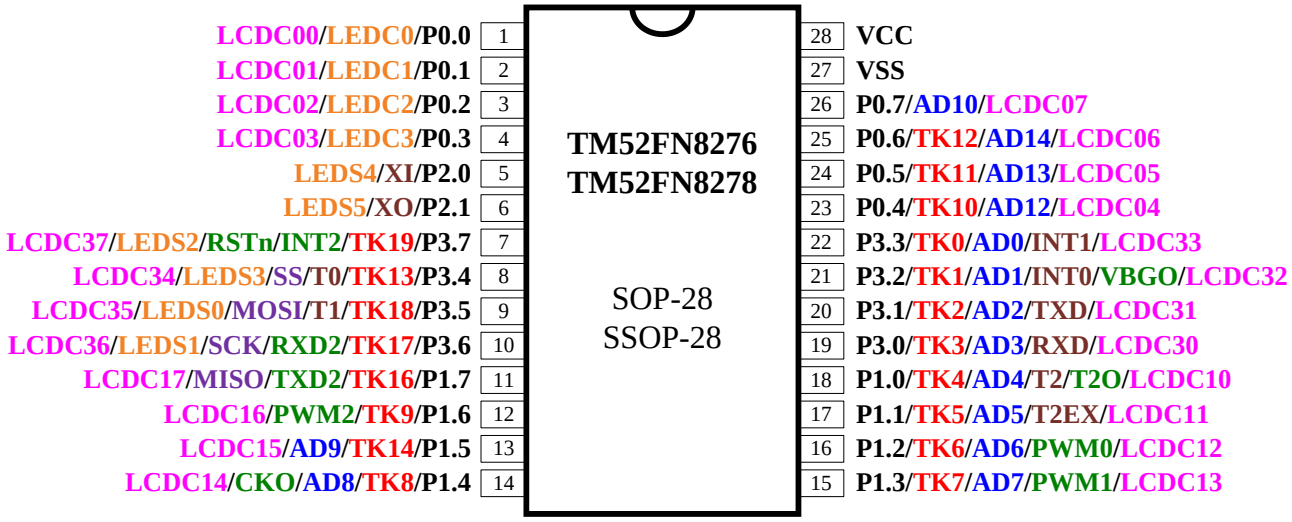
LCDC36/LEDS1/SCK/RXD2/P3.6 4
LCDC17/MISO/TXD2/P1.7 5
LCDC14/CKO/AD8/P1.4 6
LCDC13/PWM1/AD7/P1.3 7
LCDC12/PWM0/AD6/P1.2 8
TM52FN8273
TM52FN8274
SOP-16
16 P0.1/LEDC1/LCDC01
15 P0.0/LEDC0/LCDC00
14 VSS
13 VCC
12 P3.3/AD0/INT1/LCDC33
11 P3.2/AD1/INT0/VBGO/LCDC32
10 P3.1/AD2/TXD/LCDC31
9 P3.0/AD3/RXD/LCDC30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LEDS4/XI/P2.0 5
LEDS5/XO/P2.1 6
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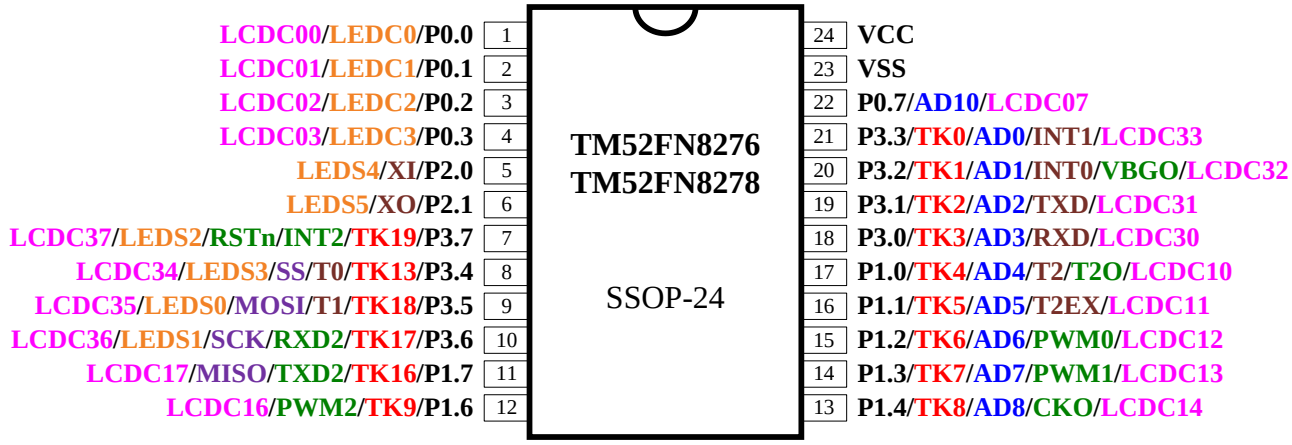
LCDC36/LEDS1/SCK/RXD2/TK17/P3.6 10
LCDC17/MISO/TXD2/TK16/P1.7 11
LCDC16/PWM2/TK9/P1.6 12
LCDC15/AD9/TK14/P1.5 13
LCDC14/CKO/AD8/TK8/P1.4 14
TM52FN8276
TM52FN8278
SOP-28
SSOP-28
28 VCC
27 VSS
26 P0.7/AD10/LCDC07
25 P0.6/TK12/AD14/LCDC06
24 P0.5/TK11/AD13/LCDC05
23 P0.4/TK10/AD12/LCDC04
22 P3.3/TK0/AD0/INT1/LCDC33
21 P3.2/TK1/AD1/INT0/VBGO/LCDC32
20 P3.1/TK2/AD2/TXD/LCDC31
19 P3.0/TK3/AD3/RXD/LCDC30
18 P1.0/TK4/AD4/T2/T2O/LCDC10
17 P1.1/TK5/AD5/T2EX/LCDC11
16 P1.2/TK6/AD6/PWM0/LCDC12
15 P1.3/TK7/AD7/PWM1/LCDC13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LCDC16/PWM2/TK9/P1.6 12
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TM52FN8278
SSOP-24
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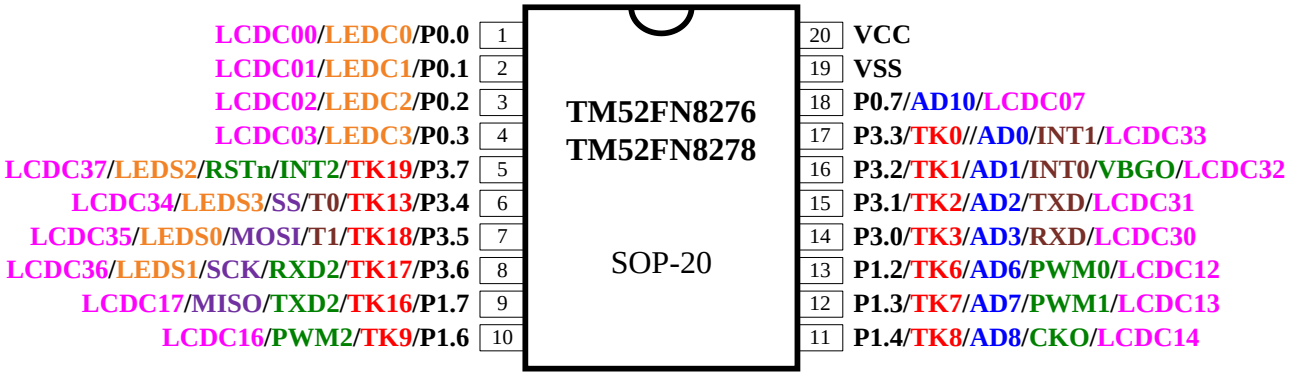
23 VSS
22 P0.7/AD10/LCDC07
21 P3.3/TK0/AD0/INT1/LCDC33
20 P3.2/TK1/AD1/INT0/VBGO/LCDC32
19 P3.1/TK2/AD2/TXD/LCDC31
18 P3.0/TK3/AD3/RXD/LCDC30
17 P1.0/TK4/AD4/T2/T2O/LCDC10
16 P1.1/TK5/AD5/T2EX/LCDC11
15 P1.2/TK6/AD6/PWM0/LCDC12
14 P1.3/TK7/AD7/PWM1/LCDC13
13 P1.4/TK8/AD8/CKO/LCDC14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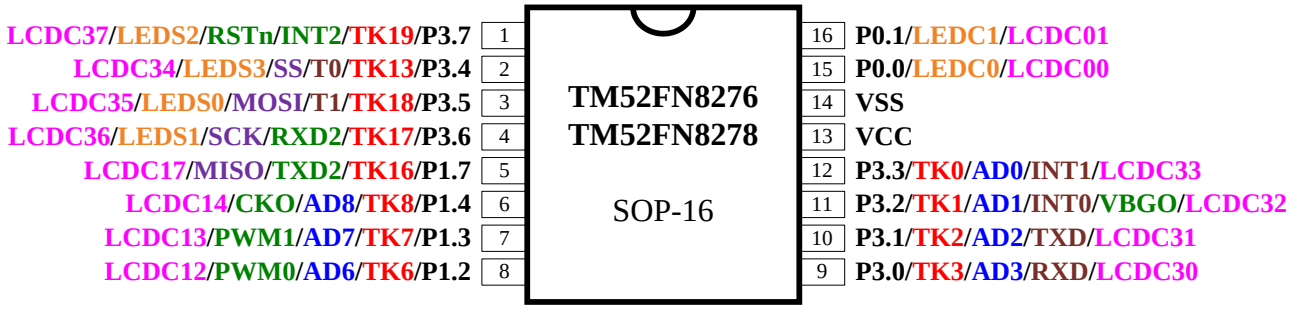
LCDC17/MISO/TXD2/TK16/P1.7 9
LCDC16/PWM2/TK9/P1.6 10
TM52FN8276
TM52FN8278
SOP-20
20 VCC
19 VSS
18 P0.7/AD10/LCDC07
17 P3.3/TK0//AD0/INT1/LCDC33
16 P3.2/TK1/AD1/INT0/VBGO/LCDC32
15 P3.1/TK2/AD2/TXD/LCDC31
14 P3.0/TK3/AD3/RXD/LCDC30
13 P1.2/TK6/AD6/PWM0/LCDC12
12 P1.3/TK7/AD7/PWM1/LCDC13
11 P1.4/TK8/AD8/CKO/LCDC14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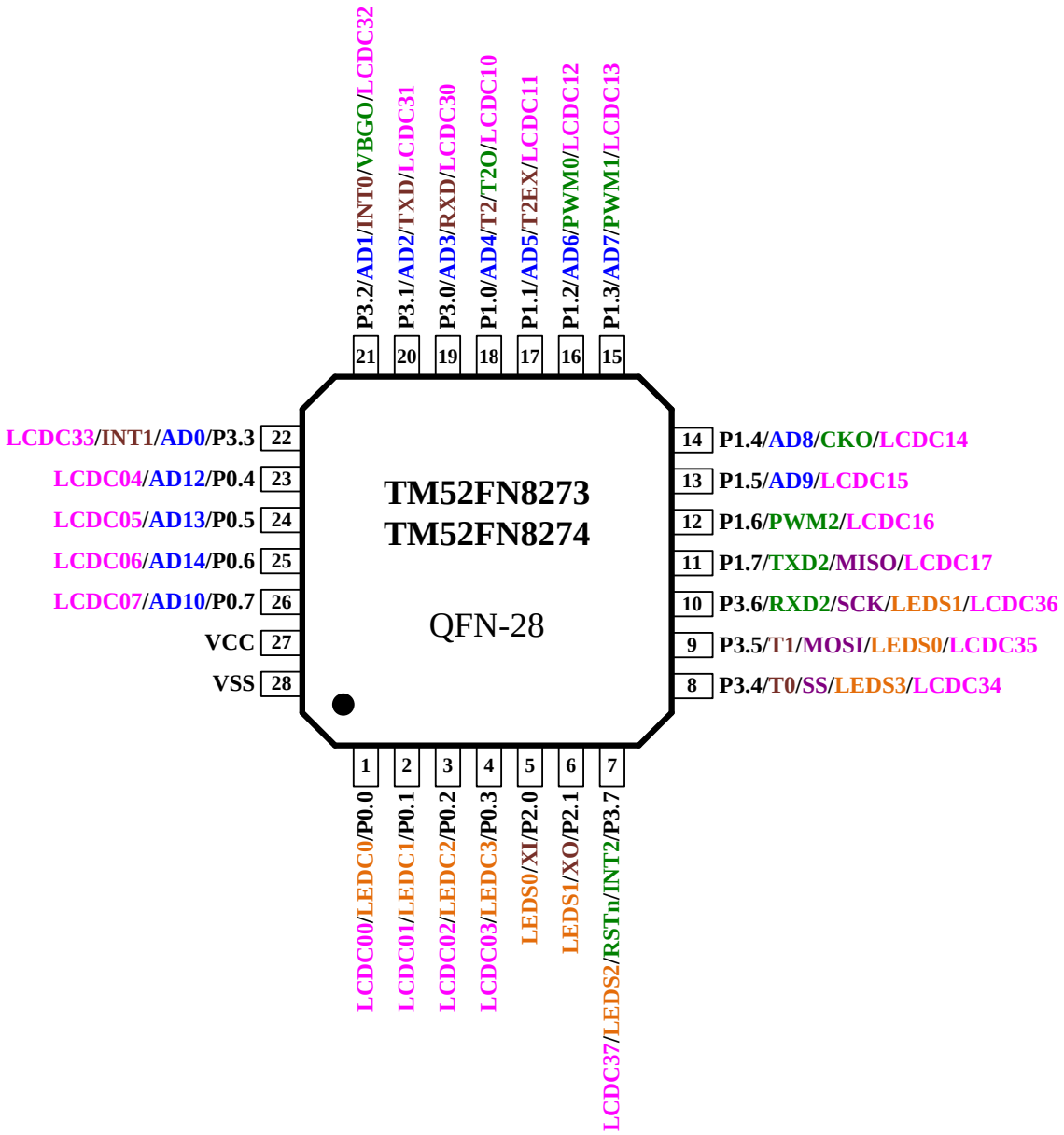
LCDC34/LEDS3/SS/T0/TK13/P3.4 2
LCDC35/LEDS0/MOSI/T1/TK18/P3.5 3
LCDC36/LEDS1/SCK/RXD2/TK17/P3.6 4
LCDC17/MISO/TXD2/TK16/P1.7 5
LCDC14/CKO/AD8/TK8/P1.4 6
LCDC13/PWM1/AD7/TK7/P1.3 7
LCDC12/PWM0/AD6/TK6/P1.2 8
TM52FN8276
TM52FN8278
SOP-16
16 P0.1/LEDC1/LCDC01
15 P0.0/LEDC0/LCDC00
14 VSS
13 VCC
12 P3.3/TK0/AD0/INT1/LCDC33
11 P3.2/TK1/AD1/INT0/VBGO/LCDC32
10 P3.1/TK2/AD2/TXD/LCDC31
9 P3.0/TK3/AD3/RXD/LCDC30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TM52FN8274
QFN-28
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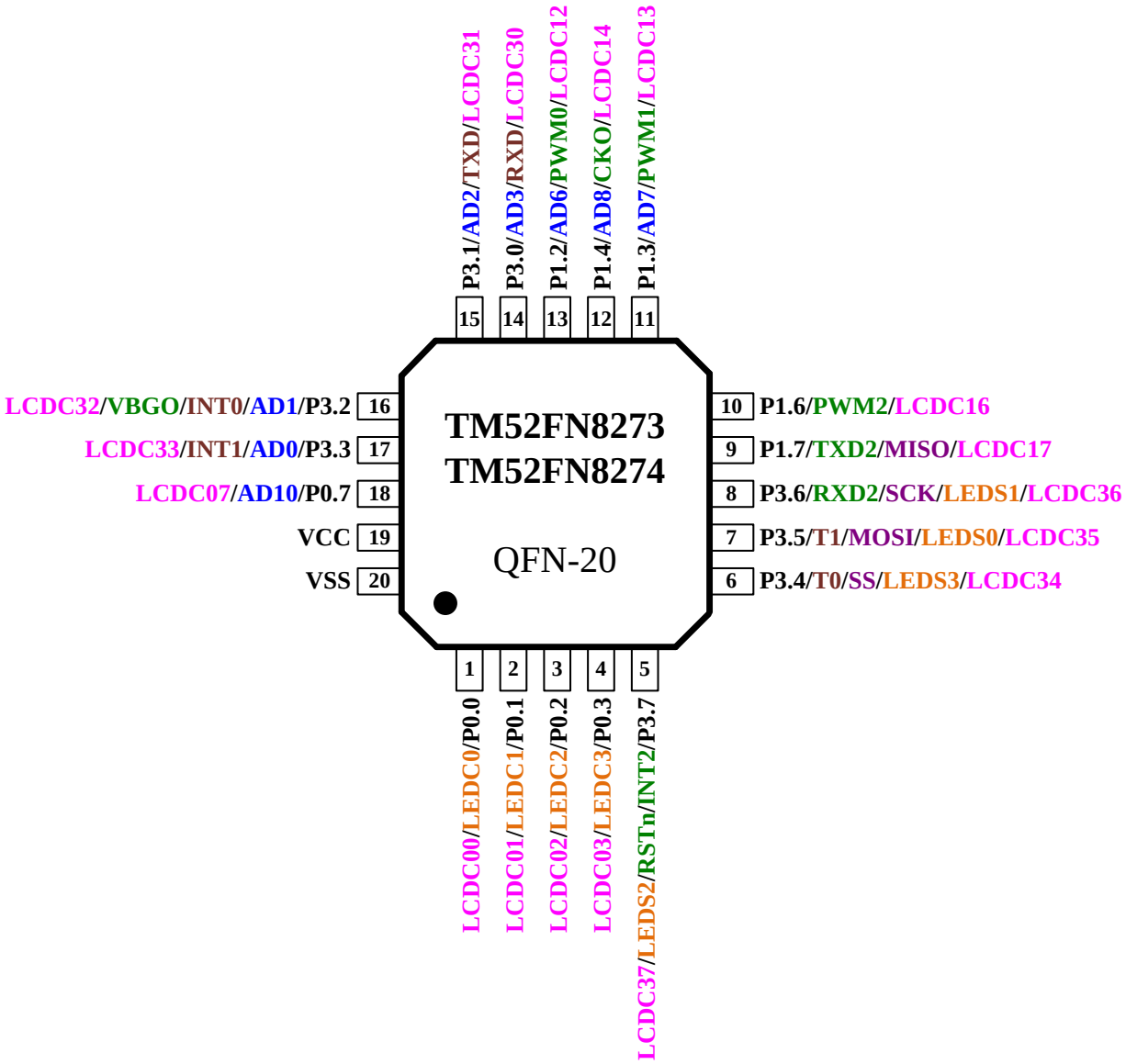
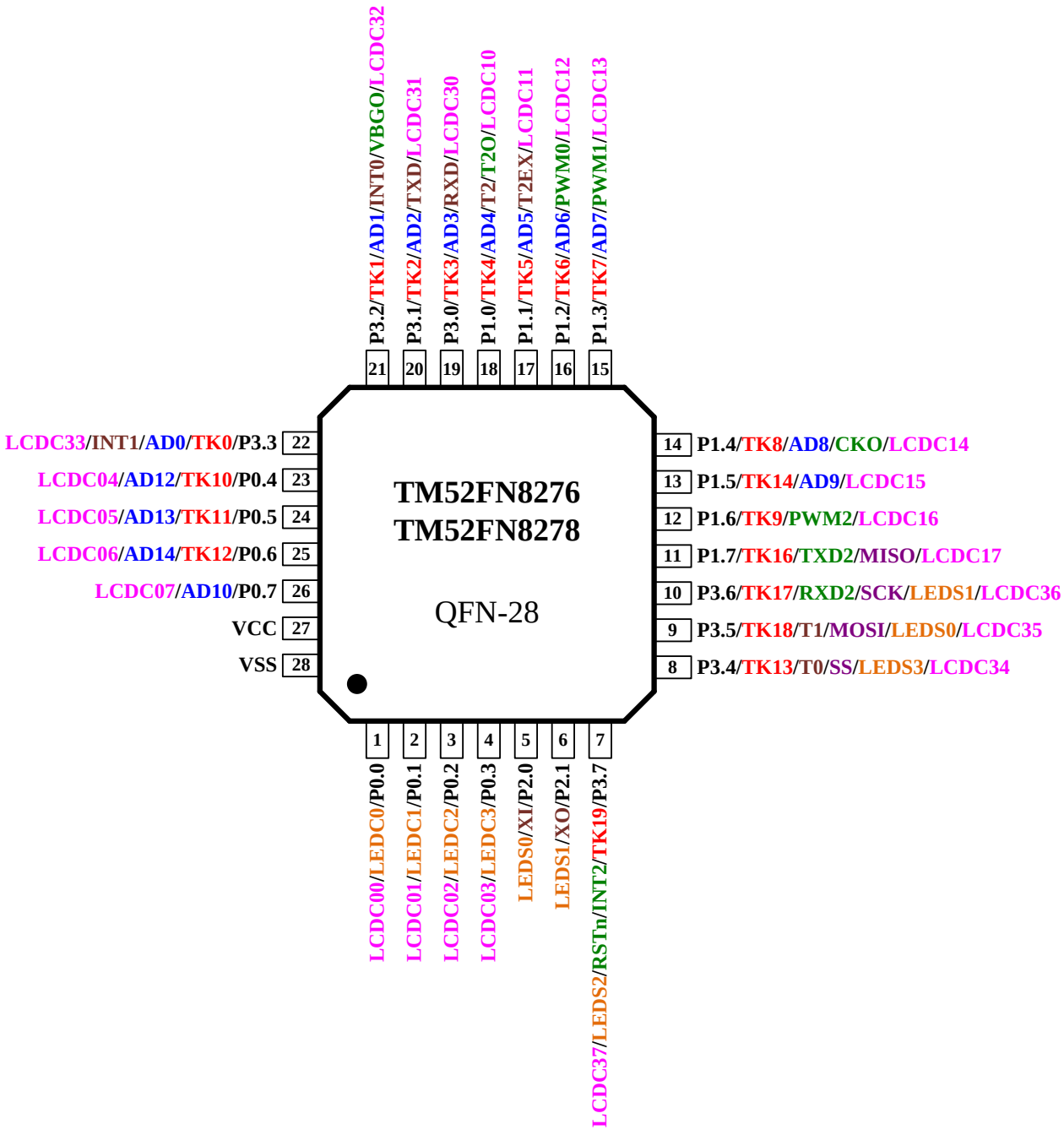
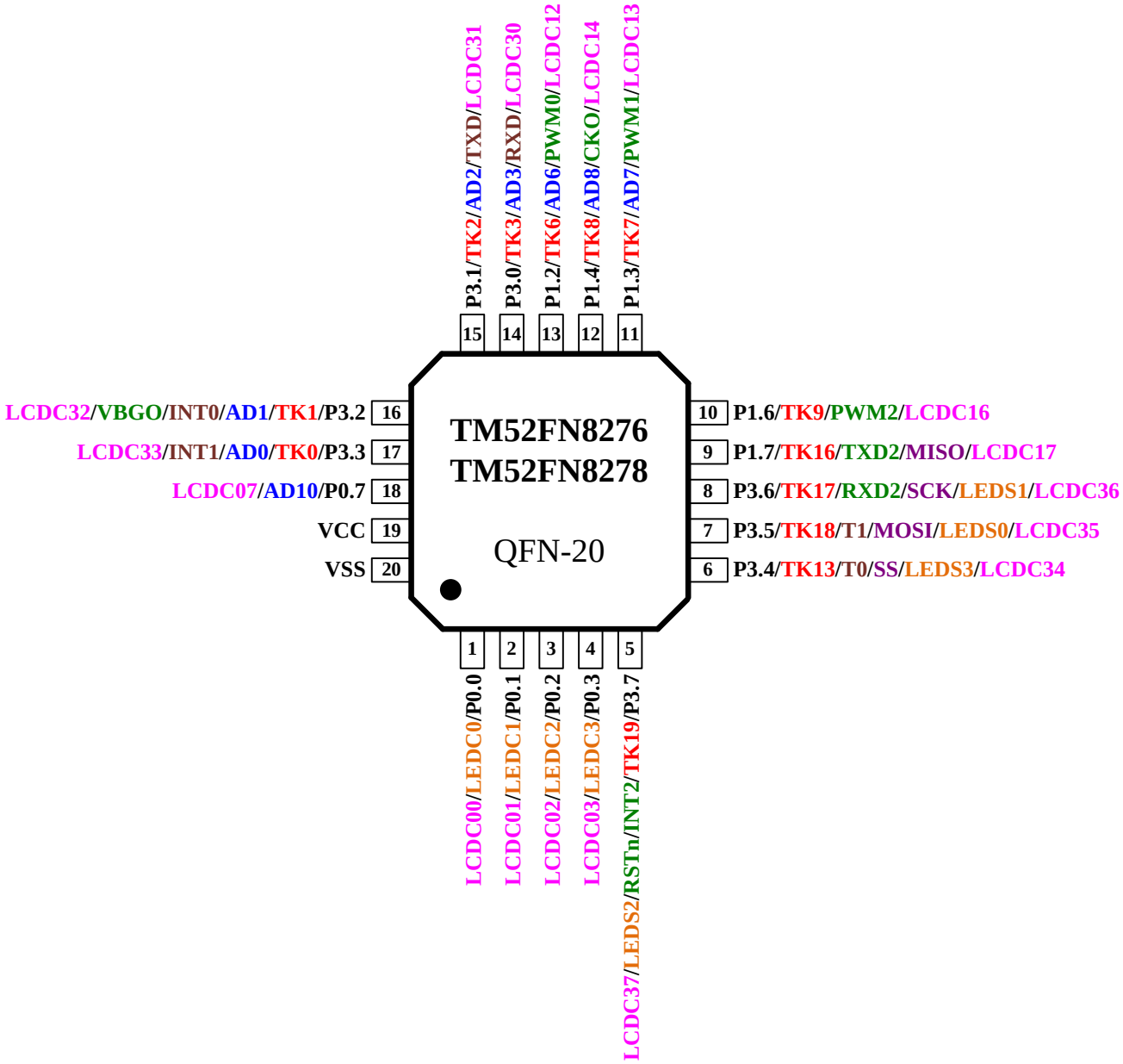
3 LCDC02/LEDC2/P0.2
4 LCDC03/LEDC3/P0.3
5 LEDS0/XI/P2.0
6 LEDS1/XO/P2.1
7 LCDC37/LEDS2/RSTn/INT2/P3.7
8 P3.4/T0/SS/LEDS3/LCDC34
9 P3.5/T1/MOSI/LEDS0/LCDC35
10 P3.6/RXD2/SCK/LEDS1/LCDC36
11 P1.7/TXD2/MISO/LCDC17
12 P1.6/PWM2/LCDC16
13 P1.5/AD9/LCDC15
14 P1.4/AD8/CKO/LCDC14
15 P1.3/AD7/PWM1/LCDC13
16 P1.2/AD6/PWM0/LCDC12
17 P1.1/AD5/T2EX/LCDC11
18 P1.0/AD4/T2/T2O/LCDC10
19 P3.0/AD3/RXD/LCDC30
20 P3.1/AD2/TXD/LCDC31
21 P3.2/AD1/INT0/VBGO/LCDC32
22 LCDC33/INT1/AD0/P3.3
23 LCDC04/AD12/P0.4
24 LCDC05/AD13/P0.5
25 LCDC06/AD14/P0.6
26 LCDC07/AD10/P0.7
27 VCC
28 VSS


TM52FN8273
TM52FN8274
QFN-20
1 LCDC00/LEDC0/P0.0
2 LCDC01/LEDC1/P0.1
3 LCDC02/LEDC2/P0.2
4 LCDC03/LEDC3/P0.3
5 LCDC37/LEDS2/RSTn/INT2/P3.7
6 P3.4/T0/SS/LEDS3/LCDC34
7 P3.5/T1/MOSI/LEDS0/LCDC35
8 P3.6/RXD2/SCK/LEDS1/LCDC36
9 P1.7/TXD2/MISO/LCDC17
10 P1.6/PWM2/LCDC16
11 P1.3/AD7/PWM1/LCDC13
12 P1.4/AD8/CKO/LCDC14
13 P1.2/AD6/PWM0/LCDC12
14 P3.0/AD3/RXD/LCDC30
15 P3.1/AD2/TXD/LCDC31
16 LCDC32/VBGO/INT0/AD1/P3.2
17 LCDC33/INT1/AD0/P3.3
18 LCDC07/AD10/P0.7
19 VCC
20 VSS


P3.2/TK1/AD1/INT0/VBGO/LCDC32
P3.1/TK2/AD2/TXD/LCDC31
P3.0/TK3/AD3/RXD/LCDC30
P1.0/TK4/AD4/T2/T2O/LCDC10
P1.1/TK5/AD5/T2EX/LCDC11
P1.2/TK6/AD6/PWM0/LCDC12
P1.3/TK7/AD7/PWM1/LCDC13
21 20 19 18 17 16 15
LCDC33/INT1/AD0/TK0/P3.3 22
LCDC04/AD12/TK10/P0.4 23
LCDC05/AD13/TK11/P0.5 24
LCDC06/AD14/TK12/P0.6 25
LCDC07/AD10/P0.7 26
VCC 27
VSS 28
TM52FN8276
TM52FN8278
QFN-28
14 P1.4/TK8/AD8/CKO/LCDC14
13 P1.5/TK14/AD9/LCDC15
12 P1.6/TK9/PWM2/LCDC16
11 P1.7/TK16/TXD2/MISO/LCDC17
10 P3.6/TK17/RXD2/SCK/LEDS1/LCDC36
9 P3.5/TK18/T1/MOSI/LEDS0/LCDC35
8 P3.4/TK13/T0/SS/LEDS3/LCDC34
1 2 3 4 5 6 7
LCDC00/LEDC0/P0.0
LCDC01/LEDC1/P0.1
LCDC02/LEDC2/P0.2
LCDC03/LEDC3/P0.3
LEDS0/XI/P2.0
LEDS1/XO/P2.1
LCDC37/LEDS2/RSTn/INT2/TK19/P3.7


P3.1/TK2/AD2/TXD/LCDC31
P3.0/TK3/AD3/RXD/LCDC30
P1.2/TK6/AD6/PWM0/LCDC12
P1.4/TK8/AD8/CKO/LCDC14
P1.3/TK7/AD7/PWM1/LCDC13
15
14
13
12
11
LCDC32/VBGO/INT0/AD1/TK1/P3.2 16
LCDC33/INT1/AD0/TK0/P3.3 17
LCDC07/AD10/P0.7 18
VCC 19
VSS 20
TM52FN8276
TM52FN8278
QFN-20
10 P1.6/TK9/PWM2/LCDC16
9 P1.7/TK16/TXD2/MISO/LCDC17
8 P3.6/TK17/RXD2/SCK/LEDS1/LCDC36
7 P3.5/TK18/T1/MOSI/LEDS0/LCDC35
6 P3.4/TK13/T0/SS/LEDS3/LCDC34
1
2
3
4
5
LCDC00/LEDC0/P0.0
LCDC01/LEDC1/P0.1
LCDC02/LEDC2/P0.2
LCDC03/LEDC3/P0.3
LCDC37/LEDS2/RSTn/INT2/TK19/P3.7

PIN DESCRIPTION

Name	In/Out	Pin Description
P0.0~P0.7	I/O	Bit-programmable I/O port for Schmitt-trigger input or CMOS push-pull output. Pull-up resistors are assignable by software.
P1.0~P1.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software. P1.0~P1.3 pin's level change can interrupt/wake up CPU from Idle/Halt/Stop mode.
P2.0~P2.1	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software.
P3.0~P3.2	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "**pseudo open drain**" output. Pull-up resistors are assignable by software.
P3.3~P3.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software.
INT0, INT1	I	External low level or falling edge Interrupt input, Idle/Halt/Stop mode wake up input.
INT2	I	External falling edge Interrupt input, Idle/Halt/Stop mode wake up input.
RXD	I/O	UART1 Mode0 transmit & receive data, Mode1/2/3 receive data
RXD2	I/O	UART2 Mode1/3 receive data
TXD	I/O	UART1 Mode0 transmit clock, Mode1/2/3 transmit data. In One Wire UART mode, this pin transmits and receives serial data.
TXD2	I/O	UART2 Mode1/3 transmit data.
T0, T1, T2	I	Timer0, Timer1, Timer2 event count pin input.
T2EX	I	Timer2 external trigger input.
T0O	O	Timer0 overflow divided by 64 output
T2O	O	Timer2 overflow divided by 2 output
CKO	O	System Clock divided by 2 output
VBGO	O	Bandgap voltage output
PWM0~PWM2	O	8+2 bit PWM output
AD0~AD10 AD12~AD14	I	ADC input
TK0~TK14 TK16~TK19	I	Touch Key input **(FN8276/78 only)**
LCDC00~LCDC07 LCDC10~LCDC17 LCDC30~LCDC37	O	LCD 1/2 bias output
LEDC0~LEDC3	O	LED common output
LEDS0~LEDS5	O	LED segment output
MISO	I/O	SPI data input for master mode, data output for slave mode
MOSI	I/O	SPI data output for master mode, data input for slave mode
SS	I	SPI active low slave select input for slave mode
SCK	I/O	SPI clock output for master or clock input for slave mode
RSTn	I	External active low reset input, Pull-up resistor is fixed enable.
XI, XO	–	Crystal/Resonator oscillator connection for System clock (FXT or SXT)
VCC, VSS	P	Power input pin and ground

PIN SUMMERY

Pin Number						Pin Name	Type	Initial State	Input			Output			Alternative Function							MISC
SOP/SSOP-28	SSOP-24	SOP-20	SOP-16	QFN-28	QFN-20				Pull-up Control	Wake up	Ext. Interrupt	CMOS P.P.	P.O.D.	O.D.	LCD/LED	ADC	Touch Key	UART	PWM	Timer	SPI	
1	1	1	15	1	1	LCDC00/LEDC0/P0.0	I/O	Hi-Z	⦿			●			●							
2	2	2	16	2	2	LCDC01/LEDC1/P0.1	I/O	Hi-Z	⦿			●			●							
3	3	3	–	3	3	LCDC02/LEDC2/P0.2	I/O	Hi-Z	⦿			●			●							
4	4	4	–	4	4	LCDC03/LEDC3/P0.3	I/O	Hi-Z	⦿			●			●							
5	5	–	–	5	–	LEDS4/XI/P2.0	I/O	Hi-Z	O			●		●	●							Crystal
6	6	–	–	6	–	LEDS5/XO/P2.1	I/O	Hi-Z	O			●		●	●							Crystal
7	7	5	1	7	5	LCDC37/LEDS2/RSTn/INT2/P3.7	I/O	Hi-Z	O	●	●	●		●	●							Reset
8	8	6	2	8	6	LCDC34/LEDS3/SS/T0/TK13/P3.4	I/O	Hi-Z	O			●		●	●		●			●	●	
9	9	7	3	9	7	LCDC35/LEDS0/MOSI/T1/P3.5	I/O	Hi-Z	O			●		●	●					●	●	
10	10	8	4	10	8	LCDC36/LEDS1/SCK/RXD2/P3.6	I/O	Hi-Z	O			●		●	●			●			●	
11	11	9	5	11	9	LCDC17/MISO/TXD2/P1.7	I/O	Hi-Z	O			●		●	●			●			●	
12	12	10	–	12	10	LCDC16/PWM2/TK9/P1.6	I/O	Hi-Z	O			●		●	●		●		●			
13	–	–	–	13	–	LCDC15/AD9/TK14/P1.5	I/O	Hi-Z	O			●		●	●	●	●					
14	13	11	6	14	**12**	LCDC14/CKO/AD8/TK8/P1.4	I/O	Hi-Z	O			●		●	●	●	●					CKO
15	14	12	7	15	**11**	LCDC13/PWM1/AD7/TK7/P1.3	I/O	Hi-Z	O	●		●		●	●	●	●		●			
16	15	13	8	16	13	LCDC12/PWM0/AD6/TK6/P1.2	I/O	Hi-Z	O	●		●		●	●	●	●		●			
17	16	–	–	17	–	LCDC11/T2EX/AD5/TK5/P1.1	I/O	Hi-Z	O	●		●		●	●	●	●			●		
18	17	–	–	18	–	LCDC10/T2O/T2/AD4/TK4/P1.0	I/O	Hi-Z	O	●		●		●	●	●	●			●		T2O
19	18	14	9	19	14	LCDC30/RXD/AD3/TK3/P3.0	I/O	Hi-Z	O			●	●		●	●	●	●				
20	19	15	10	20	15	LCDC31/TXD/AD2/TK2/P3.1	I/O	Hi-Z	O			●	●		●	●	●	●				
21	20	16	11	21	16	LCDC32/VBGO/INT0/AD1/TK1/P3.2	I/O	Hi-Z	O	●	●	●	●		●	●	●					VBGO
22	21	17	12	22	17	LCDC33/INT1/AD0/TK0/P3.3	I/O	Hi-Z	O	●	●	●		●	●	●	●					
23	–	–	–	23	–	LCDC04/AD12/TK10/P0.4	I/O	Hi-Z	⦿			●			●	●	●					
24	–	–	–	24	–	LCDC05/AD13/TK11/P0.5	I/O	Hi-Z	⦿			●			●	●	●					
25	–	–	–	25	–	LCDC06/AD14/TK12/P0.6	I/O	Hi-Z	⦿			●			●	●	●					
26	22	18	–	26	18	LCDC07/AD10/P0.7	I/O	Hi-Z	⦿			●			●	●	●					
27	23	19	14	28	20	VSS	P															
28	24	20	13	27	19	VCC	P															

Symbol:

P.P. = Push-Pull
O.D. = Open Drain
P.O.D. = Pseudo Open Drain

PS:

1. O Port1, P2.0, P2.1, Port3 these pins control Pull up resistor by operation modes
2. ⦿ Port0 control Pull up resistor while P0OE.n=0 and P0.n=1

FUNCTIONAL DESCRIPTION

1. CPU Core

In the 8051 architecture, the C programming language is used as a development platform. The TM52 device features a fast 8051 core in a highly integrated microcontroller, allowing designers to be able to achieve improved performance compared to a classic 8051 device. TM52 series microcontrollers provide a complete binary code with standard 8051 instruction set compatibility, ensuring an easy migration path to accelerate the development speed of system products. The CPU core includes an ALU, a program status word (PSW), an accumulator (ACC), a B register, a stack point (SP), DPTRs, a program counter, an instruction decoder, and core special function registers (SFRs).

1.1 Accumulator (ACC)

This register provides one of the operands for most ALU operations. Accumulators are generally referred to as A or Acc and sometimes referred to as Register A. In this document, the accumulator is represented as “A” or “ACC” including the instruction table. The accumulator, as its name suggests, is used as a general register to accumulate the intermediate results of a large number of instructions. The accumulator is the most important and frequently used register to complete arithmetic and logical operations. It holds the intermediate results of most arithmetic and logic operations and assists in data transportation.

SFR **E0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E0h.7~0 **ACC:** Accumulator

1.2 B Register (B)

The “B” register is very similar to the ACC and may hold a 1 Byte value. This register provides the second operand for multiply or divide instructions. Otherwise, it may be used as a scratch pad register. The B register is only used by two 8051 instructions, MUL and DIV. When A is to be multiplied or divided by another number, the other number is stored in B. For MUL and DIV instructions, it is necessary that the two operands are in A and B.

ex: DIV AB

When this instruction is executed, data inside A and B are divided, and the answer is stored in A.

SFR **F0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0h.7~0 **B:** B register

1.3 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the Stack Pointer.

SFR **81h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP	SP							
R/W	R/W							
Reset	0	0	0	0	0	1	1	1

81h.7~0 **SP:** Stack Point

1.4 Dual Data Pointer (DPTRs)

TM52 device has two DPTRs, which share the same SFR address. Each DPTR is 16 bits in size and consists of two registers: the DPTR high byte (DPH) and the DPTR low byte (DPL). The DPTR is used for 16-bit-address external memory accesses, for offset code byte fetches, and for offset program jumps. Setting the DPSEL control bit allows the program code to switch between the two physical DPTRs.

SFR **82h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

82h.7~0 **DPL:** Data Point low byte

SFR **83h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	DPH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

83h.7~0 **DPH:** Data Point high byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F8h.0 **DPSEL:** Active DPTR Select

1.5 Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operations. The instructions that affect the PSW are listed below.

Instruction	Flag		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		

Instruction	Flag		
	C	OV	AC
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
ORL C, /bit	X		
MOV C, bit	X		
CJNE	X		

A “0” means the flag is always cleared, a “1” means the flag is always set and an “X” means that the state of the flag depends on the result of the operation.

SFR **D0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D0h.7 **CY:** ALU carry flag

D0h.6 **AC:** ALU auxiliary carry flag

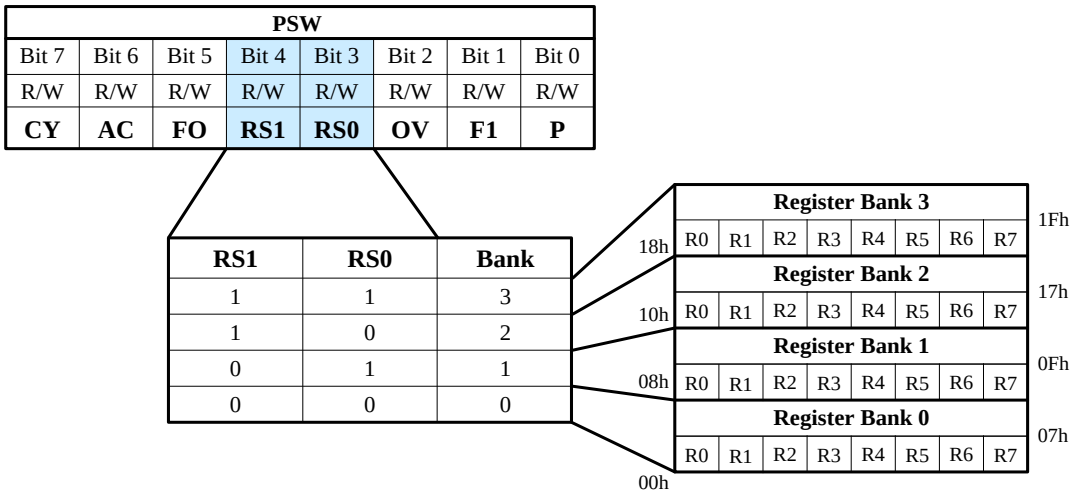
D0h.5 **F0:** General purpose user-definable flag

D0h.4~3 **RS1, RS0:** The contents of (RS1, RS0) enable the working register banks as:
- 00: Bank 0 (00h~07h)
- 01: Bank 1 (08h~0Fh)
- 10: Bank 2 (10h~17h)
- 11: Bank 3 (18h~1Fh)

D0h.2 **OV:** ALU overflow flag

D0h.1 **F1:** General purpose user-definable flag

D0h.0 **P:** Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of “one” bits in the accumulator.



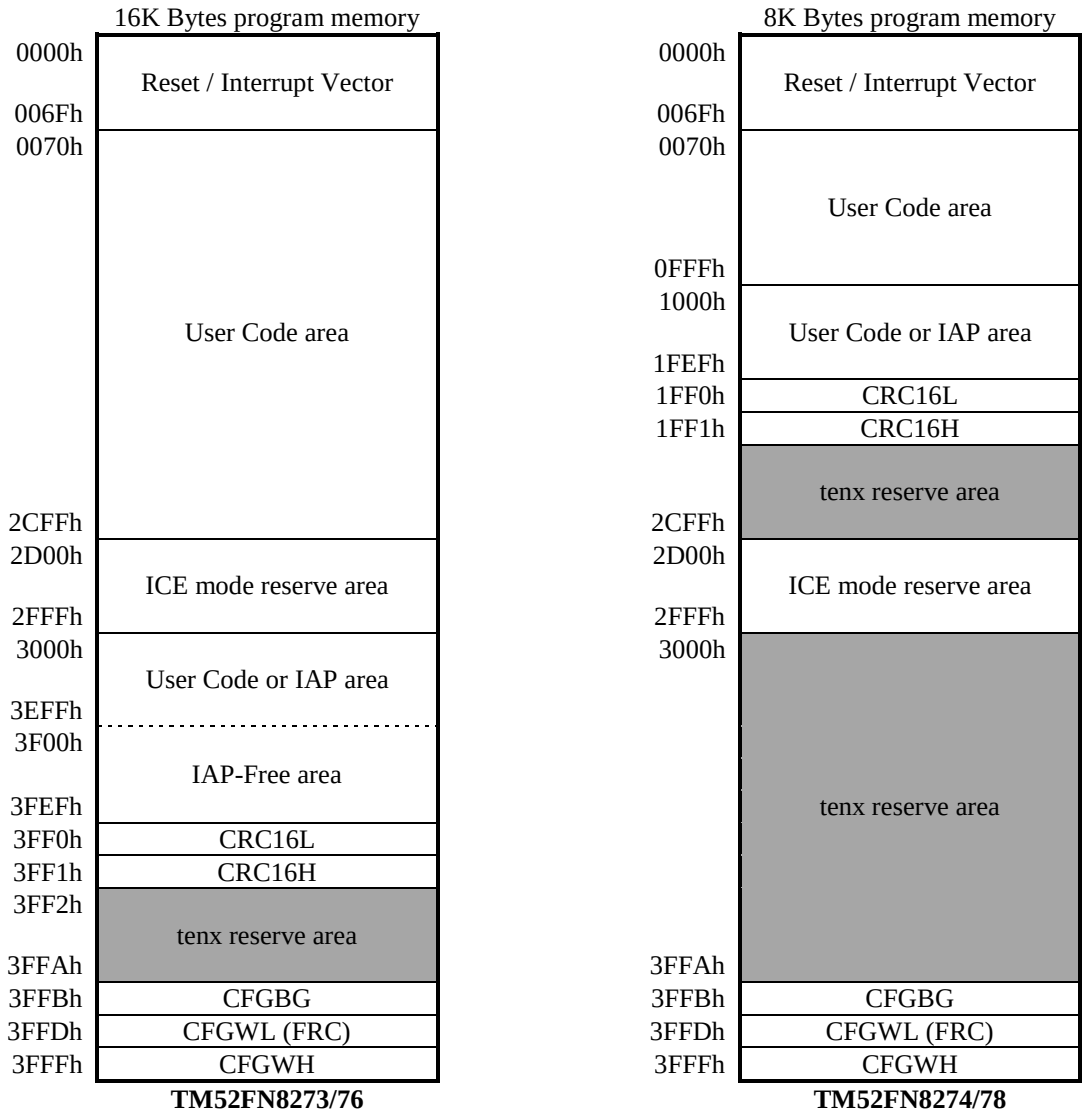
2. Memory

2.1 Program Memory

The Chip has a 16K Bytes Flash program memory for **TM52FN8273/76**, and an 8K Bytes Flash program memory for **TM52FN8274/78** which can support In Circuit Programming (ICP), In Application Programming (IAP) and In System Programming (ISP) function modes. The Flash write endurance is at least 10K cycles. The program memory address continuous space (0000h~3FFFh) is partitioned to several sectors for device operation.

2.1.1 Program Memory Functional Partition

The last 16 bytes (3FF0h~3FFFh) of program memory is defined as chip Configuration Word (CFGW), which is loaded into the device control registers upon power on reset (POR). The 0000h~006Fh is occupied by Reset/Interrupt vectors as standard 8051 definition. For **TM52FN8273/76**, the address space 3000h~3FEFh is defined as the IAP area. For **TM52FN8274/78**, the address space 1000h~1FEFh is defined as the IAP area. In the in-circuit emulation (ICE) mode, user also needs to reserve the address space 2D00h~2FFFh for ICE System communication.CRC16H/L is the reserved area of the checksum. Tenx can provide a CRC verification subroutine. The user can calculate the checksum by the CRC verification subroutine to compare with CRC16H/L and check the validity of the ROM code.



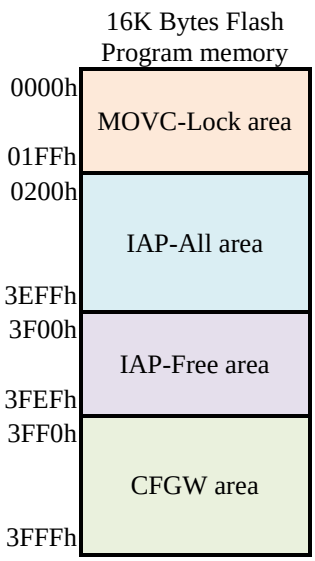
2.1.2 Flash ICP Mode

The Flash memory can be programmed by the tenx proprietary writer **(TWR99/TWR100)**, which needs at least four wires (VCC, VSS, P3.0 and P3.1) to connect to this chip. If user wants to program the Flash memory on the target circuit board (In Circuit Program, ICP), these pins must be reserved sufficient freedom to be connected to the Writer.

Writer wire number	Pin connection
4-Wire	VCC, VSS, P3.0, P3.1

2.1.3 Flash IAP Mode

The **FN8273/76/74/78** has "In Application Program" (IAP) capability, which allows software to read/write data from/to the Flash memory during CPU run time as conveniently as data EEPROM access. The IAP function is byte writable, meaning that the **FN8273/76/74/78** does not need to erase one Flash page before write. The available IAP data space is 240 Bytes after chip reset, and can be re-defined by the "MVCLOCK" and "IAPALL" control register as shown below.



Flash memory	MVCLOCK	IAPALL	MOVC Accessible	MOVX (IAP) Accessible
0000h~01FFh	1	X	No	No
	0	0	Yes	No
	0	1	Yes	Yes
0200h~3EFFh	X	0	Yes	No
	X	1	Yes	Yes
3F00h~3FEFh	X	X	Yes	Yes
3FF0h~3FF7h	X	X	Yes	Yes
3FF8h~3FFEh	X	0	Yes	No
	X	1	Yes	Yes
3FFFh	X	X	Yes	No

In IAP mode, the program Flash memory is separated into four sectors: MOVC-Lock area, IAP-All area, IAP-Free area, and CFGW area. These four sectors are regulated differently.

In the **MOVC-Lock area,** IAP read/write is limited by MVCLOCK bit, which can be set to control the accessibility of the MOVC and MOVX instructions to this area. The size of this area is 512 Bytes. The lock function is made to protect the main program code against unconsciously writing Flash memory in IAP mode. Locking or unlocking the function should be performed by the tenx TWR98/99 writing to the CFGW in Flash memory.

The **IAP-All area** is protected by the IAPALL register to prevent IAP mode from writing application data to the program area, resulting in a program code error that cannot be repaired. The size of this area is 15616 Bytes. Enabling IAPALL requires writing 65h to SFR SWCMD 97h to set the IAPALL control flag. Then, software can use MOVX instructions to write application data to flash memory from 0200h to 3EFFh. If user wants to disable IAPALL function, user can write other values to SFR SWCMD 97h to clear the IAPALL control flag. User must be careful not to overwrite program code which is already resided on the same Flash memory area.

The **IAP-Free area** has no control bit to protect. It can be used to reliably store system application data that needs to be programmed once or periodically during system operation. Other areas of Flash memory can be used to store data, but this area is usually better. The size of this area is 240 Bytes, equivalent to an EEPROM, and Flash memory can provide byte access to read and write commands. The **FN8273/76/74/78** has a physical 128 byte EEPROM memory. It has the wider writing voltage range and the better write endurance than Flash memory. It is recommended to use EEPROM memory to store application data first.

The **CFGW area** has 3 data bytes (CFGWH, CFGWL and CFGBG), which is located at the last 16 addresses of Flash memory. The CFGWH is not accessible to IAP, while the CFGWL and CFGBG can be read or written by IAP in case the IAPALL flag is set. CFGWL is copied to the SFR F6h and CFGBG is copied to the SFR F5h after power on reset, software then take over CFGWL's and CFGBG's control capability by modifying the SFR F6h and F5h.

2.1.4 IAP Mode Access Routines

Flash IAP Write is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target Flash address (0000h~3FFEh), and the ACC contains the data being written. The **FN8273/76/74/78** accepts IAP write command only when IAPWE=1. Flash IAP writing one byte requires approximately 1 ms @V_{CC}=5.0V. Meanwhile, the CPU stays in a waiting state, but all peripheral modules (Timers, LED, and others) continue running during the writing time. The software must handle the pending interrupts after an IAP write. The **FN8273/76/74/78** has a build-in IAP Time-out function for escaping write fail state. Flash IAP writing needs higher V_{CC} voltage, V_{CC}>4.0V.

Because the Program memory and the IAP data space share the same entity, a **Flash IAP Read** can be performed by the "MOVX A, @DPTR" or "MOVC" instruction as long as the target address points to the 0000h~3FFEh area. A Flash IAP read does not require extra CPU wait time.

```
  ; IAP example code (ASM)
  ; need 4.0V < VCC < 5.5V
MOV     DPTR, #3F00h        ; DPTR=3F00h=target IAP address
MOV     A, #5Ah             ; A=5Ah=target IAP write data
MOV     IAPWE, #47h         ; IAP write enable
MOV     AUX2, #02h          ; IAP Time-Out function enable
MOVX    @DPTR, A            ; Flash[3F00h] =5Ah, after IAP write
                            ; 1ms~2ms H/W writing time, CPU wait
MOV     IAPWE, #00h         ; IAP write disable, immediately after IAP write
CLR     A                   ; A=0
MOVX    A, @DPTR            ; A=5Ah
CLR     A                   ; A=0
MOVC    A, @A+DPTR          ; A=5Ah

  ; IAP example code (C)
  ; need 4.0V < VCC < 5.5V
unsigned char xdata PROM[4096] _at_ 0x2000    // 0x2000 = start address
unsigned char code CODE[4096] _at_ 0x2000    // 0x2000 = start address

IAPALL = 0x65;
IAPWE = 0x47;
PROM[0x02] = wdata;    // write data into ROM[0x2002]
IAPWE = 0x00;
IAPALL = 0x00;

rdata = CODE[0x105];    // read data from ROM[0x2105]
```

Flash **3FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE			PREAD	MVCLOCK	FRCPSC

3FFFh.1 **MVCLOCK:** If 1, the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited.

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL/SWRST							
	–						WDTO	IAPALL
R/W	W						R	R
Reset	–						0	0

97h.7~0 **IAPALL (W):** Write 65h to set IAPALL control flag; Write other value to clear IAPALL flag. It is recommended to clear it immediately after IAP access.

97h.0 **IAPALL (R):** Flag indicates Flash memory sectors can be accessed by IAP or not. This bit combines with MVCLOCK to define the accessible IAP area.

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPWE	IAPWE/EEPWE							
	IAPWE	IAPTO	EEPWE	–				
R/W	R	R	R	W				
Reset	0	0	0	–				

C9h.7~0 **IAPWE (W):** Write 47h to set IAPWE control flag; Write E2h to set EEPWE control flag; Write other value to clear IAPWE and EEPWE flag. It is recommended to clear it immediately after IAP or EEPROM write.

C9h.7 **IAPWE (R):** Flag indicates Flash memory can be written by IAP or not, 1=IAP Write enable.

C9h.6 **IAPTO (R):** IAP (or EEPROM write) Time-Out flag, Set by H/W when IAP (or EEPROM write) Time-out occurs. Cleared by H/W when IAPWE=0 (or EEPWE=0).

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	–	IAPTE		LVRPD
R/W	R/W	R/W	R/W	R/W	–	R/W		R/W
Reset	0	0	0	0	–	1	1	0

F7h.2~1 **IAPTE:** IAP (or EEPROM) write watchdog timer enable

00: Disable

01: wait 1.5ms trigger watchdog time-out flag, and escape the write fail state

10: wait 5.8ms trigger watchdog time-out flag, and escape the write fail state

11: wait 11.7ms trigger watchdog time-out flag, and escape the write fail state

2.1.5 Flash ISP Mode

The "In System Programming" (ISP) usage is similar to IAP, except the purpose is to refresh the Program code. User can use UART/SPI or other method to get new Program code from external host, then writes code as the same way as IAP. ISP operation is complicated; basically it needs to assign a Boot code area to the Flash which does not change during the ISP process.

2.2 EEPROM Memory

The **FN8273/76/74/78** contains 128 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 50K write/erase cycles.

EEPROM Memory

EE00h	EEPROM[0]
EE02h	EEPROM[1]
EE04h	. . .
EEFCh	EEPROM[126]
EEFEh	EEPROM[127]

(Only even addresses can be used, odd addresses are invalid)

The EEPROM Write usage is similar to Flash IAP mode. It is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target EEPROM address (EE00h~EEFEh, ADDR=ADDR+2), and the ACC contains the data being written. EEPROM writing requires approximately 2 ms @V_{CC}=3.0V, 1 ms @V_{CC}=5.0V. Meanwhile, the CPU stays in a waiting state, but all peripheral modules (Timers, LED, and others) continue running during the writing time. The software must handle the pending interrupts after an EEPROM write. The **FN8273/76/74/78** has a build-in EEPROM Time-out function shared with Flash IAP for escaping write fail state. EEPROM writing needs V_{CC}>3.0V.

The EEPROM Read can be performed by the "MOVX A, @DPTR" instruction as long as the target address points to the EE00h~EEFEh area. The EEPROM read does require approximately 300ns.

```
; EEPROM example code
; need 3.0V < VCC < 5.5V
MOV     DPTR, #0EE00h       ; DPTR=EE00h=target EEPROM[0] address
MOV     A, #0A5h            ; A=A5h=target EEPROM[0] write data
MOV     EEPWE, #0E2h        ; EEPROM write enable
MOV     AUX2, #004h         ; EEPROM Time-Out function enable
MOVX    @DPTR, A            ; EEPROM[0]=A5h, after EEPROM write
                            ; 1ms~2ms H/W writing time, CPU wait
MOV     EEPWE, #000h        ; EEPROM write disable, immediately after EEPROM write
CLR     A                   ; A=0
MOVX    A, @DPTR            ; A=A5h
```

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPWE	IAPWE/EEPWE							
	IAPWE	IAPTO	EEPWE	–				
R/W	R	R	R	W				
Reset	0	0	0	–				

C9h.7~0 **EEPWE (W):** Write 47h to set IAPWE control flag; Write E2h to set EEPWE control flag; Write other value to clear IAPWE and EEPWE flag. It is recommended to clear it immediately after IAP or EEPROM write.

C9h.6 **IAPTO (R):** IAP (or EEPROM write) Time-Out flag, Set by H/W when IAP (or EEPROM write) Time-out occurs. Cleared by H/W when IAPWE=0 (or EEPWE=0).

C9h.5 **EEPWE (R):** Flag indicates EEPROM memory can be written or not, 1=EEPROM Write enable.

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	–	IAPTE		LVRPD
R/W	R/W	R/W	R/W	R/W	–	R/W		R/W
Reset	0	0	0	0	–	1	1	0

F7h.2~1 **IAPTE:** IAP (or EEPROM write) watchdog timer enable

00: Disable

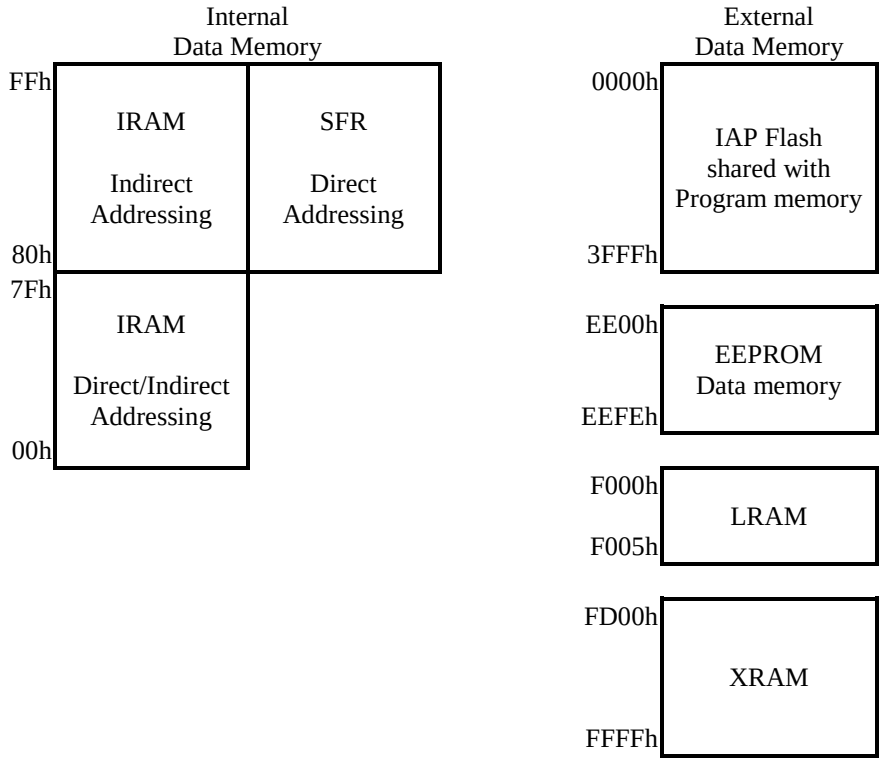
01: wait 1.5ms trigger watchdog time-out flag, and escape the write fail state

10: wait 5.8ms trigger watchdog time-out flag, and escape the write fail state

11: wait 11.7ms trigger watchdog time-out flag, and escape the write fail state

2.3 Data Memory

As the standard 8051, the Chip has both Internal and External Data Memory space. The Internal Data Memory space consists of 256 Bytes IRAM and 74 SFRs, which are accessible through a rich instruction set. The External Data Memory space consists of 768 Bytes XRAM, 6 Bytes LCD RAM, 128 Bytes EEPROM and IAP Flash, which can be only accessed by MOVX instruction.



2.3.1 IRAM

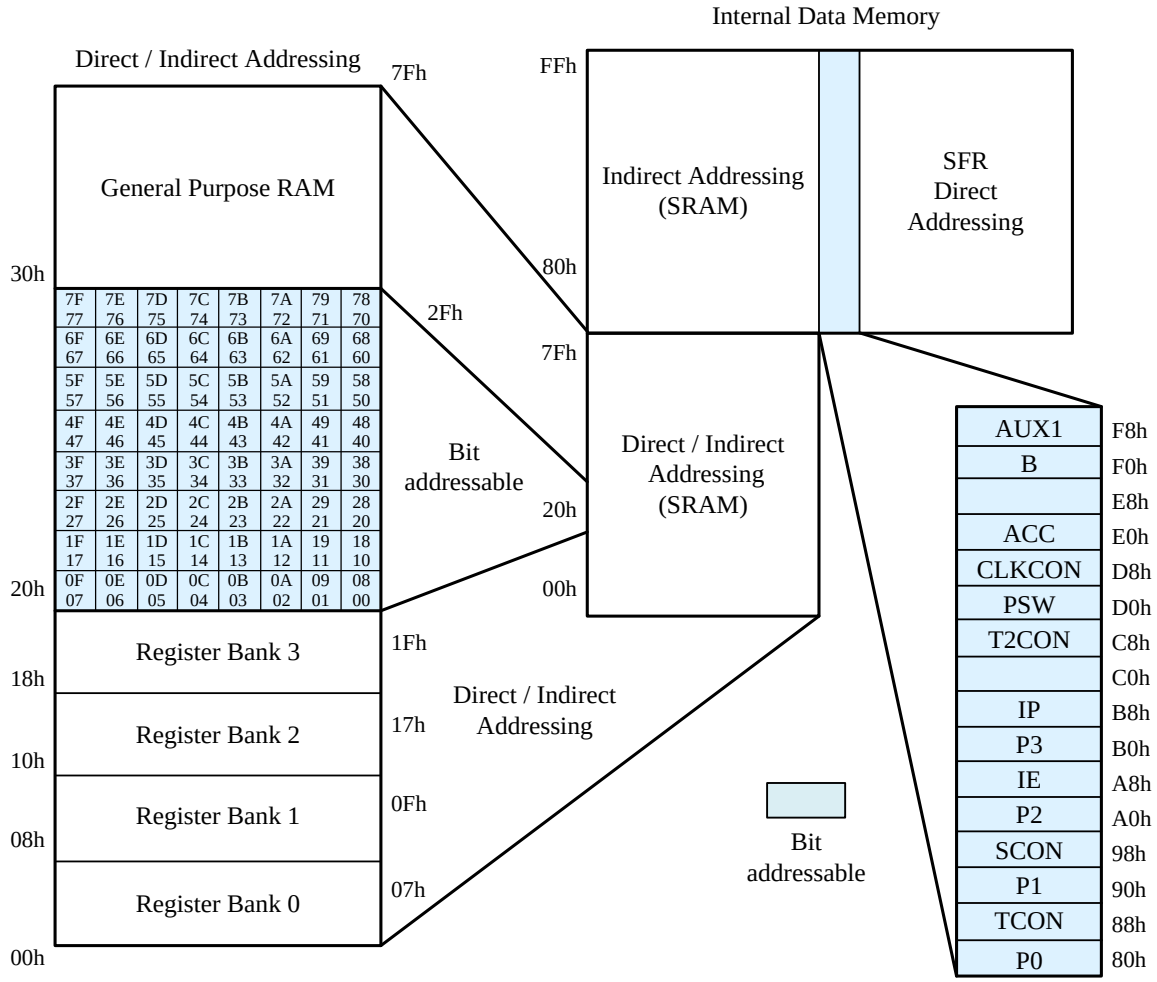
IRAM is located in the 8051 internal data memory space. The whole 256 Bytes IRAM are accessible using indirect addressing but only the lower 128 Bytes are accessible using direct addressing. There are four directly addressable register banks (switching by PSW), which occupy IRAM space from 00h to 1Fh. The address 20h to 2Fh 16 Bytes IRAM space is bit-addressable. IRAM can be used as scratch pad registers or program stack.

2.3.2 XRAM

XRAM is located in the 8051 external data memory space (address from FD00h to FFFFh). The 768 Bytes XRAM can be only accessed by “MOVX” instruction.

2.3.3 SFRs

All peripheral functional modules such as I/O ports, Timers and UART operations for the chip are accessed via Special Function Registers (SFRs). These registers occupy upper 128 Bytes of direct Data Memory space locations in the range 80h to FFh. There are 14 bit-addressable SFRs (which means that eight individual bits inside a single byte are addressable), such as ACC, B register, PSW, TCON, SCON, and others. The remaining SFRs are only byte addressable. SFRs provide control and data exchange with the resources and peripherals of the Chip. The TM52 series of microcontrollers provides complete binary code with standard 8051 instruction set compatibility. Beside the standard 8051 SFRs, the Chip implements additional SFRs used to configure and access subsystems such as the ADC/LED/LCD, which are unique to the Chip.



	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
F8h	AUX1							
F0h	B	CRCDL	CRCDH	CRCIN		CFGBG	CFGWL	AUX2
E8h								AUX3
E0h	ACC					EFTCON		
D8h	CLKCON							
D0h	PSW	P1LOE		P3LOE				
C8h	T2CON	IAPWE	RCP2L	RCP2H	TL2	TH2		
C0h								
B8h	IP	IPH	IP1	IP1H	SPCON	SPSTA	SPDAT	
B0h	P3	LEDCON	LEDCON2		TKTMRL	TKCON2	ADCHS	TKDHH
A8h	IE	INTE1	ADTKDT	ADCDH	TKDL	TKFREQ	TKCON	P0ADIE
A0h	P2	PWMCON	P1MODL	P1MODH	P3MODL	P3MODH	PINMOD	PWMCON2
98h	SCON	SBUF	PWM0PRD	PWM0DH	PWM1PRD	PWM1DH	PWM2PRD	PWM2DH
90h	P1	P0OE	P0LOE	P2MOD	OPTION	INTFLG	P1WKUP	SWCMD
88h	TCON	TMOD	TL0	TL1	TH0	TH1	SCON2	SBUF2
80h	P0	SP	DPL	DPH				PCON

3. LVR setting

The Chip offers LVR functions. There are 8-level LVR can be selected by CFGWH. The SFR LVRPD and PWRSAV bits also affect LVR function as tables below.

Operation Mode	SFR		CFGWH	LVR	Function	Note
	LVRPD	PWRSAV	LVRE			
Fast Slow	0	X	000	ON	LV Reset 2.2V	
	0	X	001	ON	LV Reset 2.5V	
	0	X	010	ON	LV Reset 2.8V	
	0	X	011	ON	LV Reset 3.1V	
	0	X	100	ON	LV Reset 3.4V	
	0	X	101	ON	LV Reset 3.7V	
	0	X	110	ON	LV Reset 4.0V	
	0	X	111	ON	LV Reset 4.3V	
Idle Stop Halt	0	0	000	ON	LV Reset 2.2V	Current consumption about 60～100uA
	0	0	001	ON	LV Reset 2.5V	
	0	0	010	ON	LV Reset 2.8V	
	0	0	011	ON	LV Reset 3.1V	
	0	0	100	ON	LV Reset 3.4V	
	0	0	101	ON	LV Reset 3.7V	
	0	0	110	ON	LV Reset 4.0V	
	0	0	111	ON	LV Reset 4.3V	
Idle	0	1	XXX	ON	Disable LVR Enable POR 1.90V	Current consumption about 40uA
Stop Halt	0	1	XXX	OFF	Disable	Minimum Current consumption
Fast Slow Idle	1	X	XXX	ON	Disable LVR Enable POR 1.90V	Current consumption about 40uA
Stop Halt	1	X	XXX	OFF	Disable	Minimum Current consumption

Note: *The current consumption of Halt mode is more than Stop mode about 5~23uA, because SRC is enabled.*

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	–	IAPTE		LVRPD
R/W	R/W	R/W	R/W	R/W	–	R/W		R/W
Reset	0	0	0	0	–	1	1	0

F7h.5 **PWRSAV**: Power save
Set 1 to reduce the chip's power consumption at Idle/Halt/Stop mode

F7h.0 **LVRPD:** LVR power down
0: LVR enable
1: LVR disable

Flash **3FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE			PREAD	MVCLOCK	FRCPSC

3FFFh.5~3 **LVRE:** Low Voltage Reset function select
000: Set LVR at 2.2V 100: Set LVR at 3.4V
001: Set LVR at 2.5V 101: Set LVR at 3.7V
010: Set LVR at 2.8V 110: Set LVR at 4.0V
011: Set LVR at 3.1V 111: Set LVR at 4.3V

4. Reset

The Chip has five types of reset methods. Resets can be caused by Power on Reset (POR), External Pin Reset (XRST), Software Command Reset (SWRST), Watchdog Timer Reset (WDTR), or Low Voltage Reset (LVR). The CFGWH controls the Reset functionality. The SFRs are returned to their default value after Reset.

4.1 Power on Reset

After Power on Reset, the device stays on Reset state for 40 ms as chip warm up time, then downloads the CFGW register from ROM's last six bytes. The Power on Reset needs VCC pin's voltage first discharge to near VSS level, then rise beyond 2.2V.

4.2 External Pin Reset

External Pin Reset is active low. It needs to keep at least 2 SRC clock cycle long to be seen by the Chip. External Pin Reset can be disabled or enabled by CFGW.

4.3 Software Command Reset

Software Reset is activated by writing the SFR 97h with data 56h.

4.4 Watchdog Timer Reset

WDT overflow Reset is disabled or enabled by SFR F7h. The WDT uses SRC as its counting time base. It runs in Fast/Slow mode and runs or stops in Idle/Halt/Stop mode. WDT overflow speed can be defined by WDTPSC SFR. WDT is cleared by device Reset or CLRWDT SFR bit.

4.5 Low Voltage Reset

The Chip offers 8 options for LVR function. The user can make a selection by CFGWH, let LVR voltages of 4.3V, 4.0V, 3.7V, 3.4V, 3.1V, 2.8V, 2.5V and 2.2V be selected separately.

Note: *LVR must be enable, also refer to AP-TM52XXXXX_02S for LVR setting information*

Flash **3FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE			PREAD	MVCLOCK	FRCPSC

3FFFh.6 **XRSTE:** External Pin Reset control
0: Disable External Pin Reset
1: Enable External Pin Reset

3FFFh.5~3 **LVRE:** Low Voltage Reset function select
000: Set LVR at 2.2V 100: Set LVR at 3.4V
001: Set LVR at 2.5V 101: Set LVR at 3.7V
010: Set LVR at 2.8V 110: Set LVR at 4.0V
011: Set LVR at 3.1V 111: Set LVR at 4.3V

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	–	WDTPSC		ADCKS		–	–
R/W	R/W	–	R/W		R/W		–	–
Reset	0	–	0	0	0	0	–	–

94h.5~4 **WDTPSC:** Watchdog Timer pre-scalar time select
00: 400ms WDT overflow rate
01: 200ms WDT overflow rate
10: 100ms WDT overflow rate
11: 50ms WDT overflow rate

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL/SWRST							
R/W	W						R/W	R/W
Reset	–						–	0

97h.7~0 **SWRST:** Write 56h to generate S/W Reset

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	–	IAPTE		LVRPD
R/W	R/W	R/W	R/W	R/W	–	R/W		R/W
Reset	0	0	0	0	–	1	1	0

F7h.7~6 **WDTE:** Watchdog Timer Reset control

0x: Watchdog Timer Reset disable

10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Halt/Stop mode

11: Watchdog Timer Reset always enable

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F8h.7 **CLRWDT:** Set to clear WDT, H/W auto clear it at next clock cycle

5. Clock Circuitry & Operation Mode

5.1 System Clock

The Chip is designed with dual-clock system. During runtime, user can directly switch the System clock from fast to slow or from slow to fast. It also can directly select a clock divider of 1, 2, 4 or 16. The Fast clock can be selected as FXT (Fast Crystal, 1~16 MHz) or FRC (Fast Internal RC, 14.7456 MHz). The Slow clock can be selected as SXT (Slow Crystal, 32 KHz) or SRC (Slow Internal RC, 80 KHz). Fast mode and Slow mode are defined as the CPU running at Fast and Slow clock speeds.

After Reset, the device is running at Slow mode with 80 KHz SRC. S/W should select the proper clock rate for chip operation safety. The higher V_{CC} allows the chip to run at a higher System clock frequency. In a typical condition, a 16 MHz System clock rate requires V_{CC}> 2.2V.

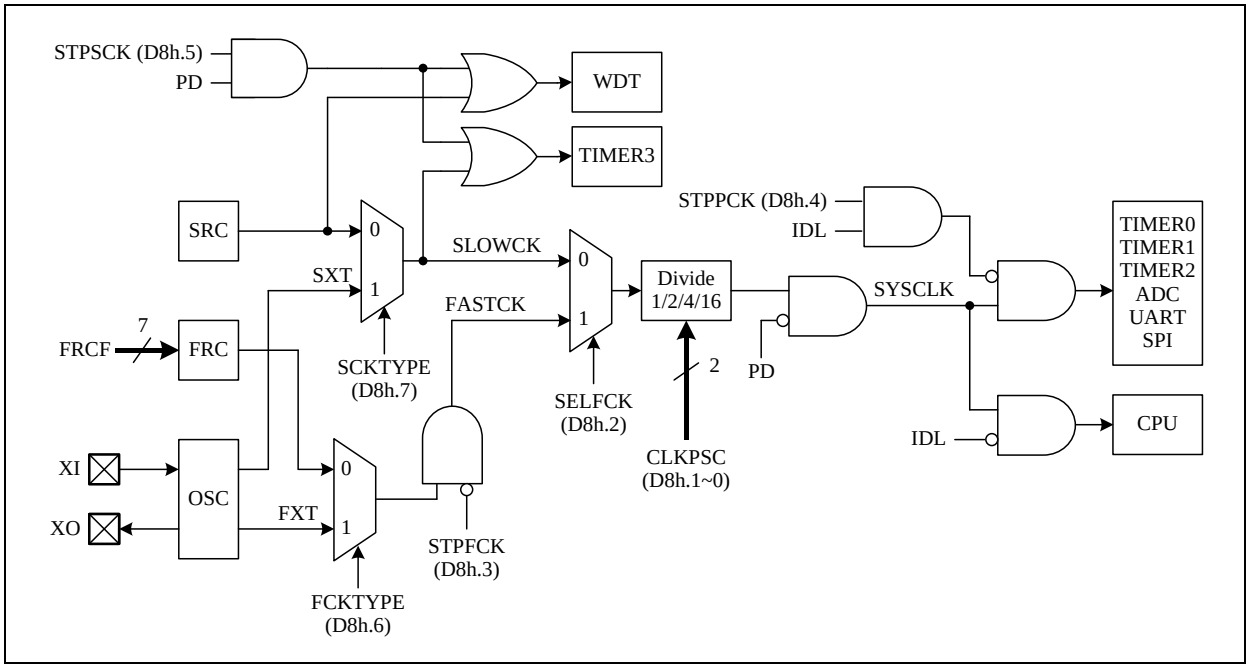
The Chip has an external oscillators connected to the XI/XO pins. It relies on external circuitry for the clock signal and frequency stabilization, such as a stand-alone oscillator, quartz crystal, or ceramic resonator. In Fast mode, the fast oscillator can be used in the range from 1~16 MHz. In Slow mode, the slow oscillator can only use a clock frequency of 32.768 KHz.

The **CLKCON** SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow clock type in Fast mode and change the Fast clock type in Slow mode. Never to write both STPFCK=1 & SELFCK=1. It is recommended to write this SFR bit by bit.

If user wants to switch Fsys from Slow clock to FXT, user should be following the step below

1. Set FCKTYPE (D8h.6)
2. Wait 2ms until FXT oscillation stable
3. Set SELFCK (D8h.2)

The chip can also output the "System clock divided by 2" signal (CKO) to P1.4 pin. CKO pin's output setting is controlled by TCOE SFR (***see Chapter 7***).



Clock Structure

Note: *Because of the CLKPSC delay, it needs to wait for 16 clock cycles (max.) before switching Slow clock to Fast clock. Also refer to AP-TM52XXXXX_01S and AP-TM52XXXXX_02S about System Clock Application Note.*

SYSCLK	CLKCON (D8h)			
	bit7 SCKTYPE	bit6 FCKTYPE	bit3 STPFCK	bit2 SELFCK
Fast FXT	0/1	1	0	1
Fast FRC	0/1	0	0	1
Slow SXT	1	0/1	0/1	0
Slow SRC	0	0/1	0/1	0
Fast type change	0/1	0 ← → 1	0/1	0
Slow type change	0 ← → 1	0/1	0	1
Stop FRC/FXT	0/1	0/1	0 → 1	0
Switch to FRC/FXT	0/1	0/1	0	0 → 1
Switch to SRC/SXT	0/1	0/1	0	1 → 0

Flash **3FFDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	–	FRCF						

3FFDh.6~0 **FRCF:** FRC frequency adjustment.
FRC is trimmed to 14.7456 MHz in chip manufacturing. FRCF records the adjustment data.

SFR **F6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	–	FRCF						
R/W	–	R/W						
Reset	–	–	–	–	–	–	–	–

F6h.6~0 **FRCF:** FRC frequency adjustment
00h= lowest frequency, 7Fh=highest frequency.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	1	0	0	0	1	1

D8h.7 **SCKTYPE:** Slow clock type. This bit can be changed only in Fast mode (SELFCK=1).
0: SRC
1: SXT, P2.0 and P2.1 are crystal pins

D8h.6 **FCKTYPE:** Fast clock type. This bit can be changed only in Slow mode (SELFCK=0).
0: FRC
1: FXT, P2.0 and P2.1 are crystal pins, oscillator gain is high for FXT

D8h.5 **STPSCK:** Set 1 to stop Slow clock in Stop mode.

D8h.4 **STPPCK:** Set 1 to stop UARTs/Timer0/Timer1/Timer2/ADC clock in Idle mode for current reducing. If set, only Timer3 and pin interrupts are alive in Idle mode.

D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.

D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock

D8h.1~0 **CLKPSC:** System clock prescaler. Effective after 16 clock cycles (Max.) delay.
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

5.2 Operation Modes

There are five operation modes for this device. **Fast Mode** is defined as the CPU running at Fast clock speed. **Slow Mode** is defined as the CPU running at Slow clock speed. When the System clock speed is lower, the power consumption is lower.

Idle Mode is entered by setting the IDL bit in PCON SFR. Both Fast and Slow clock can be set as the System clock source in Idle Mode, but Slow clock is better for power saving. In Idle mode, the CPU puts itself to sleep while the on-chip peripherals stay active. The "STPPCK" bit in CLKCON SFR can be set to furthermore reduce Idle mode current. If STPPCK is set, only Timer3 and pin interrupts are alive in Idle Mode, others peripherals such as Timer0/1/2, UARTs and ADC are stop. The slower System clock rate also helps current saving. It can be achieved by setup the CLKPSC SFR to divide System clock frequency. Idle mode is terminated by Reset or enabled Interrupts wake up.

Stop Mode is entered by setting the PD bit in PCON SFR and STPSCK is set. This mode is the so-called "Power Down" mode in standard 8051. In Stop mode, all clocks stop except the WDT could be alive if it is enabled. Stop Mode is terminated by Reset or pin wake up.

Halt Mode is entered by setting the PD bit in PCON SFR and STPSCK is cleared. In Halt mode, all clocks stop except the Timer3 and WDT could be alive if they are enabled. Halt Mode is terminated by Reset, pin wake up or Timer3 interrupt.

Note: *Chip cannot enter Halt/Stop mode if INTn pin is low and wakeup is enable. (INTn=0 and EXn=1, n=0,1,2)*
Note: *FW must turn off Bandgap to obtain Tiny Current (VBGOUT=0)*

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter Halt/Stop mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter Idle mode.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	1	0	0	0	1	1

D8h.7 **SCKTYPE:** Slow clock type. This bit can be changed only in Fast mode (SELFCK=1).
0: SRC 1: SXT

D8h.6 **FCKTYPE:** Fast clock type. This bit can be changed only in Slow mode (SELFCK=0).
0: FRC 1: FXT

D8h.5 **STPSCK:** Set 1 to stop Slow clock in Stop mode.

D8h.4 **STPPCK:** Set 1 to stop UART/Timer0/Timer1/Timer2/ADC clock in Idle mode for current reducing. If set, only Timer3 and pin interrupts are alive in Idle mode.

D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.

D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock 1: Fast clock

D8h.1~0 **CLKPSC:** System clock prescaler. Effective after 16 clock cycles (Max.) delay.
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	–	IAPTE		LVRPD
R/W	R/W	R/W	R/W	R/W	–	R/W		R/W
Reset	0	0	0	0	–	1	1	0

F7h.4 **VBGOUT:** Bandgap voltage output to P3.2, when ADCHS = 1011b
0: Disable
1: Enable

6. Interrupt & Wake-up

This Chip has a 12-source four-level priority interrupt structure. All enabled Interrupts can wake up CPU from Idle mode, but only the Pin Interrupts can wake up CPU from Halt/Stop mode. Each interrupt source has its own enable control bit. An interrupt event will set its individual Interrupt Flag, no matter whether its interrupt enable control bit is 0 or 1. The Interrupt vectors and flags are list below.

Vector	Flag	Description
0003	IE0	INT0 external pin Interrupt (can wake up Halt/Stop mode)
000B	TF0	Timer0 Interrupt
0013	IE1	INT1 external pin Interrupt (can wake up Halt/Stop mode)
001B	TF1	Timer1 Interrupt
0023	RI+TI	Serial Port (UART1) Interrupt
002B	TF2+EXF2	Timer2 Interrupt
0033	–	Reserved for ICE mode use
003B	TF3	Timer3 Interrupt
0043	P1IF	P1.0~P1.3 external pin change Interrupt (can wake up Halt/Stop mode)
004B	IE2	INT2 external pin Interrupt (can wake up Halt/Stop mode)
0053	ADIF+TKIF	ADC/Touch Key Interrupt
005B	SPIF+WCOL+MODF	SPI Interrupt
0063	RI2+TI2	Serial Port (UART2) Interrupt

Interrupt Vector & Flag

6.1 Interrupt Enable and Priority Control

The IE and INTE1 SFRs decide whether the pending interrupt is serviced by CPU. The P1WKUP SFR controls the individual Port1 pin's wake-up and interrupt capability. The IP, IPH, IP1 and IP1H SFRs decide the interrupt priority. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

SFR **96h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1WKUP	–	–	–	–	P1WKUP			
R/W	–	–	–	–	R/W			
Reset	0	0	0	0	0	0	0	0

96h.7~4 **Reserved, Keep 0**

96h.3~0 **P1WKUP:** P1.3~P1.0 pin individual Wake-up / Interrupt enable control

0: Disable

1: Enable

SFR **A8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A8h.7 **EA:** Global interrupt enable control.
0: Disable all Interrupts.
1: Each interrupt is enabled or disabled by its individual interrupt control bit

A8h.5 **ET2:** Timer2 interrupt enable
0: Disable Timer2 interrupt
1: Enable Timer2 interrupt

A8h.4 **ES:** Serial Port (UART1) interrupt enable
0: Disable Serial Port (UART1) interrupt
1: Enable Serial Port (UART1) interrupt

A8h.3 **ET1:** Timer1 interrupt enable
0: Disable Timer1 interrupt
1: Enable Timer1 interrupt

A8h.2 **EX1:** External INT1 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT1 pin Interrupt and Halt/Stop mode wake up
1: Enable INT1 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

A8h.1 **ET0:** Timer0 interrupt enable
0: Disable Timer0 interrupt
1: Enable Timer0 interrupt

A8h.0 **EX0:** External INT0 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT0 pin Interrupt and Halt/Stop mode wake up
1: Enable INT0 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	–	–	ES2	SPIE	ADTKIE	EX2	P1IE	TM3IE
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

A9h.5 **ES2:** Serial Port (UART2) interrupt enable
0: Disable Serial Port (UART2) interrupt
1: Enable Serial Port (UART2) interrupt

A9h.4 **SPIE:** SPI interrupt enable
0: Disable SPI interrupt
1: Enable SPI interrupt

A9h.3 **ADTKIE:** ADC/Touch Key interrupt enable
0: Disable ADC/Touch Key interrupt
1: Enable ADC/Touch Key interrupt

A9h.2 **EX2:** External INT2 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT2 pin Interrupt and Halt/Stop mode wake up
1: Enable INT2 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

A9h.1 **P1IE:** P1.0~P1.3 pin change interrupt enable. This bit does not affect the P1.0~P1.3 pin's Halt/Stop mode wake up capability.
0: Disable P1.0~P1.3 pin change interrupt
1: Enable P1.0~P1.3 pin change interrupt

A9h.0 **TM3IE:** Timer3 interrupt enable
0: Disable Timer3 interrupt
1: Enable Timer3 interrupt

SFR **B9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPH	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

SFR **B8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

B9h.5, B8h.5 **PT2H, PT2 :** Timer2 Interrupt Priority control. (PT2H, PT2) =
11: Level 3 (highest priority)
10: Level 2
01: Level 1
00: Level 0 (lowest priority)

B9h.4, B8h.4 **PSH, PS :** Serial Port (UART1) Interrupt Priority control. Definition as above.

B9h.3, B8h.3 **PT1H, PT1 :** Timer1 Interrupt Priority control. Definition as above.

B9h.2, B8h.2 **PX1H, PX1 :** External INT1 pin Interrupt Priority control. Definition as above.

B9h.1, B8h.1 **PT0H, PT0 :** Timer0 Interrupt Priority control. Definition as above.

B9h.0, B8h.0 **PX0H, PX0 :** External INT0 pin Interrupt Priority control. Definition as above.

SFR **BBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1H	–	–	PS2H	PSPIH	PADTKIH	PX2H	PP1H	PT3H
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

SFR **BAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1	–	–	PS2	PSPI	PADTKI	PX2	PP1	PT3
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

BBh.5, BAh.5 **PS2H, PS2 :** Serial Port (UART2) Interrupt Priority control. Definition as above.

BBh.4, BAh.4 **PSPIH,PSPI :** SPI Interrupt Priority control. Definition as above.

BBh.3, BAh.3 **PADTKIH, PADTKI :** ADC/Touch Key Interrupt Priority control. Definition as above.

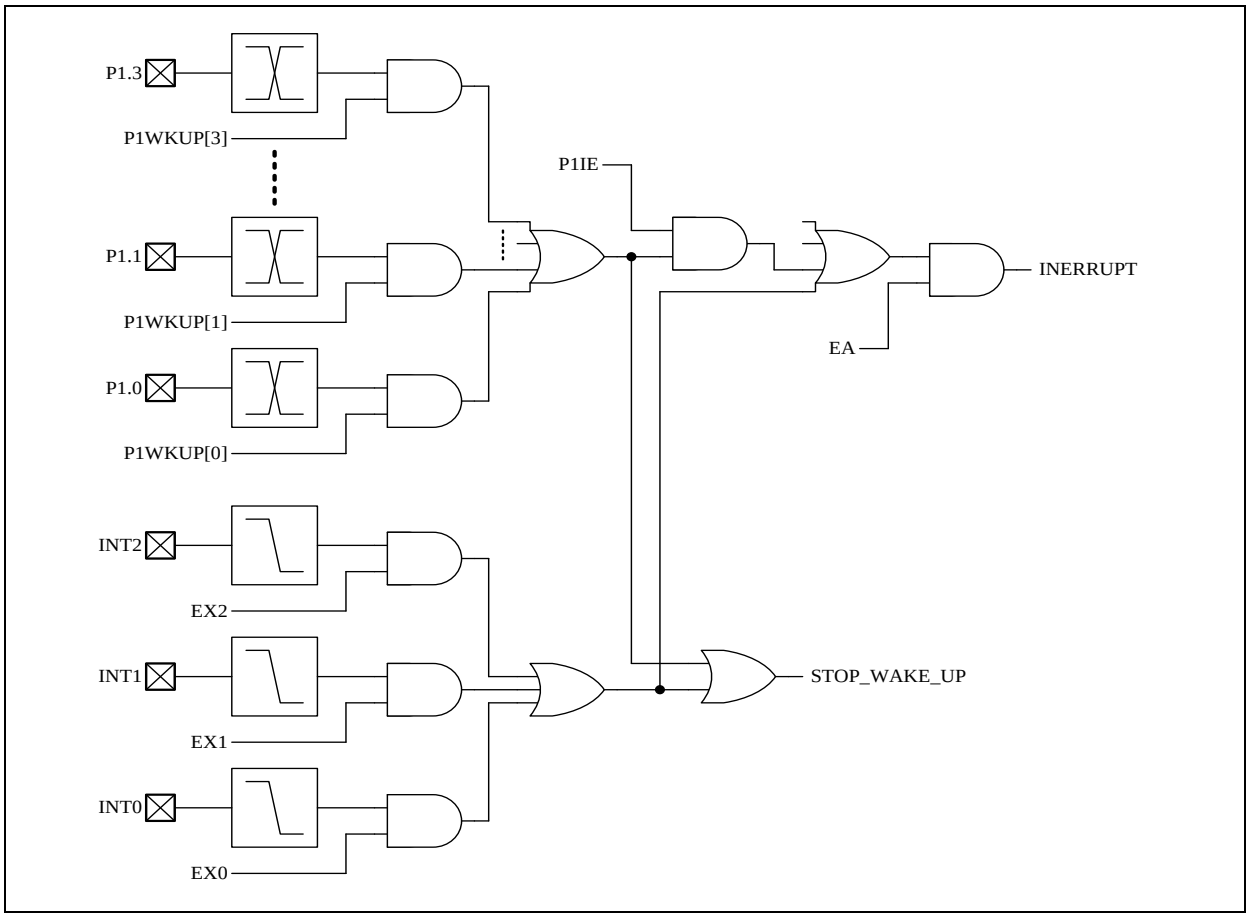
BBh.2, BAh.2 **PX2H, PX2 :** External INT2 pin Interrupt Priority control. Definition as above.

BBh.1, BAh.1 **PP1H, PP1 :** P1.0~P1.3 Pin Change Interrupt Priority control. Definition as above.

BBh.0, BAh.0 **PT3H, PT3 :** Timer3 Interrupt Priority control. Definition as above.

6.2 Pin Interrupt

Pin Interrupts include INT0 (P3.2), INT1 (P3.3), INT2 (P3.7) and P1.0~P1.3 Change Interrupt. These pins also have the Halt/Stop mode wake up capability. INT0 and INT1 are falling edge or low level triggered as the 8051 standard. INT2 is falling edge triggered and P1.0~P1.3 Pin Change Interrupt is triggered by any P1.0~P1.3 pin state change.



Pin Interrupt & Wake up

Note: *Chip cannot enter Halt/Stop mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0~2)*

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.3 **IE1:** External Interrupt 1 (INT1 pin) edge flag.
Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.2 **IT1:** External Interrupt 1 control bit
0: Low level active (level triggered) for INT1 pin
1: Falling edge active (edge triggered) for INT1 pin

88h.1 **IE0:** External Interrupt 0 (INT0 pin) edge flag
Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.0 **IT0:** External Interrupt 0 control bit
0: Low level active (level triggered) for INT0 pin
1: Falling edge active (edge triggered) for INT0 pin

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	TKIF	ADIF	–	IE2	P1IF	TF3
R/W	–	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

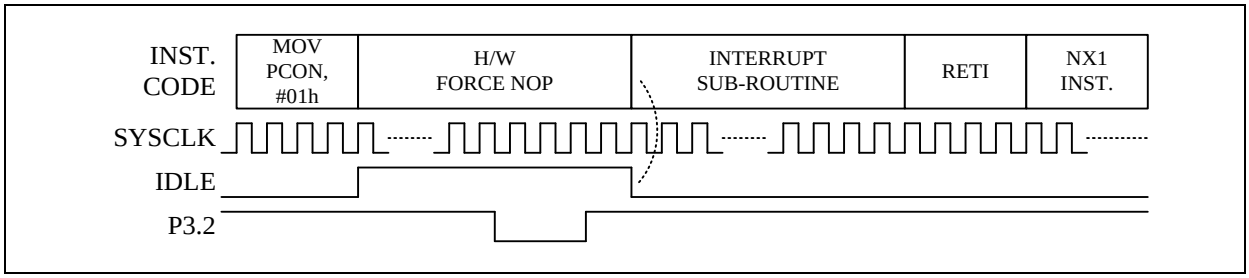
95h.2 **IE2:** External Interrupt 2 (INT2 pin) edge flag
Set by H/W when a falling edge is detected on the INT2 pin, no matter the EX2 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FBh to INTFLG to clear this bit. (***Note***)

95h.1 **P1IF:** P1.0~P1.3 pin change interrupt flag
Set by H/W when a P1.0~P1.3 pin state change is detected and its interrupt enable bit is set (P1WKUP). P1IE does not affect this flag's setting.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FDh to INTFLG to clear this bit. (***Note***)

Note: *S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.*

6.3 Idle mode Wake up and Interrupt

Idle mode is waked up by enabled Interrupts, which means individual interrupt enable bit (ex: EX0) and EA bit must be both set to 1 to establish Idle mode wake up capability. All enabled Interrupts (Pins, Timers, ADC, TK, SPI and UARTs) can wake up CPU from Idle mode. Upon Idle wake-up, Interrupt service routine is entered immediately. "The first instruction behind IDL (PCON.0) setting" is executed after interrupt service routine return.



EA=EX0=1, Idle mode wake-up and Interrupt by P3.2 (INT0)

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

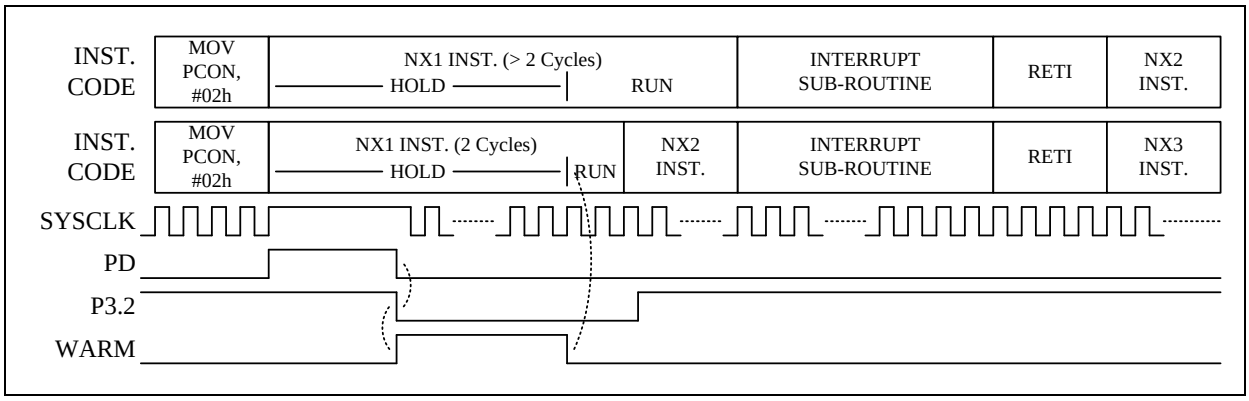
87h.1 **PD:** Power down control bit, set 1 to enter Halt/Stop mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter Idle mode.

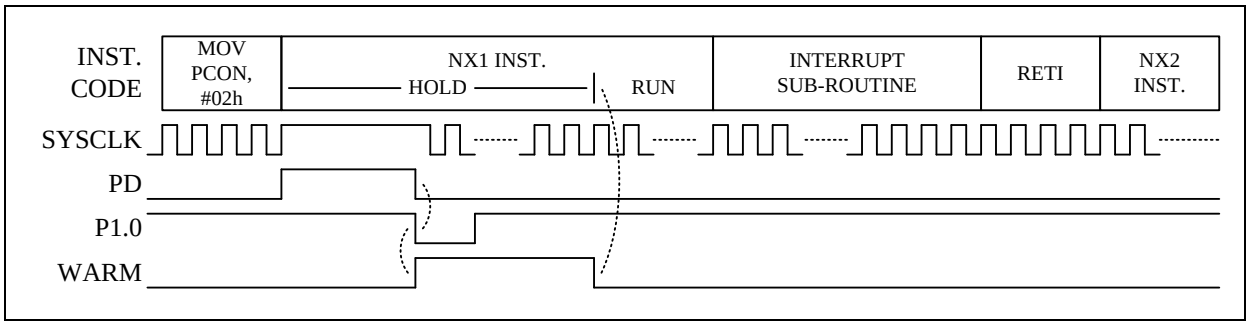
6.4 Halt/Stop mode Wake up and Interrupt

Halt/Stop mode wake up is simple, as long as the individual pin interrupt enable bit (ex: EX0) is set, the pin wake up capability is asserted. Set EX0/EX1/EX2 can enable INT0/INT1/INT2 pins' Halt/Stop mode wake up capability. Set P1WKUP bit 3~0 can enable P1.3~P1.0's Halt/Stop mode wake up capability. Upon Halt/Stop wake up, "the first instruction behind PD setting (PCON.1)" is executed immediately before Interrupt service. Interrupt entry requires EA=1 (P1WKUP also needs P1IE=1) and trigger state of the pin staying sufficiently long to be observed by the System clock. This feature allows CPU to enter or not enter Interrupt sub-routine after Halt/Stop mode wake up.

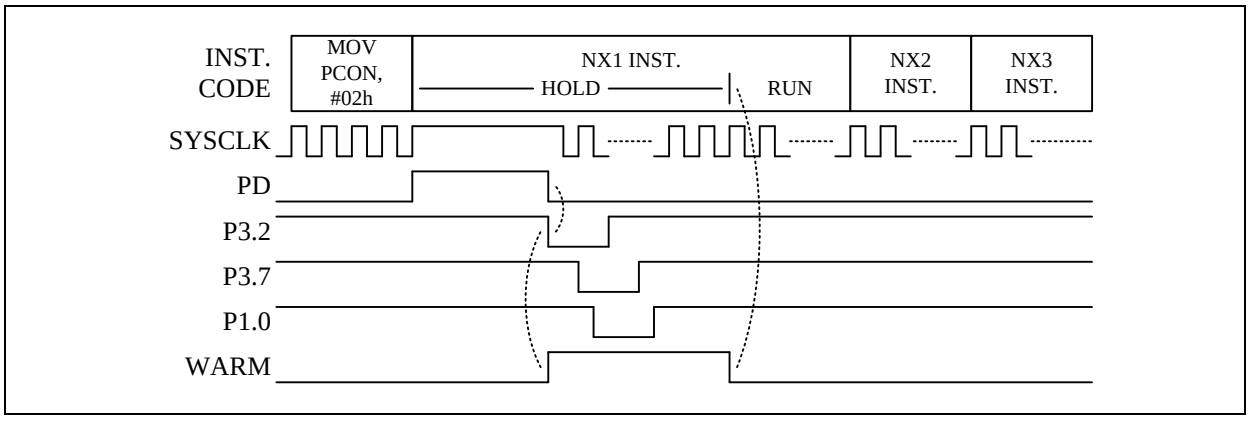
Note: *It is recommended to place the NX1/NX2 with NOP Instruction in figures below.*



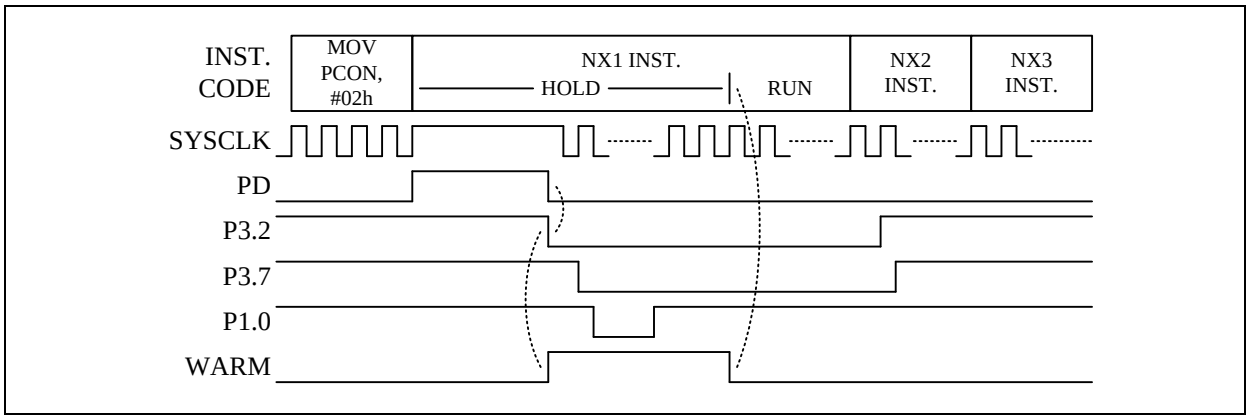
EA=EX0=1, P3.2 (INT0) is sampled after warm-up, Halt/Stop mode wake-up and Interrupt



EA=P1IE=P1WKUP=1, P1.0 change (not need clock sample), Halt/Stop mode wake-up and Interrupt



EA=EX0=EX2=P1WKUP=1, P1IE=0, Halt/Stop mode wake-up but not Interrupt. P3.2/P3.7 pulse too narrow



EX0=EX2=P1WKUP=P1IE=1, EA=0, Halt/Stop mode wake-up but not Interrupt

7. I/O Ports

The Chip has total 26 multi-function I/O pins. All I/O pins follow the standard 8051 "Read-Modify-Write" feature. The instructions that read the SFR rather than the Pin State are the ones that read a port or port bit value, possibly change it, and then rewrite it to the SFR (ex: ANL P1, A; INC P2; CPL P3.0).

7.1 Port1 & P2.1~P2.0 & Port 3

These pins can operate in four different modes as below.

Mode	Port1, P2.1~P2.0, Port3 pin function		Px.n SFR data	Pin State	Resistor Pull-up	Digital Input
	P3.0~P3.2	Others				
Mode 0	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Pull-up	Y	Y
Mode 1	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Hi-Z	N	Y
Mode 2	CMOS Output		0	Drive Low	N	N
			1	Drive High	N	N
Mode 3	Analog input for ADC, digital input buffer is disabled		X (don't care)	–	N	N

I/O Pin Function Table

If a Port1, P2.1~P2.0 or Port3 pin is used for Schmitt-trigger input, S/W must set the I/O pin to Mode0 or Mode1 and set the corresponding Port Data SFR to 1 to disable the pin's output driving circuitry.

Beside I/O port function, each Port1, P2.1~P2.0 and Port3 pin has one or more alternative functions, such as LCD, LED, ADC and Touch Key. Most of the functions are activated by setting the individual pin mode control SFR to Mode3. Port1/Port3 pins have standard 8051 auxiliary definition such as INT0/1, T0/1/2, or RXD/TXD. These pin functions need to set the pin mode SFR to Mode0 or Mode1 and keep the P1.n/P3.n SFR at 1.

Pin Name	8051	Wake-up	CKO	ADC	TK	LCD	LED	others	Mode3
P1.0	T2	Y	T2O	AD4	TK4	LCDC10			AD4
P1.1	T2EX	Y		AD5	TK5	LCDC11			AD5
P1.2		Y		AD6	TK6	LCDC12		PWM0	AD6
P1.3		Y		AD7	TK7	LCDC13		PWM1	AD7
P1.4		Y	CKO	AD8	TK8	LCDC14			AD8
P1.5		Y		AD9	TK14	LCDC15			AD9
P1.6		Y			TK9	LCDC16		PWM2	
P1.7	TXD2	Y			TK16	LCDC17		MISO	
P3.0	RXD			AD3	TK3	LCDC30			AD3
P3.1	TXD			AD2	TK2	LCDC31			AD2
P3.2	INT0	Y		AD1	TK1	LCDC32		VBGO	AD1
P3.3	INT1	Y		AD0	TK0	LCDC33			AD0
P3.4	T0		T0O		TK13	LCDC34	LEDS3	SS	
P3.5	T1				TK18	LCDC35	LEDS0	MOSI	
P3.6	RXD2				TK17	LCDC36	LEDS1	SCK	
P3.7	INT2	Y			TK19	LCDC37	LEDS2	RSTn	
P2.0							LEDS4	XI	
P2.1							LEDS5	XO	

Port1, P2.1~P2.0, Port3 multi-function Table

The necessary SFR setting for Port1/P2.1~P2.0/Port3 pin's alternative function is list below.

Alternative Function	Mode	Px.n SFR data	Pin State	Other necessary SFR setting
T0, T1, T2, T2EX, INT0, INT1, INT2	**0**	1	Input with Pull-up	
	1	1	Input	
RXD, TXD	**0**	1	Input with Pull-up / Pseudo Open Drain Output	
	1	1	Input / Pseudo Open Drain Output	
RXD2,TXD2	**0**	1	Input with Pull-up / Open Drain Output	
	1	1	Input / Open Drain Output	
T0O, T2O, CKO	**0**	X	Clock Open Drain Output with Pull-up	PINMOD
	1	X	Clock Open Drain Output	
	2	X	Clock Output (CMOS Push-Pull)	
VBGO	**X**	X	Bandgap Voltage output	VBGOUT ADCHS
LCDC10~ LCDC17 LCDC30~ LCDC37	**X**	X	1/2 Vcc Bias Output	P1LOE P3LOE
LEDS0~ LEDS5 (***Note***)	**X**	X	LED Waveform Output	LEDCON
TK0~TK14 TK16~TK19	**0**	1	Touch Key Idling, Pull-up	TKCHS
			Touch Key Scanning	
	2	X	Touch Key Idling, CMOS Push-Pull	
			Touch Key Scanning	
AD0~AD9	**3**	X	ADC Channel	ADCHS
PWM0~PWM2	**0**	X	PWM Open Drain Output with Pull-up	PINMOD PWMCON2
	1	X	PWM Open Drain Output	
	2	X	PWM Output (CMOS Push-Pull)	
SPI Master Mode MISO	**1**	1	SPI Data Input	SPCON
SPI Master Mode SCK, MOSI	**2**	X	SPI Clock/Data Output (CMOS Push-Pull)	SPCON
SPI Slave Mode MISO	**2**	X	SPI Data Output (CMOS Push-Pull)	SPCON
SPI Slave Mode SCK, MOSI	**1**	1	SPI Clock/Data Input	SPCON
SS	**1**	1	SPI Chip Selection	SPCON
XI, XO	**0**	1	Crystal oscillation	CLKCON

Mode Setting for Port1, P2.1~P2.0, Port3 Alternative Function

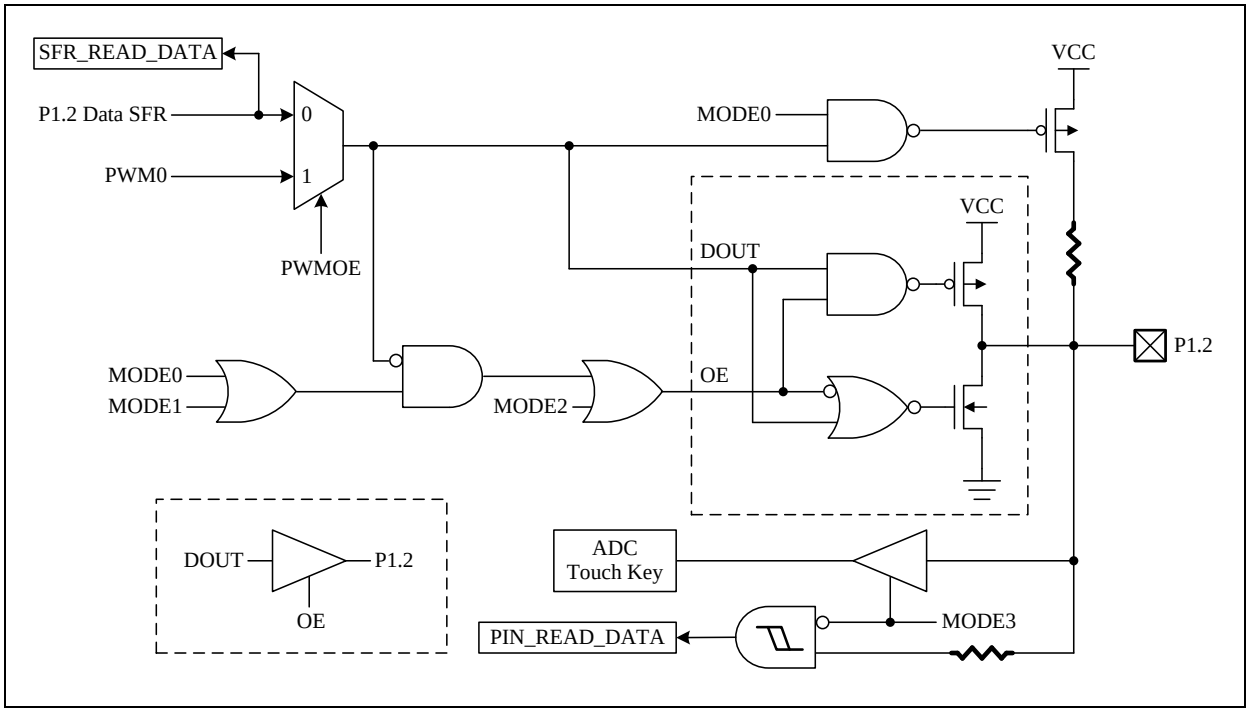
For tables above, a "**CMOS Output**" pin means it can sink and drive at least 4 mA current. It is not recommended to use such pin as input function.

An "**Open Drain**" pin means it can sink at least 4 mA current but only drive a small current (<20 μA). It can be used as input or output function and typically needs an external pull up resistor.

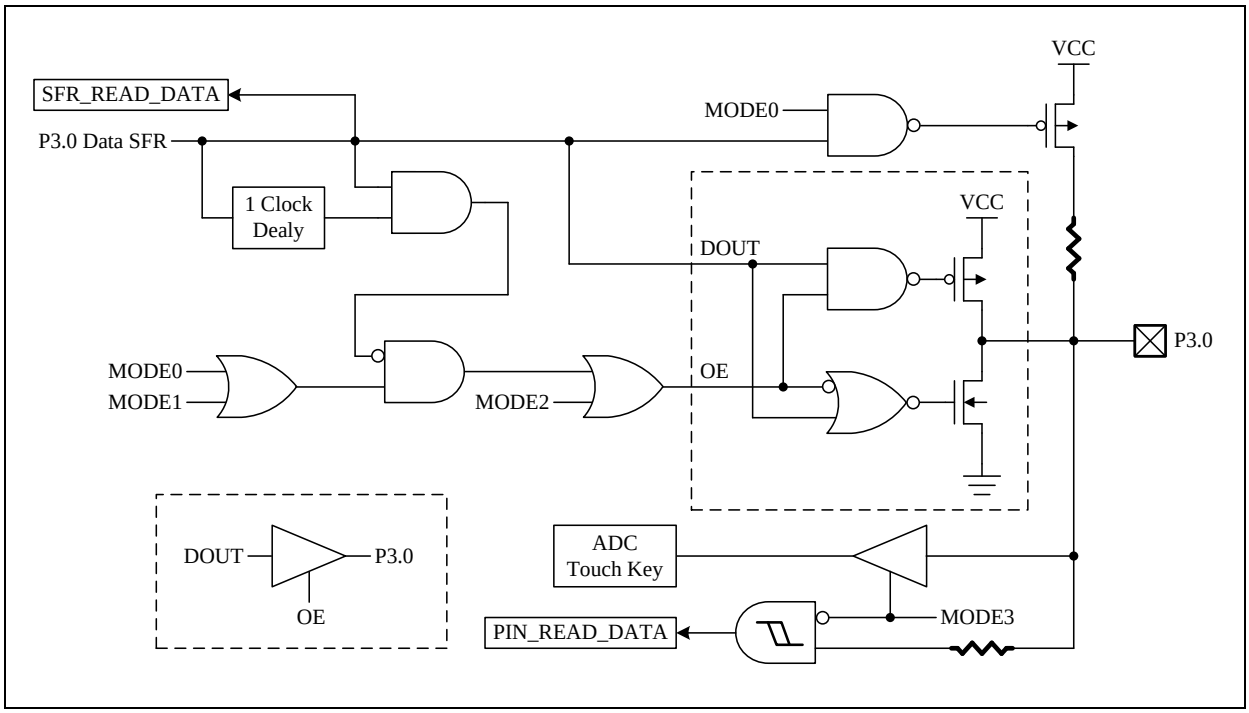
An 8051 standard pin is a "**Pseudo Open Drain**" pin. It can sink at least 4 mA current when output is at low level, and drives at least 4 mA current for 1~2 clock cycle when output transits from low to high, then keeps driving a small current (<20 μA) to maintain the pin at high level. It can be used as input or output function.

Note: *for the necessary SFR setting above, LCD/LED pin has the highest priority. Therefore, if a pin is not used for Segment (ex: pin is I/O, ADC, TK, and SPI…), S/W must disable the LCD/LED function.*

The chip also supports I/O High-sink function. It is an option and is turned on by default. For efficient control, we divide the High-sink pins into three groups (Group 0: P00~P03, P20, P21, P34~P37; Group 1: P04, P05, P10~P17; Group 2: P06, P07, P22~P25, P30~P33). It is enabled by setting SFR HSNK0EN, HSNK1EN and HSNK2EN.



P1.2 Pin Structure



P3.0 Pin Structure

SFR **90h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

90h.7~0 **P1:** Port1 data

SFR **A0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

A0h.1~0 **P2.1~P2.0:** P2.1~P2.0 data

SFR **B0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

B0h.7~0 **P3:** Port1 data

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	1	0	0	0	1	1

D8h.7 **SCKTYPE:** Slow clock type. This bit can be changed only in Fast mode (SELFCK=1).
0: SRC
1: SXT, P2.0 and P2.1 are crystal pins

D8h.6 **FCKTYPE:** Fast clock type. This bit can be changed only in Slow mode (SELFCK=0).
0: FRC
1: FXT, P2.0 and P2.1 are crystal pins, oscillator gain is high for FXT

SFR **A2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODL	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A2h.7~6 **P1MOD3:** P1.3 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.3 is ADC input

A2h.5~4 **P1MOD2:** P1.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.2 is ADC input

A2h.3~2 **P1MOD1:** P1.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.1 is ADC input

A2h.1~0 **P1MOD0:** P1.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.0 is ADC input

SFR **A3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODH	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A3h.7~6 **P1MOD7:** P1.7 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A3h.5~4 **P1MOD6:** P1.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A3h.3~2 **P1MOD5:** P1.5 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.5 is ADC input

A3h.1~0 **P1MOD4:** P1.4 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.4 is ADC input

SFR **A4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODL	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A4h.7~6 **P3MOD3:** P3.3 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P3.3 is ADC input

A4h.5~4 **P3MOD2:** P3.2 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P3.2 is ADC input

A4h.3~2 **P3MOD1:** P3.1 pin control.
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P3.1 is ADC input

A4h.1~0 **P3MOD0:** P3.0 pin control.
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P3.0 is ADC input

SFR **A5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODH	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A5h.7~6 **P3MOD7:** P3.7 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3

A5h.5~4 **P3MOD6:** P3.6 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3

A5h.3~2 **P3MOD5:** P3.5 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3

A5h.1~0 **P3MOD4:** P3.4 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2MOD	–	–	–	–	P2MOD1		P2MOD0	
R/W	–	–	–	–	R/W		R/W	
Reset	–	–	–	–	0	1	0	1

93h.3~2 **P2MOD1:** P2.1 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: not defined

93h.1~0 **P2MOD0:** P2.0 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: not defined

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1OE	PWM0OE	TCOE	T2OE	HSNK2EN	HSNK1EN	HSNK0EN	T0OE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	0

A6h.7 **PWM1OE:** PWM1 control
- 0: PWM1 disable
- 1: PWM1 enable and signal output to P1.3 pin

A6h.6 **PWM0OE:** PWM0 control
- 0: PWM0 disable
- 1: PWM0 enable and signal output to P1.2 pin

A6h.5 **TCOE:** System clock signal output (CKO) control
- 0: Disable "System clock divided by 2" output to P1.4 pin
- 1: Enable "System clock divided by 2" output to P1.4 pin

A6h.4 **T2OE:** Timer2 signal output (T2O) control
- 0: Disable "Timer2 overflow divided by 2" output to P1.0 pin
- 1: Enable "Timer2 overflow divided by 2" output to P1.0 pin

A6h.3 **HSNK2EN:** Pin High-sink enable (Group 2: P06, P07, P22~P25, P30~P33)
- 0: Group 2 High-sink disable
- 1: Group 2 High-sink enable

A6h.4 **HSNK1EN:** Pin High-sink enable (Group 1: P04, P05, P10~P17)
- 0: Group 1 High-sink disable
- 1: Group 1 High-sink enable

A6h.1 **HSNK0EN:** Pin High-sink enable (Group 0: P00~P03, P20, P21, P34~P37)
- 0: Group 0 High-sink disable
- 1: Group 0 High-sink enable

A6h.0 **T0OE:** Timer0 signal output (T0O) control
- 0: Disable "Timer0 overflow divided by 64" output to P3.4 pin
- 1: Enable "Timer0 overflow divided by 64" output to P3.4 pin

SFR **A7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON2	–	–	–	PWM2OE	PWM2CKS		PWM2DL	
R/W	–	–	–	R/W	R/W		R/W	
Reset	–	–	–	0	1	0	0	0

A7h.4 **PWM2OE:** PWM2 control
- 0: PWM2 disable
- 1: PWM2 enable and signal output to P1.6 pin

SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LEDCON	LEDEN		LEDPSC		LEDHOLD	LEDBRIT		
R/W	R/W		R/W		R/W	R/W		
Reset	0	0	0	0	0	1	0	0

B1h.7~6 **LEDEN:** LED Enable
00: LED disable
01: LED 1/8 duty (COM0~3, SEG0~3), the LED pins' state will be controlled automatically
10: Reserved
11: LED 1/10 duty (COM0~3, SEG0~5), the LED pins' state will be controlled automatically

SFR **BCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPCON	SPEN	MSTR	CPOL	CPHA	SSDIS	LSBF	SPCR	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

BCh.7 **SPEN:** SPI enable
0: SPI disable
1: SPI enable, P1.7, P3.5, P3.6 are SPI functional pins.

BCh.3 **SSDIS:** SS pin disable
0: Enable SS pin, P3.4 is SPI chip selection input.
1: Disable SS pin

SFR **D1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1LOE	P1LOE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D1h.7~0 **P1LOE:** Port1 LCD 1/2 bias output enable control
0: Disable
1: Enable

SFR **D3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3LOE	P3LOE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D3h.7~0 **P3LOE:** Port3 LCD 1/2 bias output enable control
0: Disable
1: Enable

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	–	IAPTE		LVRPD
R/W	R/W	R/W	R/W	R/W	–	R/W		R/W
Reset	0	0	0	0	–	1	1	0

F7h.4 **VBGOUT:** Bandgap voltage output control
0: Disable
1: Bandgap voltage output to P3.2 pin, when ADCHS=1011b

7.2 Port0

These pins are shared with TK, ADC, LCD/LED. If a Port0 is defined as I/O pin, it can be used as CMOS push-pull output or Schmitt-trigger input. The pin's pull up function is enable while SFR bit P0OE.n=0 and P0.n=1.

Port0 pin function	P0OE.n	P0.n SFR data	Pin State	Resistor Pull-up	Digital Input
Input	0	0	Hi-Z	N	Y
	0	1	Pull-up	Y	Y
CMOS Output	1	0	Drive Low	N	N
	1	1	Drive High	N	N

Port0 Pin Function Table

Pin Name	Wake-up	ADC	TK	LCD	LED	Others
P0.0				LCDC00	LEDC0	
P0.1				LCDC01	LEDC1	
P0.2				LCDC02	LEDC2	
P0.3				LCDC03	LEDC3	
P0.4		AD12	TK10	LCDC04		
P0.5		AD13	TK11	LCDC05		
P0.6		AD14	TK12	LCDC06		
P0.7		AD10		LCDC07		

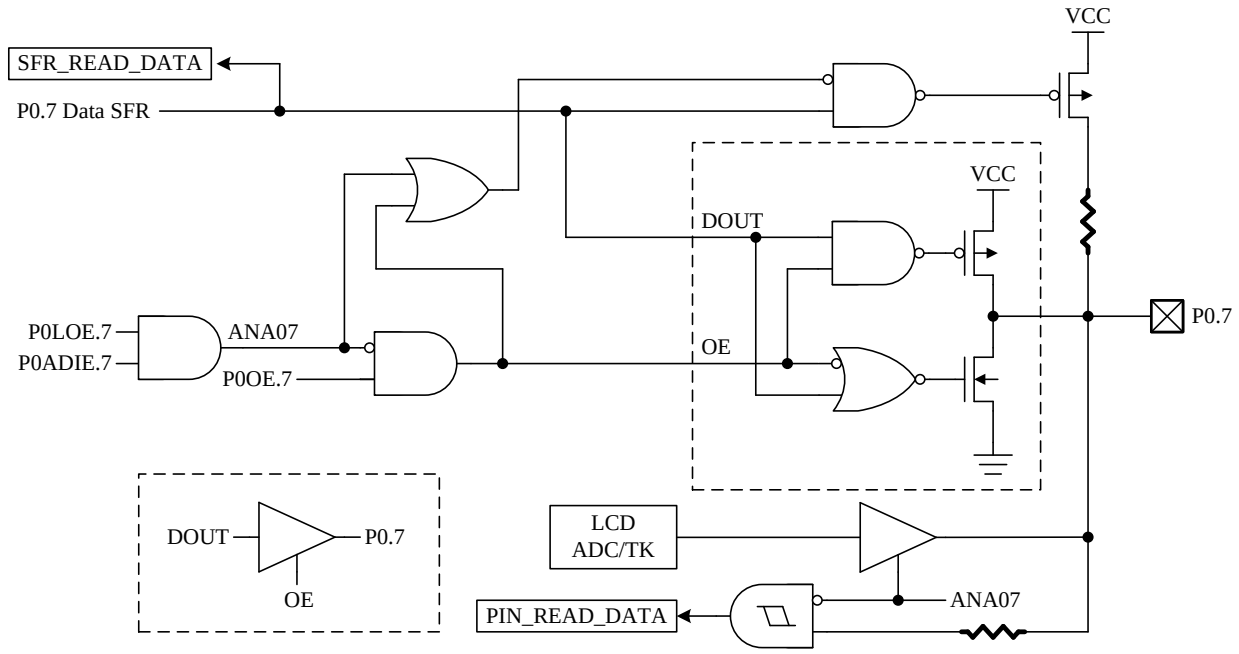
Port0 multi-function Table

The necessary SFR setting for Port0 pin's alternative function is list below.

Alternative Function	PxOE.n	Px.n SFR data	Pin State	other necessary SFR setting
LEDC0~ LEDC3	X	X	LED Waveform Output	LEDCON
LCDC00~ LCDC07	X	X	1/2 Bias Output	P0LOE
AD10, AD12~AD14	X	X	ADC Channel	P0ADIE
TK10~TK12	0	1	Touch Key Idling, Pull-up	TKCHS
			Touch Key Scanning	
	1	X	Touch Key Idling, CMOS Push-Pull	
			Touch Key Scanning	

Mode Setting for Port0 Alternative Function Table

Note: *P0LOE and P0ADIE have higher priority than P0OE.*



P0.7 Pin Structure

SFR **80h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

80h.7~0 **P0:** Port0 data, also controls the P0.n pin's pull-up function. If the P0.n SFR data is "1" and the corresponding P0OE.n = 0 (input mode), the pull-up is enabled.

SFR **91h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0OE	P0OE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

91h.7~0 **P0OE:** Port0 CMOS Push-Pull output enable control
0: Disable
1: Enable

SFR **92h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0LOE	P0LOE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

92h.7~0 **P0LOE:** Port0 LCD 1/2 bias output enable control
0: Disable
1: Enable

SFR **AFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0ADIE	P0ADIE				–	–	–	–
R/W	R/W				–	–	–	–
Reset	0	0	0	0	–	–	–	–

AFh.7~4 **P0ADIE:** ADC channel input Enable
0000: P0.7~P0.4 are digital input
1xxx: P0.7 is ADC input
x1xx: P0.6 is ADC input
xx1x: P0.5 is ADC input
xxx1: P0.4 is ADC input

SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LEDCON	LEDEN		LEDPSC		LEDHOLD	LEDBRIT		
R/W	R/W		R/W		R/W	R/W		
Reset	0	0	0	0	0	1	0	0

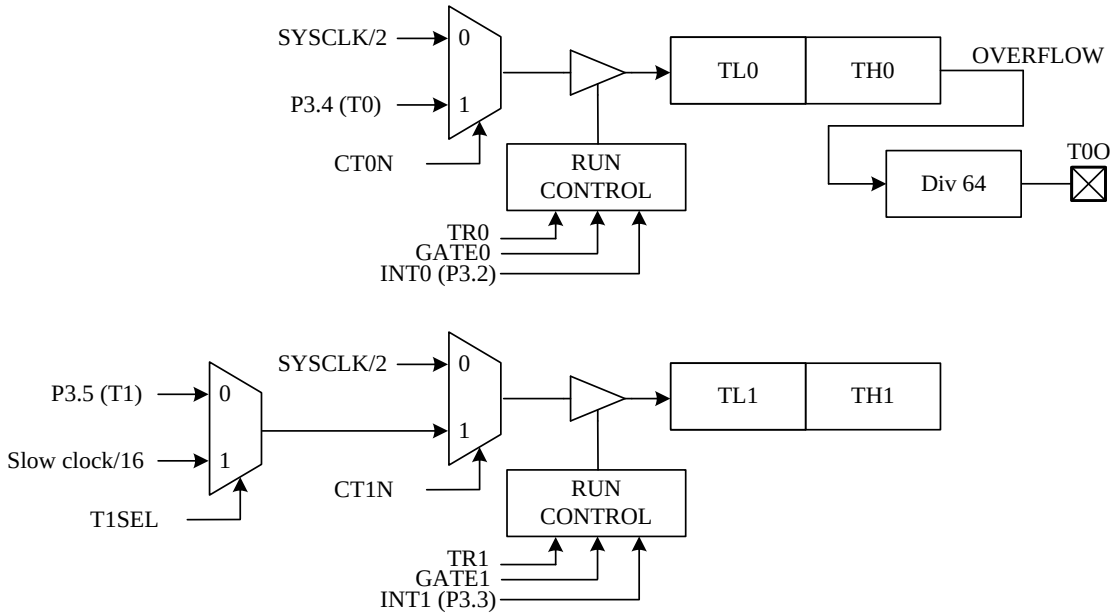
B1h.7~6 **LEDEN:** LED Enable
00: LED disable
01: LED 1/8 duty (COM0~3, SEG0~3), the LED pins' state will be controlled automatically
10: Reserved
11: LED 1/10 duty (COM0~3, SEG0~5) , the LED pins' state will be controlled automatically

8. Timers

Timer0, Timer1 and Timer2 are provided as standard 8051 compatible timer/counter. Compare to the traditional 12T 8051, the Chip's Timer0/1/2 use 2 System clock cycle as the time base unit. That is, in timer mode, these timers increase at every "2 System clock" rate; in counter mode, T0/T1/T2 pin input pulse must be wider than 2 System clock to be seen by this device. In addition to the standard 8051 timers function. The T0O pin can output the "Timer0 overflow divided by 64" signal, and the T2O pin can output the "Timer2 overflow divided by 2" signal. Timer3 is provided for a real-time clock count, when its time base is SXT.

8.1 Timer0 / Timer1

TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the Timer0/Timer1, with the timer/counter values stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).



Timer0 and Timer1 Structure

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.7 **TF1:** Timer1 overflow flag
Set by H/W when Timer/Counter 1 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.6 **TR1:** Timer1 run control
0: Timer1 stops
1: Timer1 runs

88h.5 **TF0:** Timer0 overflow flag
Set by H/W when Timer/Counter 0 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.4 **TR0:** Timer0 run control
0: Timer0 stops
1: Timer0 runs

SFR **89h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

89h.7 **GATE1:** Timer1 gating control bit
0: Timer1 enable when TR1 bit is set
1: Timer1 enable only while the INT1 pin is high and TR1 bit is set

89h.6 **CT1N:** Timer1 Counter/Timer select bit
0: Timer mode, Timer1 data increases at 2 System clock cycle rate
1: Counter mode, Timer1 data increases at T1 pin's negative edge

89h.5~4 **TMOD1:** Timer1 mode select
00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow.
11: Timer1 stops

89h.3 **GATE0:** Timer0 gating control bit
0: Timer0 enable when TR0 bit is set
1: Timer0 enable only while the INT0 pin is high and TR0 bit is set

89h.2 **CT0N:** Timer0 Counter/Timer select bit
0: Timer mode, Timer0 data increases at 2 System clock cycle rate
1: Counter mode, Timer0 data increases at T0 pin's negative edge

89h.1~0 **TMOD0:** Timer0 mode select
00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow.
11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.

SFR **8Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL0	TL0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ah.7~0 **TL0:** Timer0 data low byte

SFR **8Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL1	TL1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Bh.7~0 **TL1:** Timer1 data low byte

SFR **8Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH0	TH0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ch.7~0 **TH0:** Timer0 data high byte

SFR **8Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH1	TH1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Dh.7~0 **TH1:** Timer1 data high byte

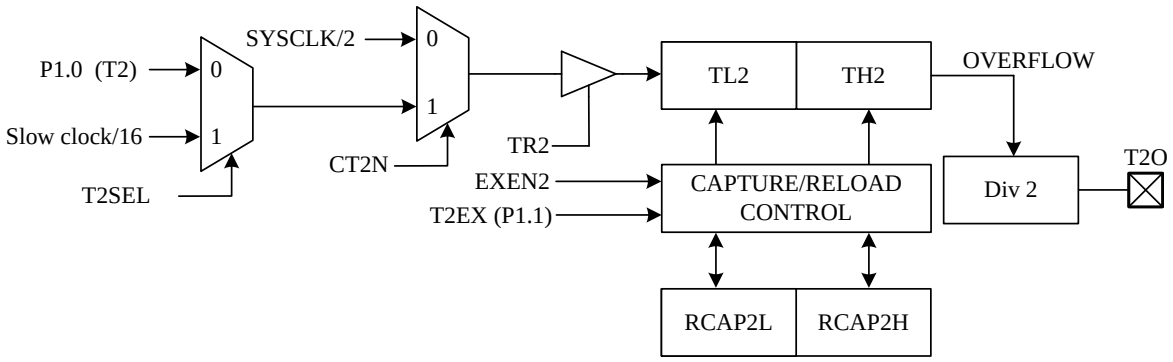
SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F8h.1 **T1SEL:** Timer1 Counter mode, T1 pin input select
0: P3.5 (T1)
1: Slow clock/16

***Note**: See also Chapter 6 for more information on Timer0/1 interrupt enable and priority.*
***Note**: See also Chapter 7 for details on T0O pin output settings.*

8.2 Timer2

Timer2 is controlled through the TCON2 register with the low and high bytes of Timer/Counter2 stored in TL2 and TH2 and the low and high bytes of the Timer2 reload/capture registers stored in RCAP2L and RCAP2H.



Timer2 Structure

SFR **C8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

C8h.7 **TF2:** Timer2 overflow flag
Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.

C8h.6 **EXF2:** T2EX interrupt pin falling edge flag
Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.

C8h.5 **RCLK:** UART receive clock control bit
0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3
1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3

C8h.4 **TCLK:** UART transmit clock control bit
0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3
1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3

C8h.3 **EXEN2:** T2EX pin enable
0: T2EX pin disable
1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0

C8h.2 **TR2:** Timer2 run control
0: Timer2 stops
1: Timer2 runs

C8h.1 **CT2N:** Timer2 Counter/Timer select bit
0: Timer mode, Timer2 data increases at 2 System clock cycle rate
1: Counter mode, Timer2 data increases at T2 pin's negative edge

C8h.0 **CPRL2N:** Timer2 Capture/Reload control bit
0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1.
1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1.
If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.

SFR **CAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2L	RCP2L							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CAh.7~0 **RCP2L:** Timer2 reload/capture data low byte

SFR **CBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2H	RCP2H							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CBh.7~0 **RCP2H:** Timer2 reload/capture data high byte

SFR **CCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL2	TL2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CCh.7~0 **TL2:** Timer2 data low byte

SFR **CDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH2	TH2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CDh.7~0 **TH2:** Timer2 data high byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F8h.2 **T2SEL:** Timer2 Counter mode, T2 pin input select
0: P1.0 (T2)
1: Slow clock/16

***Note**: See also Chapter 6 for more information on Timer2 interrupt enable and priority.*
***Note**: See also Chapter 7 for details on T2O pin output settings.*

8.3 Timer3

Timer3 works as a time-base counter, which generates interrupts periodically. It generates an interrupt flag (TF3) with the clock divided by 32768, 16384, 8192, …, 256 depending on the TM3PSC SFR. The Timer3 clock source is Slow clock (SRC or SXT). This is ideal for real-time-clock (RTC) functionality when the clock source is SXT.

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	TKIF	ADIF	–	IE2	P1IF	TF3
R/W	–	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.0 **TF3:** Timer3 Interrupt Flag
Set by H/W when Timer3 reaches TM3PSC setting cycles. Cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit. (***Note***)

Note: *S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.*

SFR **EFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX3	–	–	TM3PSC			VBGEN	–	ADCVREFS
R/W	–	–	R/W			R/W	–	R/W
Reset	–	–	0	0	0	0	0	0

EFh.5~3 **TM3PSC:** Timer3 Interrupt rate
000: Timer3 Interrupt rate is 32768 Slow clock cycle
001: Timer3 Interrupt rate is 16384 Slow clock cycle
010: Timer3 Interrupt rate is 8192 Slow clock cycle
011: Timer3 Interrupt rate is 4096 Slow clock cycle
100: Timer3 Interrupt rate is 2048 Slow clock cycle
101: Timer3 Interrupt rate is 1024 Slow clock cycle
110: Timer3 Interrupt rate is 512 Slow clock cycle
111: Timer3 Interrupt rate is 256 Slow clock cycle

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F8h.6 **CLRTM3:** Set 1 to clear Timer3, H/W auto clear it at next clock cycle.

Note: *also refer to Chapter 6 for more information about Timer3 Interrupt enable and priority.*

8.4 T0O and T2O Output Control

This device can generate various frequency waveform pin output (in CMOS or Open-Drain format) for Buzzer. The T0O and T2O waveform is divided by Timer0/Timer2 overflow signal. The T0O waveform is Timer0 overflow divided by 64, and T2O waveform is Timer2 overflow divided by 2. User can control their frequency by Timers auto reload speed. Set T0OE and T2OE SFRs can output these waveforms.

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1OE	PWM0OE	TCOE	T2OE	HSNK2EN	HSNK1EN	HSNK0EN	T0OE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	0

A6h.4 **T2OE:** Timer2 signal output (T2O) control
0: Disable Timer2 overflow divided by 2 output to P1.0
1: Enable Timer2 overflow divided by 2 output to P1.0

A6h.0 **T0OE:** Timer0 signal output (T0O) control
0: Disable Timer0 overflow divided by 64 output to P3.4
1: Enable Timer0 overflow divided by 64 output to P3.4

9. UARTs

This Chip has two UARTs, UART1 and UART2.

The **UART1** uses SCON and SBUF SFRs. SCON is the control register, SBUF is the data register. Data is written to SBUF for transmission and SBUF is read to obtain received data. The received data and transmitted data registers are completely independent. In addition to standard 8051's full duplex mode, this chip also provides one wire mode. If the UART1W bit is set, both transmit and receive data use P3.1 pin.

The **UART2** uses SCON2 and SBUF2 SFRs. SCON2 is the control register, SBUF2 is the data register. Data is written to SBUF2 for transmission and SBUF2 is read to obtain received data. The received data and transmitted data registers are completely independent. The UART2 supports most of the functions of UART, but it does not support Mode0 and Mode2, it also does not support Timer2 and one wire UART mode. On other hand, the option of SMOD is not use for UART2. UART2 double baud rate is always enabled.

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.7 **SMOD:** UART1 double baud rate control bit
0: Disable UART1 double baud rate
1: Enable UART1 double baud rate

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	–	WDTPSC		ADCKS		–	–
R/W	R/W	–	R/W		R/W		–	–
Reset	0	–	0	0	0	0	–	–

94h.7 **UART1W:** One wire UART1 mode enable, both TXD/RXD use P3.1 pin
0: Disable one wire UART1 mode
1: Enable one wire UART1 mode

SFR **98h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

98h.7~6 **SM0,SM1:** UART1 serial port mode select bit 0,1
00: Mode0: 8 bit shift register, Baud Rate=F_{SYSCLK}/2
01: Mode1: 8 bit UART1, Baud Rate is variable
10: Mode2: 9 bit UART1, Baud Rate=F_{SYSCLK}/32 or/64
11: Mode3: 9 bit UART1, Baud Rate is variable

98h.5 **SM2:** Serial port mode select bit 2
SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

98h.4 **REN:** UART1 reception enable
0: Disable reception
1: Enable reception

98h.3 **TB8:** Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3

98h.2 **RB8:** Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit is Mode 1 if SM2=0

98h.1 **TI:** Transmit interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.

98h.0 **RI:** Receive interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

SFR **99h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF	SBUF							
R/W	R/W							
Reset	–	–	–	–	–	–	–	–

99h.7~0 **SBUF:** UART1 transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

SFR **8Eh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON2	SM	–	–	REN2	TB82	RB82	TI2	RI2
R/W	R/W	–	–	R/W	R/W	R/W	R/W	R/W
Reset	0	–	–	0	0	0	0	0

8Eh.7 **SM:** UART2 Serial port mode select bit
0: Mode1: 8 bit UART2, Baud Rate is variable
1: Mode3: 9 bit UART2, Baud Rate is variable
(UART2 does not support Mode0/Mode2)

8Eh.4 **REN2:** UART2 reception enable
0: Disable reception
1: Enable reception

8Eh.3 **TB82:** Transmit Bit 8, the ninth bit to be transmitted in Mode 3

8Eh.2 **RB82:** Receive Bit 8, contains the ninth bit that was received in Mode3

8Eh.1 **TI2:** Transmit interrupt flag
Set by H/W at the beginning of the stop bit in Mode 1 & 3. Must be cleared by S/W.

8Eh.0 **RI2:** Receive interrupt flag
Set by H/W at the sampling point of the stop bit in Mode 1 & 3. Must be cleared by S/W.

SFR **8Fh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF2	SBUF2							
R/W	R/W							
Reset	–	–	–	–	–	–	–	–

8Fh.7~0 **SBUF2:** UART2 transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

F_{SYSCLK} denotes System clock frequency, the UART baud rate is calculated as below.

- **Mode 0: (UART2 invalid)**
  Baud Rate=$F_{SYSCLK}/2$
- **Mode 1, 3:** if using Timer1 auto reload mode
  Baud Rate= (SMOD + 1) x F_{SYSCLK}/ (32 x 2 x (256 – TH1))
- **Mode 1, 3:** if using Timer2 **(UART2 invalid)**
  Baud Rate=Timer2 overflow rate/16 = F_{SYSCLK}/ (32 x (65536 – RCP2H, RCP2L))
- **Mode 2: (UART2 invalid)**
  Baud Rate= (SMOD + 1) x $F_{SYSCLK}/64$

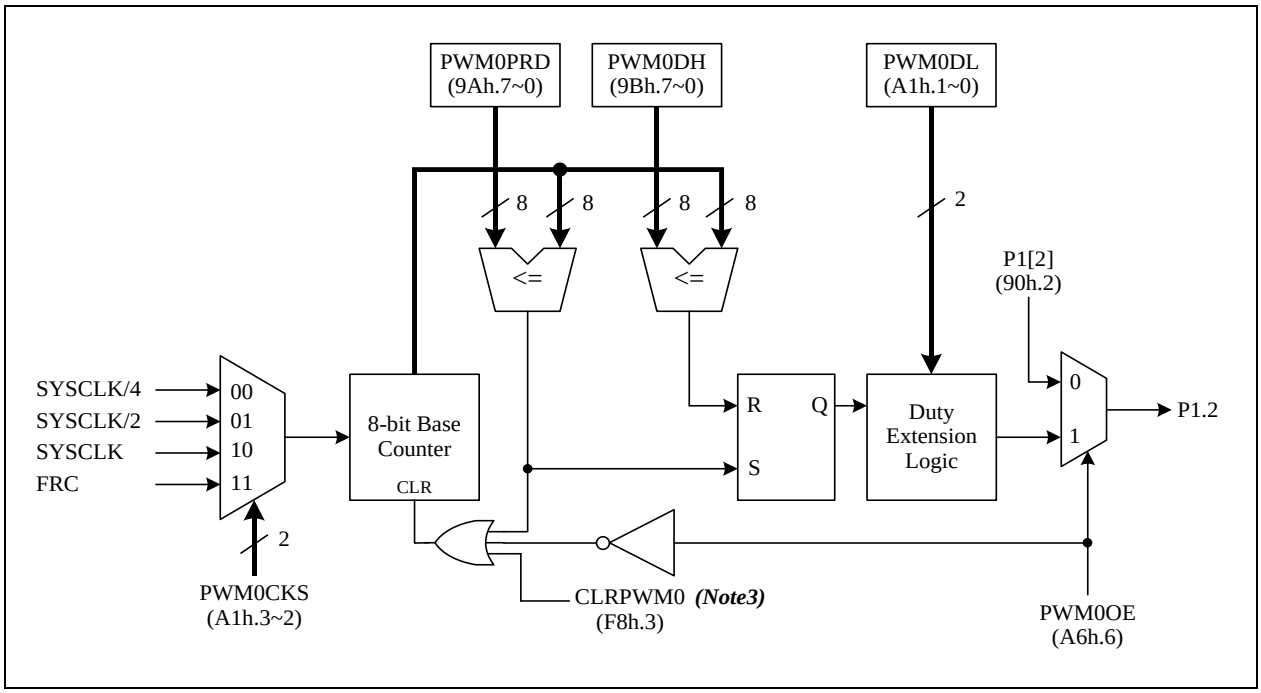
Note: *also refer to Chapter 6 for more information about UART Interrupt enable and priority.*
Note: *also refer to Chapter 8 for more information about how Timer2 controls UART clock.*

10. PWMs

The Chip has three independent PWM modules, PWM0, PWM1 and PWM2. The PWM can generate a fixed frequency waveform with 1024 duty resolution on the basis of the PWM clock. The PWM clock can select FRC or F_{SYSCLK} divided by 1, 2, or 4 as its clock source. A spread LSB technique allows PWM to run its frequency at the "PWM clock divided by 256" instead of at the "PWM clock divided by 1024", which means the PWM is four times faster than normal. The advantage of a higher PWM frequency is that the post RC filter can transform the PWM signal to a more stable DC voltage level.

The PWM output signal resets to a low level whenever the 8-bit base counter matches the 8-bit MSB of the PWM duty register. When the base counter rolls over, the 2-bit LSB of the PWM duty register decides whether to set the PWM output signal high immediately or set it high after one clock cycle delay. The PWM period can be set by writing the period value to the 8-bit PWM period register.

The pin mode SFR controls the PWM output waveform format. Mode1 makes the PWM open drain output and Mode2 makes the PWM CMOS push-pull output. (***see Chapter 7***)



PWM0 Structure

Note: *the PWM1 and PWM2 are almost the same as the PWM0, except they have no clear control bit.*

SFR **9Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRD	PWM0PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

9Ah.7~0 **PWM0PRD:** PWM0 8-bit period register

SFR **9Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DH	PWM0DH							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

9Bh.7~0 **PWM0DH:** bits 9~2 of the PWM0 10-bit duty register

SFR **9Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRD	PWM1PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

9Ch.7~0 **PWM1PRD:** PWM1 8-bit period register

SFR **9Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DH	PWM1DH							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

9Dh.7~0 **PWM1DH:** bits 9~2 of the PWM1 10-bit duty register

SFR **A1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON	PWM1CKS		PWM1DL		PWM0CKS		PWM0DL	
R/W	R/W		R/W		R/W		R/W	
Reset	1	0	0	0	1	0	0	0

A1h.7~6 **PWM1CKS:** PWM1 clock source
- 00: $F_{SYSCLK}/4$
- 01: $F_{SYSCLK}/2$
- 10: F_{SYSCLK}
- 11: FRC

A1h.5~4 **PWM1DL:** bits 1~0 of the PWM1 10-bit duty register

A1h.3~2 **PWM0CKS:** PWM0 clock source
- 00: $F_{SYSCLK}/4$
- 01: $F_{SYSCLK}/2$
- 10: F_{SYSCLK}
- 11: FRC

A1h.1~0 **PWM0DL:** bits 1~0 of the PWM0 10-bit duty register

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1OE	PWM0OE	TCOE	T2OE	HSNK2EN	HSNK1EN	HSNK0EN	T0OE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	0

A6h.7 **PWM1OE:** PWM1 control
- 0: PWM1 disable
- 1: PWM1 enable and signal output to P1.3 pin

A6h.6 **PWM0OE:** PWM0 control
- 0: PWM0 disable
- 1: PWM0 enable and signal output to P1.2 pin

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F8h.3 **CLRPWM0:** PWM0 clear enable
- 0: PWM0 is running
- 1: PWM0 is cleared and held

SFR **9Eh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2PRD	PWM2PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

9Eh.7~0 **PWM2PRD:** PWM2 8-bit period register

SFR **9Fh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2DH	PWM2DH							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

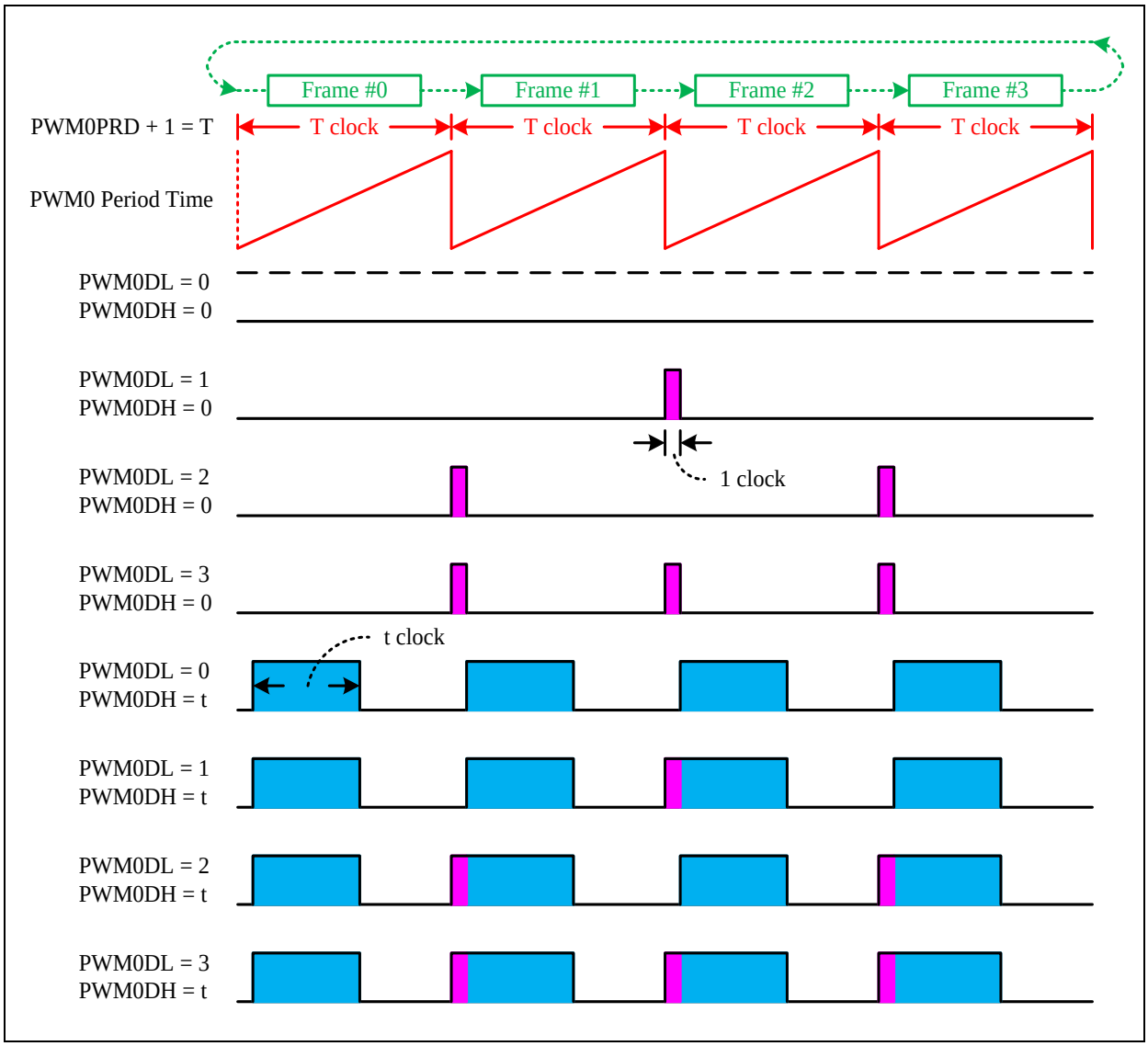
9Fh.7~0 **PWM2DH:** bits 9~2 of the PWM2 10-bit duty register

SFR **A7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON2	–	–	–	PWM2OE	PWM2CKS		PWM2DL	
R/W	–	–	–	R/W	R/W		R/W	
Reset	–	–	–	0	1	0	0	0

A7h.4 **PWM2OE:** PWM1 control
0: PWM2 disable
1: PWM2 enable and signal output to P1.6 pin

A7h.3~2 **PWM2CKS:** PWM2 clock source
00: $F_{SYSCLK}/4$
01: $F_{SYSCLK}/2$
10: F_{SYSCLK}
11: FRC

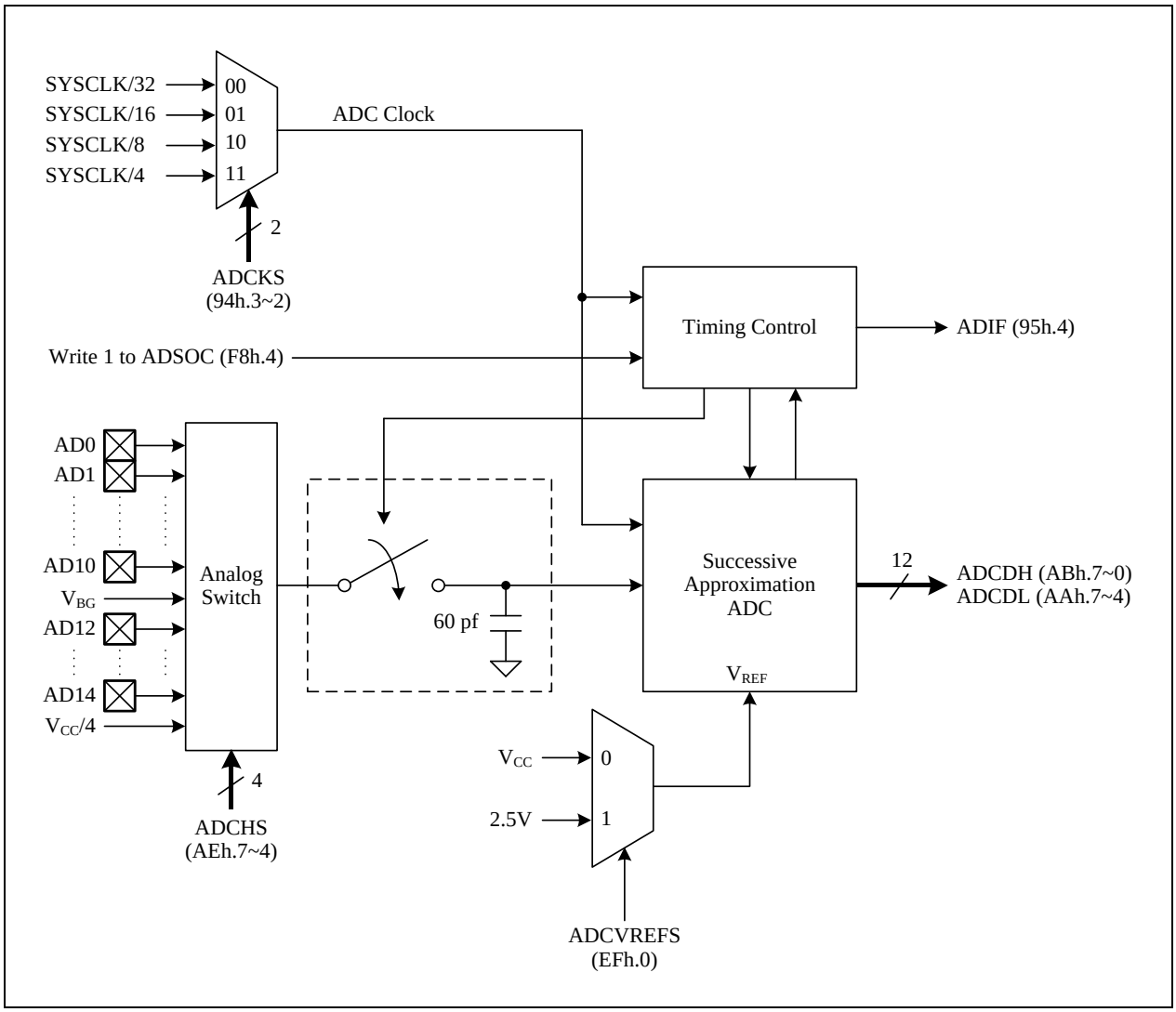
A7h.1~0 **PWM2DL:** bits 1~0 of the PWM2 10-bit duty register



PWM Waveform

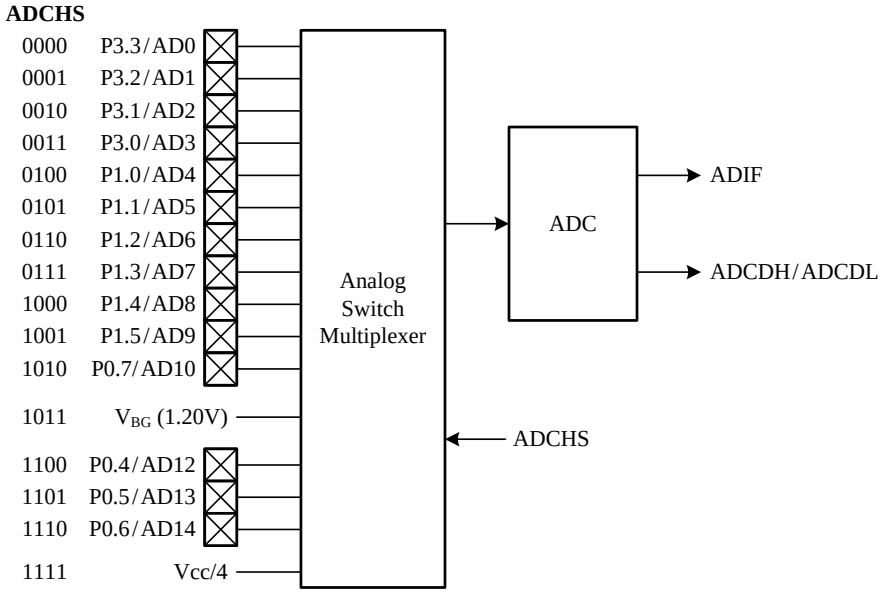
11. ADC

The Chip offers a 12-bit ADC consisting of a 16-channel analog input multiplexer, control register, clock generator, 12-bit successive approximation register, and output data register. To use the ADC, set the ADCKS bit first to choose a proper ADC clock frequency, which must be less than 1 MHz. Then, launch the ADC conversion by setting the ADSOC bit, and H/W will automatic clear it at the end of the conversion. After the end of the conversion, H/W will set the ADIF bit and generate an interrupt if an ADC interrupt is enabled. The ADIF bit can be cleared by writing 0 to this bit or 1 to the ADSOC bit. Because certain channels are shared with the Touch Key, the ADC channel must be configured differently from the Touch Key channel to avoid affecting the channel input sensitivity. There are two ADC reference volts (V_{REF}) can be selected by setting ADCVREFS. The analog input level must remain within the range from V_{SS} to V_{REF}.



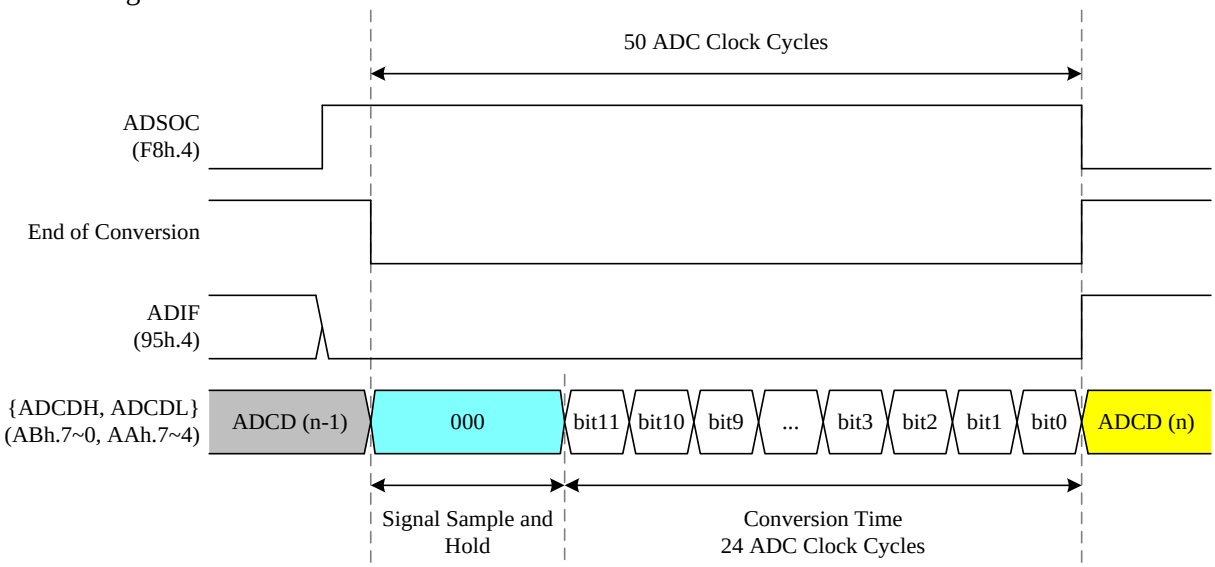
11.1 ADC Channels

The 12-bit ADC has a total of 16 channels, designated AD0~AD10, AD12~AD14, V_{CC}/4, and V_{BG}. The ADC channels are connected to the analog input pins via the analog switch multiplexer. The analog switch multiplexer is controlled by the ADCHS register. The Chip offers up to 14 analog input pins, designated AD0~AD10 and AD12~AD14. In addition, there are two analog input pins for voltage reference connections. When ADCHS is set to 1111b, the analog input will connect to V_{CC}/4, and when ADCHS is set to 1011b, the analog input will connect to V_{BG}. V_{BG} is an internal voltage reference at 1.20V. After the ADCHS is set, the ADC module is connected to the I/O port through the selection of ADCHS. If the I/O port is used as Touch Key, it will affect the Touch Key function. Therefore, when the ADC is not in use, it is recommended to set the ADCHS to 1111b (V_{CC}/4) or 1011b (V_{BG}) to disconnect the ADC module from the I/O port.



11.2 ADC Conversion Time

The conversion time is the time required for the ADC to convert the voltage. The ADC requires two ADC clock cycles to convert each bit and several clock cycles to sample and hold the input voltage. A total of 50 ADC clock cycles are required to perform the complete conversion. When the conversion time is complete, the ADIF interrupt flag is set by H/W, and the result is loaded into the ADCDH and ADCDL registers of the 12-bit A/D result.



SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	–	WDTPSC		ADCKS		–	–
R/W	R/W	–	R/W		R/W		–	–
Reset	0	–	0	0	0	0	–	–

94h.3~2 **ADCKS:** ADC clock rate select

00: F_{SYSCLK}/32
01: F_{SYSCLK}/16
10: F_{SYSCLK}/8
11: F_{SYSCLK}/4

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	TKIF	ADIF	–	IE2	P1IF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.4 **ADIF:** ADC interrupt flag

Set by H/W at the end of ADC conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag. (***Note***)

SFR **AAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADTKDT	ADCDL				TKDH			
R/W	R				R			
Reset	–	–	–	–	–	–	–	–

AAh.7~4 **ADCDL:** ADC data bit 3~0

SFR **ABh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDH	ADCDH							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ABh.7~0 **ADCDH:** ADC data bit 11~4

SFR **B6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCHS	–	–	–	–	ADCHS			
R/W	–	–	–	–	R/W			
Reset	–	–	–	–	1	1	1	1

B6h.3~0 **ADCHS:** ADC channel select

0000: AD0 (P3.3)
0001: AD1 (P3.2)
0010: AD2 (P3.1)
0011: AD3 (P3.0)
0100: AD4 (P1.0)
0101: AD5 (P1.1)
0110: AD6 (P1.2)
0111: AD7 (P1.3)
1000: AD8 (P1.4)
1001: AD9 (P1.5)
1010: AD10 (P0.7)
1011: V_{BG} (Internal Bandgap Reference Voltage)
1100: AD12 (P0.4)
1101: AD13 (P0.5)
1110: AD14 (P0.6)
1111: V_{CC}/4

Note: *FW must turn off Bandgap to obtain Tiny Current (ADCHS ≠1011b)*

SFR **EFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX3	–	–	TM3PSC			VBGEN	–	ADCVREFS
R/W	–	–	R/W			R/W	–	R/W
Reset	–	–	0	0	0	0	0	0

EFh.1 **Reserved, Keep 0**

EFh.0 **ADCVREFS:** ADC reference voltage (V_{REF}) select

0: V_{CC}

1: 2.5V

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F8h.4 **ADSOC:** Start ADC conversion

Set the ADSOC bit to start ADC conversion, and the ADSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.

Note: *also refer to Chapter 6 for more information about ADC Interrupt enable and priority.*

Note: *also refer to Chapter 7 for more information about ADCinput channel setting.*

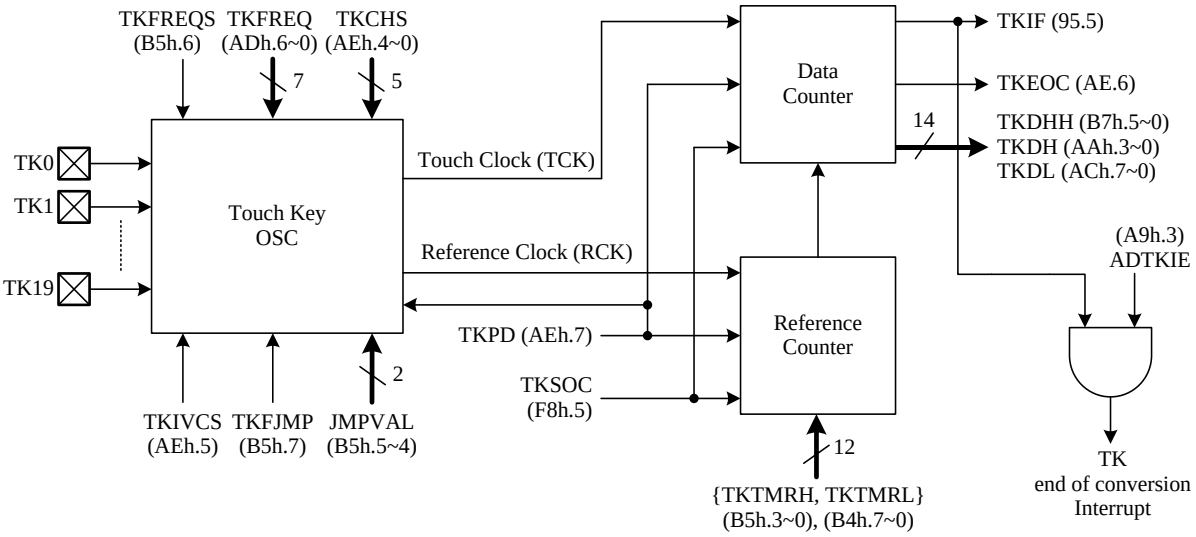
12. Touch Key (FN8276/78 only)

The Touch Key offers an easy, simple and reliable method to implement finger touch detection. The device support 19 channels touch key detection.

To use the Touch Key, user must setup the Pin Mode (***see Chapter 7***) correctly as below table. Setting Mode2 for an Idling Touch Key pin can CMOS output Low and reduce the mutual interference between the adjacent keys.

P0OEx / P1MODx / P3MODx setting for Touch Key	TK0~TK14, TK16~TK19
Pin is Touch Key, Idling	Drive Low
Pin is Touch Key, Scanning	

There are two oscillators: Reference Clock (RCK) and Touch Clock (TCK). They are connected to the Reference Counter and Data Counter respectively. The frequency of RCK can be adjusted by setting TKFREQ. Reference Counter is used to control conversion time. From starting touch key conversion to end, it will take 0 to 4096 RCK oscillation cycles by setting TKTMR. After end of conversion, user can get TKDATA (TKDHH, TKDL) from Data counter. TKDATA is affected by finger touching. As finger touching TCK is getting slower, the value of TKDATA is smaller than the no finger touching. According to the difference of TKDATA, user can check if it is touched of not. The frequency of TCK will adjust automatically by setting TKFJMP=1, otherwise it can be adjusted by TKFREQS and JMPVAL when TKFJMP=0.



Touch Key Structure

To start the Scanning, user assigns TKPD=0, then set the TKSOC bit to start touch key conversion, the TKSOC bit can be automatically cleared while end of conversion. However, if the SYSCLK is too slow, H/W might fail to clear TKSOC due to clock sampling rate. TKEOC=0 means conversion is in process. TKEOC=1 means the conversion is finish, and the touch key counting result is stored into the 14 bits Touch Key Data Counter TKDHH and TKDL.

There is an internal reference capacitor inside the Touch Key to simulate the behavior of the finger touching. Set TKCHS=15, it will forcefully switch to the internal reference capacitor, and start the touch key conversion to get the TKDATA. Because the internal capacitor has never been affected by water or mobile phones, it is very useful for comparing environmental background noise.

When TKPD=0 and TKCHS is set, the Touch Key module is connected to the I/O port through the selection of TKCHS. If the I/O port is used as other functions, it must be affected. Therefore, when the Touch Key module is not in use, it is recommended to set TKPD =1 to disconnect the TK module from the I/O port.

◇ Example:

```
MOV     TKCON,#000h         ; TKPD=0, TKCHS=0 (select TK0)

MOV     TKFREQ,#040h        ; Set an appropriate value for TK scanning

MOV     TKCON2,#084h        ; TKFJMP=1
MOV     TKTMRL,#000h        ; TKTMR=400h

MOV     INTFLG,#11011111b   ; clear TKIF
ORL     INTE1,#008h
ORL     IE,#080h

SETB    TKSOC
```

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	TKIF	ADIF	–	IE2	P1IF	TF3
R/W	–	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.5 **TKIF:** Touch Key Interrupt Flag
Set by H/W at the end of Touch Key conversion if SYSCLK is fast enough. S/W writes DFh to INTFLG or sets the TKSOC bit to clear this flag. (***Note***)

Note: *S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.*

SFR **B7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKDHH	–	–	TKDHH					
R/W	–	–	R					
Reset	–	–	–	–	–	–	–	–

B7h.5~0 **TKDHH**: Touch Key counter data bit 13~8

SFR **AAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADTKDT	ADCDL				TKDH			
R/W	R				R			
Reset	–	–	–	–	–	–	–	–

AAh.3~0 **TKDH:** Touch Key counter data bit 11~8

SFR **ACh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKDL	TKDL							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ACh.7~0 **TKDL:** Touch Key counter data bit 7~0

SFR **ADh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKFREQ	–	TKFREQ						
R/W	–	R/W						
Reset	–	1	0	0	0	0	0	0

ADh.6~0 **TKFREQ:** Touch Key oscillation capacitor adjustment
00: TKDATA is smallest
…
7F: TKDATA is biggest

SFR **AEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKCON	TKPD	TKEOC	TKIVCS	TKCHS				
R/W	R/W	R	R/W	R/W				
Reset	1	0	0	0	1	1	1	1

AEh.7 **TKPD:** Touch Key power down
0: Touch Key enable
1: Touch Key disable

AEh.6 **TKEOC:** Touch Key end of conversion flag, TKEOC may have 3uS delay after TKSOC=1, so F/W must wait enough time before polling this Flag.
0: Indicates conversion is in progress
1: Indicates conversion is finished

AEh.5 **TKIVCS**: Touch Key internal LDO voltage control
0:1.4V
1:1.8V

AEh.4~0 **TKCHS**: Touch Key channel select
00000: TK0 (P3.3)
00001: TK1 (P3.2)
00010: TK2 (P3.1)
00011: TK3 (P3.0)
00100: TK4 (P1.0)
00101: TK5 (P1.1)
00110: TK6 (P1.2)
00111: TK7 (P1.3)
01000: TK8 (P1.4)
01001: TK9 (P1.6)
01010: TK10 (P0.4)
01011: TK11 (P0.5)
01100: TK12 (P0.6)
01101: TK13 (P3.4)
01110: TK14 (P1.5)
01111: internal reference key
10000: TK16 (P1.7)
10001: TK17 (P3.6)
10010: TK18 (P3.5)
10011: TK19 (P3.7)

SFR **B4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKTMRL	TKTMRL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

B4h.7~0 **TKTMRL:** Touch Key reference counter data bit 7~0

SFR **B5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKCON2	TKFJMP	TKFREQS	JMPVAL		TKTMRH			
R/W	R/W	R/W	R/W		R/W			
Reset	0	0	0	0	0	0	0	0

B5h.7 **TKFJMP:** Touch Key clock frequency auto-change selection
0: fix frequency
1: auto-change

B5h.6 **TKFREQS:** Touch Key clock frequency select
0: slow frequency
1: fast frequency

B5h.5~4 **JMPVAL:** Touch Key clock frequency fine tune **(only available in TKFJMP=0)**
00: frequency is slowest
~
11: frequency is fastest

B5h.3~0 **TKTMRH**: Touch Key reference counter data bit 11~8

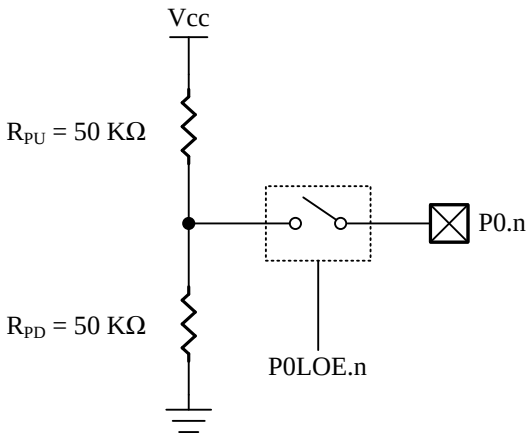
SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F8h.5 **TKSOC:** Touch Key Start of Conversion
Set 1 to start Touch Key conversion. If SYSCLK is fast enough, this bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.

Note: *also refer to Chapter 6 for more information about Touch Key Interrupt enable and priority.*

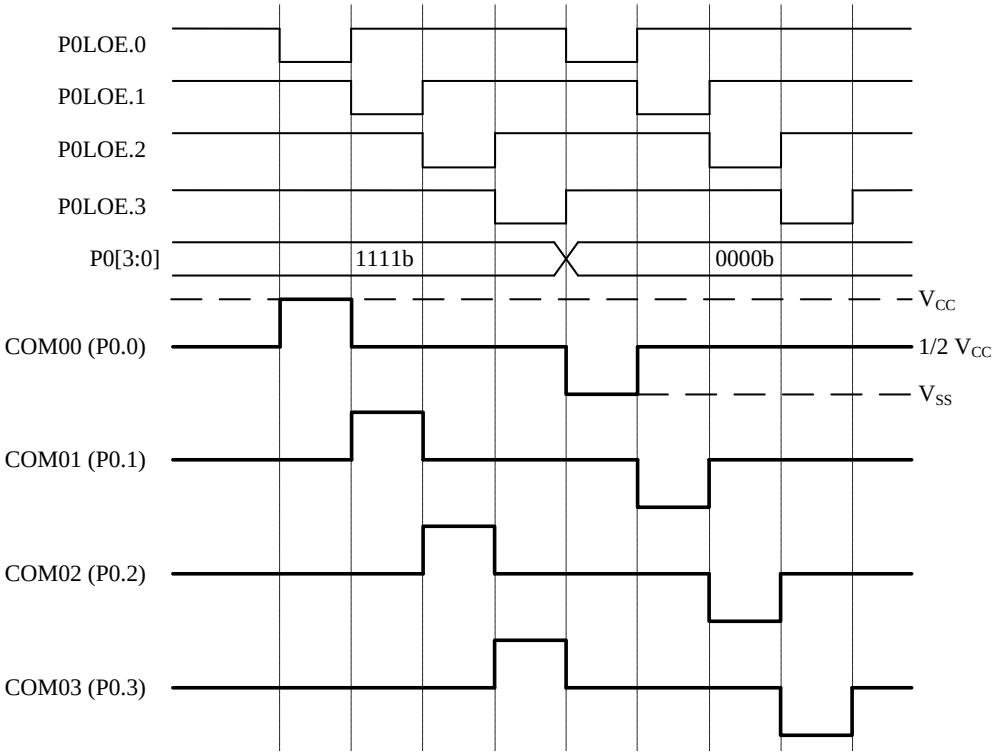
13. S/W Controller LCD Driver

The chip supports an S/W controlled method to driving LCD. Most of the IO pins can be the Common pins. User can flexibly adjust the Common pins and Segment pins. It is capable of driving the LCD panel with 144 dots (Max.) by 12 Commons (COM) and 12 Segments (SEG). The P0.0~P0.7 are used for Common pins COM00~COM07. The P1.0~P1.7 are used for Common pins COM10~COM17. The P3.0~P3.7 are used for Common pins COM30~COM37. Common pins are capable of driving 1/2 bias by setting the corresponding registers P0LOE, P1LOE or P3LOE. Refer to the following figures.



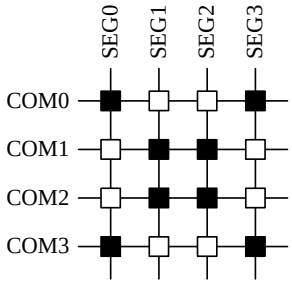
LCD COM00~07 Circuit

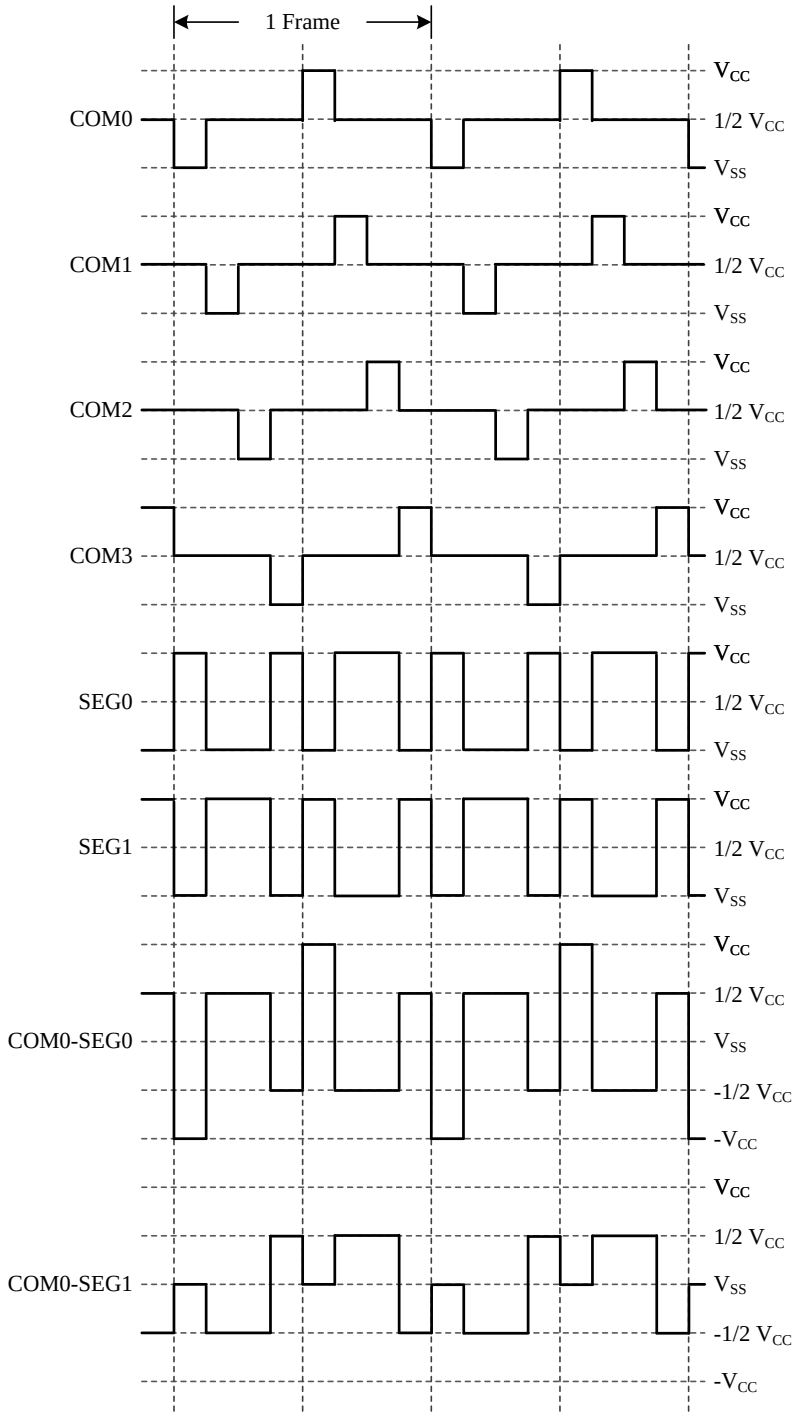
The frequency of any repeating waveform output on the COM pin can be used to represent the LCD frame rate. The figure below shows an LCD frame.



S/W Controlled LCD COM00~03 Scanning

1/4 Duty, 1/2 Bias Output Waveform





SFR **92h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0LOE	P0LOE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

92h.7~0 **P0LOE:** P0.7~P0.0 LCD 1/2 bias output enable control
0: Disable
1: Enable

SFR **D1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1LOE	P1LOE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

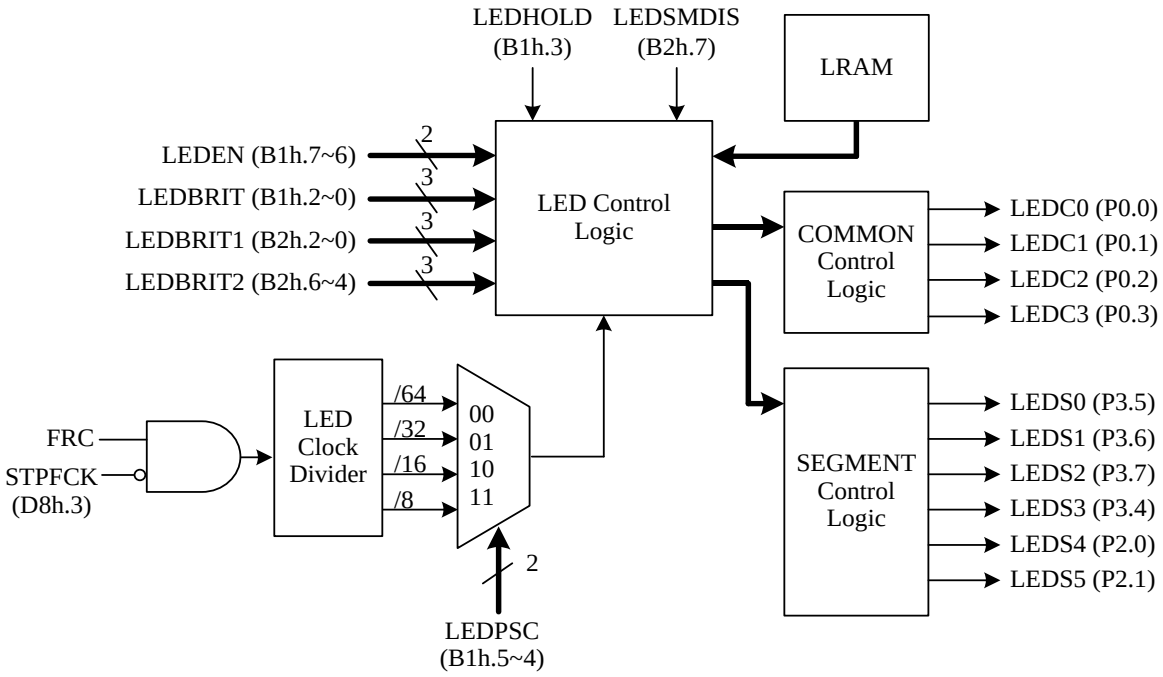
D1h.7~0 **P1LOE:** P1.7~P1.0 LCD 1/2 bias output enable control
0: Disable
1: Enable

SFR **D3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3LOE	P3LOE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D3h.7~0 **P3LOE:** P3.7~P3.0 LCD 1/2 bias output enable control
0: Disable
1: Enable

14. LED Controller/Driver

The chip supports a LED controller and driver by Matrix mode of operation. The LED Matrix mode can drive more number of LED pixels than the tradition mode, when they use the same number of pins. In this mode, it provides maximum 10 pins (LEDC0~C3, LEDS0~S5) to drive a LED module with 48 pixels. All 10 pins have a high sink current for driving LED directly. In the other hand, this LED controller also provides 3groups 8-level of brightness adjustment for all 10 pin. It can make the brightness smoother by setting the LEDSMDIS=0. To avoid LED flicker when the common signal is changing, the chip provides a dead time control. In the dead time period, segment pins will output a short inactive signal instead of changing the signal immediately. To start the LED scanning, it only has to set the LEDEN. Then H/W will control the Pin mode automatically. It also provides the scan hold function by setting LEDHOLD.



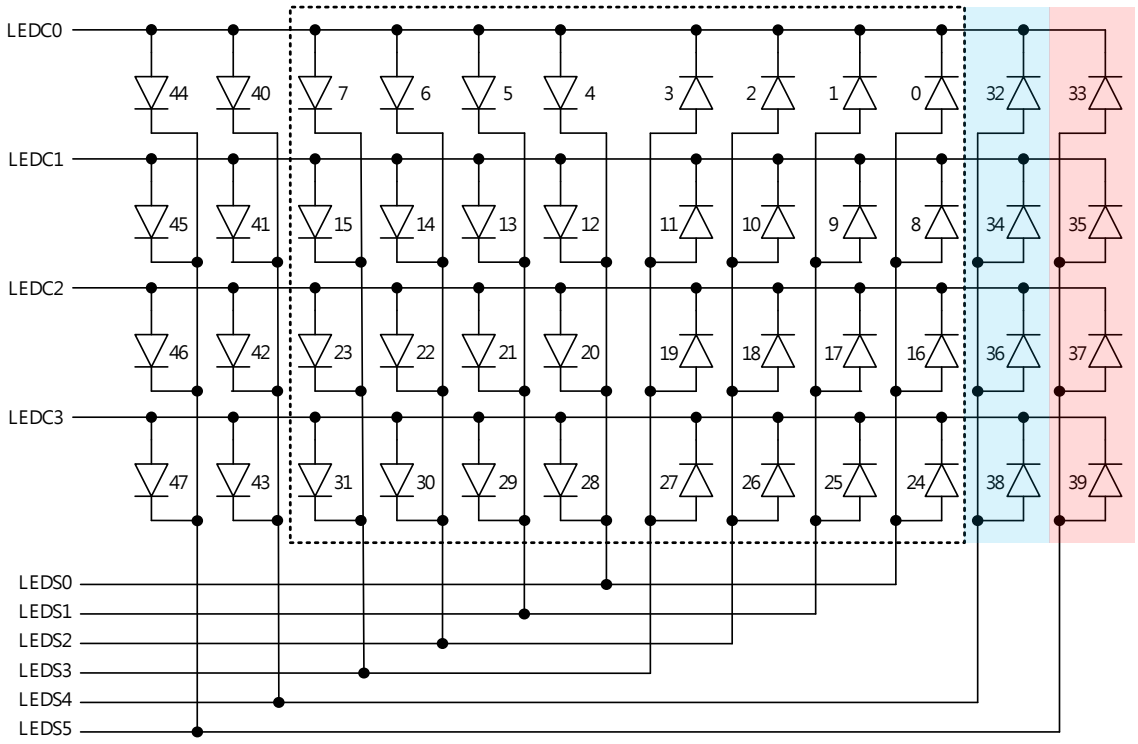
LEDEN	Duty	Matrix	Max pixels
0	Disable	-	-
1	1/8	4COM x 4SEG	32 (4x4x2)
2	Reserved	-	-
3	1/10	4COM x 6SEG	48 (4x6x2)

LRAM (External Data Memory)

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F000h	SEG3-COM0+	SEG2-COM0+	SEG1-COM0+	SEG0-COM0+	COM0-SEG3+	COM0-SEG2+	COM0-SEG1+	COM0-SEG0+
F001h	SEG3-COM1+	SEG2-COM1+	SEG1-COM1+	SEG0-COM1+	COM1-SEG3+	COM1-SEG2+	COM1-SEG1+	COM1-SEG0+
F002h	SEG3-COM2+	SEG2-COM2+	SEG1-COM2+	SEG0-COM2+	COM2-SEG3+	COM2-SEG2+	COM2-SEG1+	COM2-SEG0+
F003h	SEG3-COM3+	SEG2-COM3+	SEG1-COM3+	SEG0-COM3+	COM3-SEG3+	COM3-SEG2+	COM3-SEG1+	COM3-SEG0+
F004h	COM3-SEG5+	COM3-SEG4+	COM2-SEG5+	COM2-SEG4+	COM1-SEG5+	COM1-SEG4+	COM0-SEG5+	COM0-SEG4+
F005h	SEG5-COM3+	SEG5-COM2+	SEG5-COM1+	SEG5-COM0+	SEG4-COM3+	SEG4-COM2+	SEG4-COM1+	SEG4-COM0+

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F000h	7	6	5	4	3	2	1	0
F001h	15	14	13	12	11	10	9	8
F002h	23	22	21	20	19	18	17	16
F003h	31	30	29	28	27	26	25	24
F004h	39	38	37	36	35	34	33	32
F005h	47	46	45	44	43	42	41	40

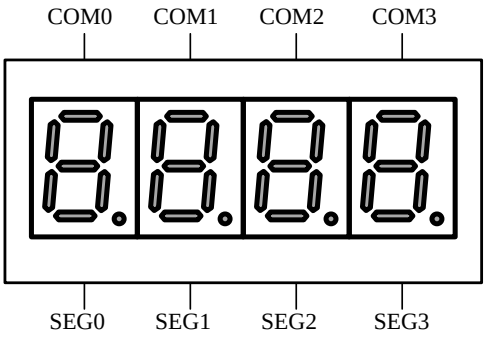
LED matrix mode corresponding display configuration table

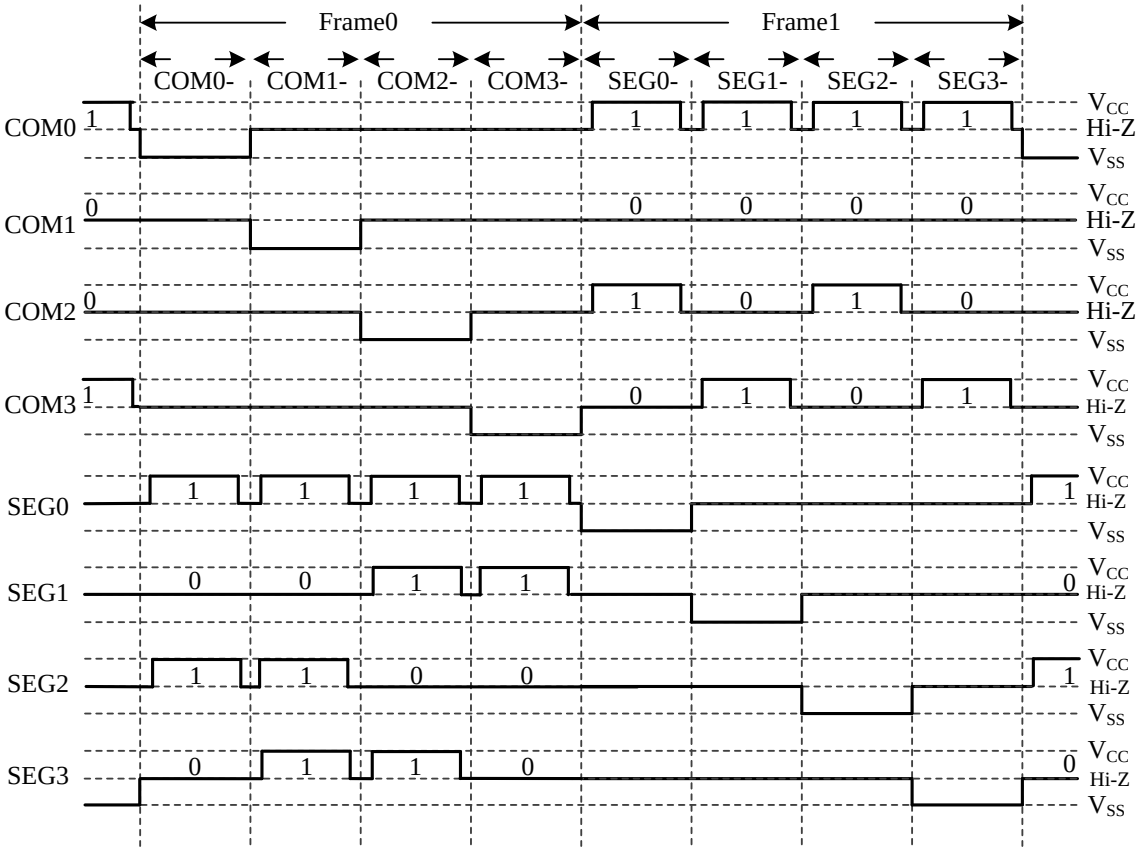


LED 4*6 matrix mode

***Note*:** *LEDBRIT (B1h.2~0) : LED number 0~31, 40~47 brightness control*
LEDBRIT1 (B2h.2~0): LED number 32, 34, 36, 38 brightness control
LEDBRIT2 (B2h.6~4): LED number 33, 35, 37, 39 brightness control

Application Circuit: 4COM x 4SEG (1/8 Duty)





◇ Example:

```
MOV     DPTR,#0F000h    ; LEDRAM0
MOV     A,#0FFh
MOVX    @DPTR, A        ; F000h = FFh

MOV     LEDCON,#056h    ; LED duty = 1/8
                        ; LEDPSC = FRC/32
                        ; Brightness=6
```

SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LEDCON	LEDEN		LEDPSC		LEDHOLD	LEDBRIT		
R/W	R/W		R/W		R/W	R/W		
Reset	0	0	0	0	0	1	0	0

B1h.7~6 **LEDEN:** LED enable and duty select
00: LED disable
01: LED 1/8 duty (4COM x 4SEG)
10: Reserved
11: LED 1/10 duty (4COM x 6SEG)

B1h.5~4 **LEDPSC:** LED clock prescaler select
00: LED clock is FRC divided by 64
01: LED clock is FRC divided by 32
10: LED clock is FRC divided by 16
11: LED clock is FRC divided by 8

B1h.3 **LEDHOLD:** LED hold function
0:Release to run LED scanning
1: Hold LED scanning, all LED pins state are Hi-Z

B1h.2~0 **LEDBRIT:** LED COM0+ ~ COM3+ & SEG0+ ~ SEG3+ (LED number 0~31, 40~47) brightness select
000: Level 0 (Darkest)
…
111: Level 7 (Brightest)

SFR **B2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LEDCON2	LEDSMDIS	LEDBRIT2			–	LEDBRIT1		
R/W	R/W	R/W			–	R/W		
Reset	0	1	0	0	–	1	0	0

B2h.7 **LEDSMDIS:** LED brightness smooth control
0: Brightness smooth enable
1: Brightness smooth disable

B2h.6~4 **LEDBRIT2:** LED SEG5+ (LED number 33, 35, 37, 39) brightness select
000: Level 0 (Darkest)
…
111: Level 7 (Brightest)

B2h.2~0 **LEDBRIT1:** LED SEG4+ (LED number 32, 34, 36, 38) brightness select
000: Level 0 (Darkest)
…
111: Level 7 (Brightest)

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	1	0	0	0	1	1

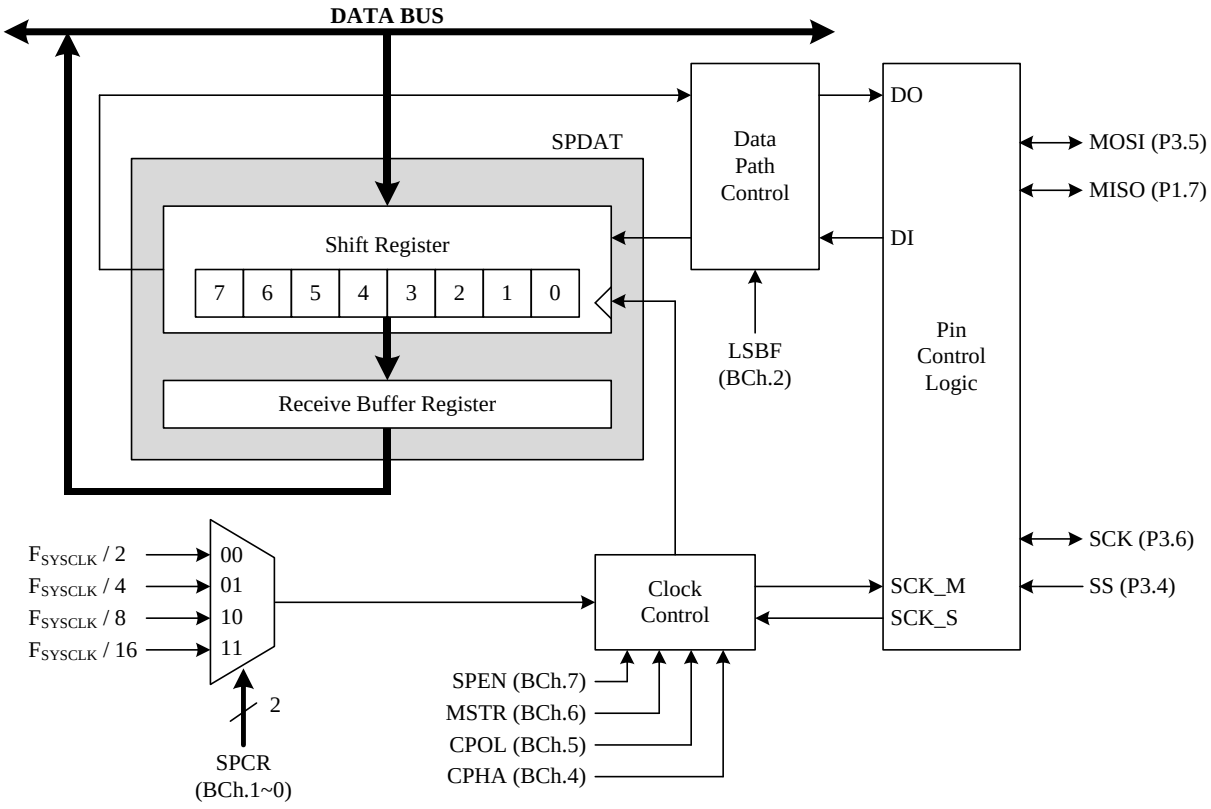
D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.

15. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) module is capable of full-duplex, synchronous, serial communication between the MCU and peripheral devices. The peripheral devices can be other MCUs, A/D converter, sensors, or flash memory, etc. The SPI runs at a clock rate up to the system clock divided by two. Firmware can read the status flags, or the operation can be interrupt driven. Following figure shows the SPI system block diagram.

The features of the SPI module include:

- Master or Slave mode operation
- 3-wire or 4-wire mode operation
- Full-duplex operation
- Programmable transmit bit rate
- Single buffer receive
- Serial clock phase and polarity options
- MSB-first or LSB-first shifting selectable



SPI Function Pin	P1/P3 Mode	P1.n/P3.n SFR data
Master Mode, MISO	Mode1	1
Master Mode, SCK, MOSI	Mode2	X
Slave Mode, MISO	Mode2	X
Slave Mode, SCK, MOSI	Mode1	1
SS	Mode1	1

Pin Mode Setting for SPI

The four signals used by SPI are described below. The MOSI (P3.5) signal is an output from a Master Device and an input to Slave Devices. The signal is an output when SPI is operating in Master mode and an input when SPI is operating in Slave mode. The MISO (P1.7) signal is an output from a Slave Device and an input to a Master Device. The signal is an input when SPI is operating in Master mode and an output when SPI is operating in Slave mode. Data is transferred most-significant bit (MSB) or least-significant bit (LSB) first by setting the LSBF bit. The SCK (P3.6) signal is an output from a Master Device and an input to Slave Devices. It is used to synchronize the data on the MOSI and MISO lines of Master and Slave. SPI generates the signal with eight programmable clock rates in Master mode. The SS (P3.4) signal is a low active slave select pin. In 4-wire Slave mode, the signal is ignored when the Slave is not selected (SS=1). The SS is ignored when the SSDIS in SPCON is set in both Master and Slave modes. In Slave mode and the SSDIS is clear, the SPI active when SS stay low. For multiple-slave mode, only one slave device is selected at a time to avoid bus collision on the MISO line. In Master mode and the SSDIS is cleared, the MODF in SPSTA is set when this signal is low. For multiple-master mode, enable SS line to avoid multiple driving on MOSI and SCK lines from multiple masters.

Master Mode

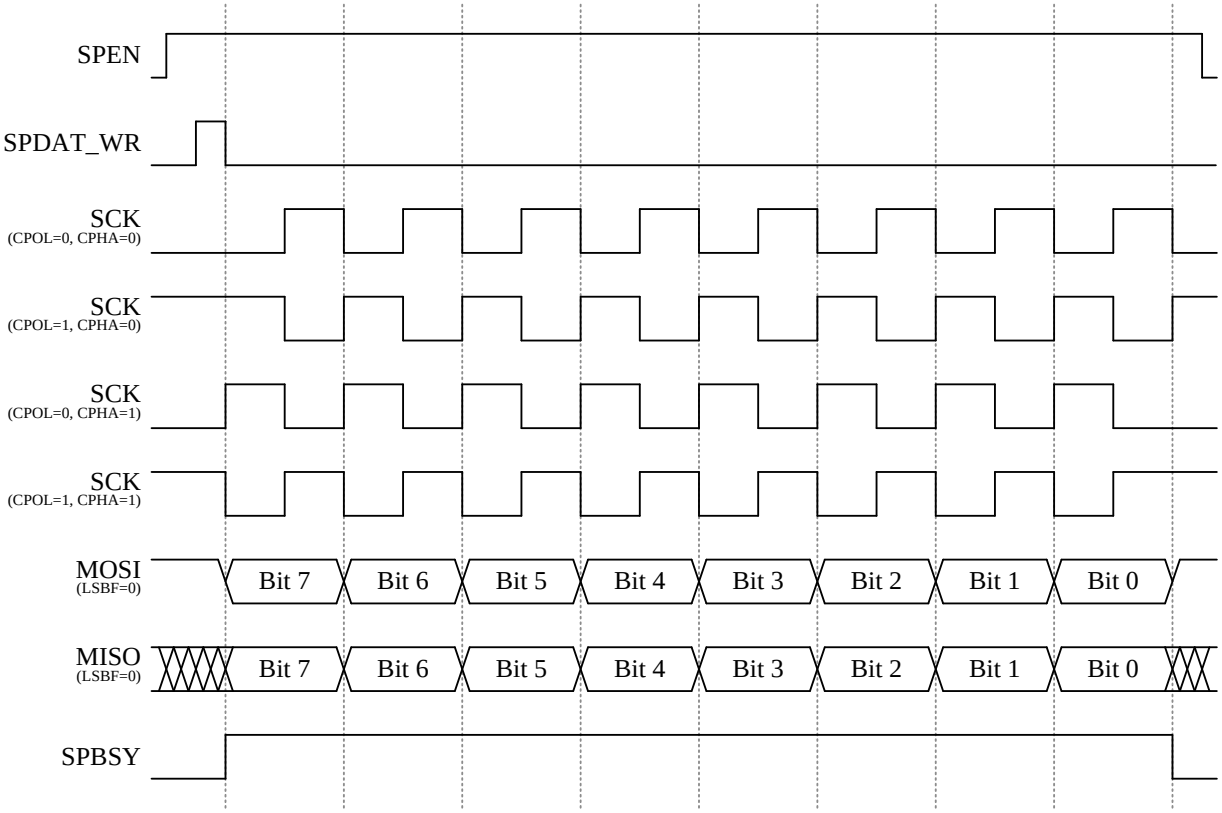
The SPI operates in Master mode by setting the MSTR bit in the SPCON. To start transmit, writing a data to the SPDAT. If the SPBSY bit is cleared, the data will be transferred to the shift register and starts shift out on the MOSI line. The data of the slave shift in from the MISO line at the same time. When the SPIF bit in the SPSTA becomes set at the end of the transfer, the receive data is written to receiver buffer and the RCVBF bit in the SPSTA is set. To prevent an overrun condition, software must read the SPDAT before next byte enters the shift register. The SPBSY bit will be set when writing a data to SPDAT to start transmit, and be cleared at the end of the eighth SCK period in Master mode.

Slave Mode

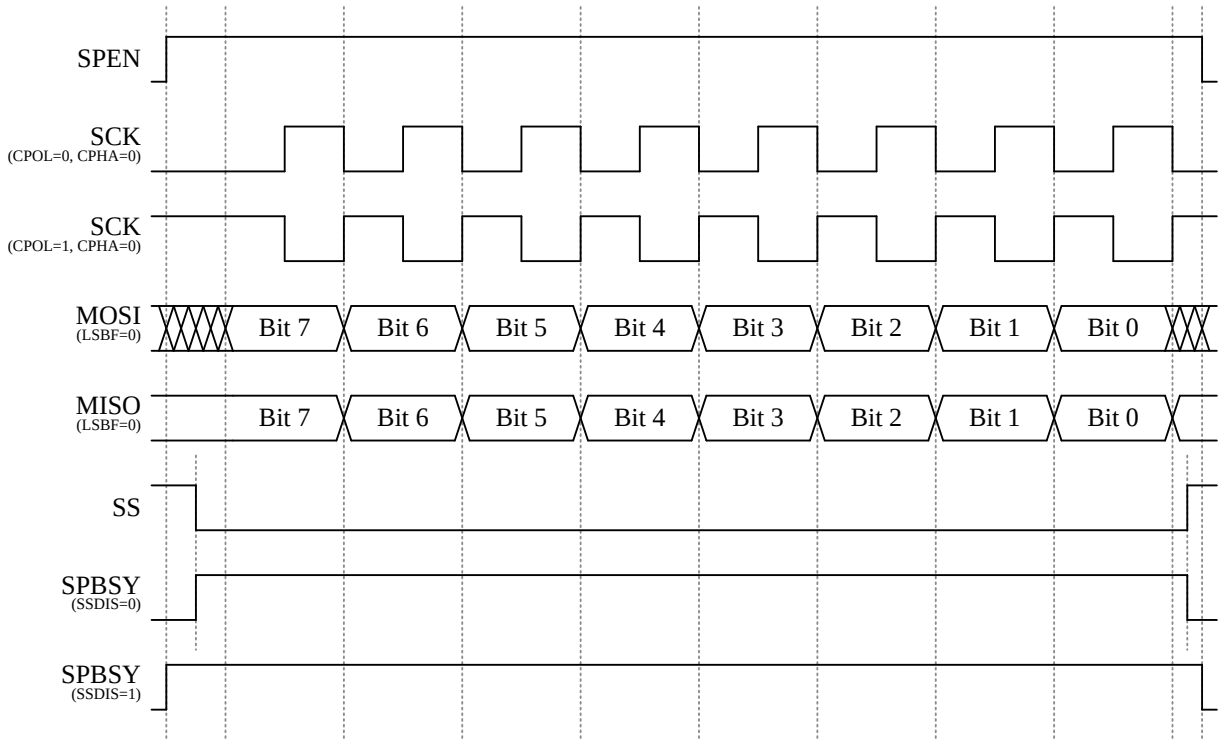
The SPI operates in Slave mode by clearing the MSTR bit in the SPCON. If the SSDIS is cleared, the transmission will start when the SS become low and remain low until the end of a data transfer. If the SSDIS is set, the transmission will start when the SPEN bit in the SPCON is set, and don't care the SS. The data from a master will shift into the shift register through the MOSI line, and shift out from the shift register on the MISO line. When a byte enters the shift register, the data will be transferred to receiver buffer if the RCVBF is cleared. If the RCVBF is set, the newer receive data will not be transferred to receiver buffer and the RCVOVF bit is set. After a byte enters the shift register, the SPIF and RCVBF bits are set. To prevent an overrun condition, software must read the SPDAT or write 0 to RCVBF before next byte enters the shift register. **The maximum SCK frequency allowed in Slave mode is $F_{SYSCLK}/4$.** In Slave mode, the SPBSY bit refers to the SS pin when the SSDIS bit is cleared, and refer to the SPEN bit when SSDIS bit is set.

Serial Clock

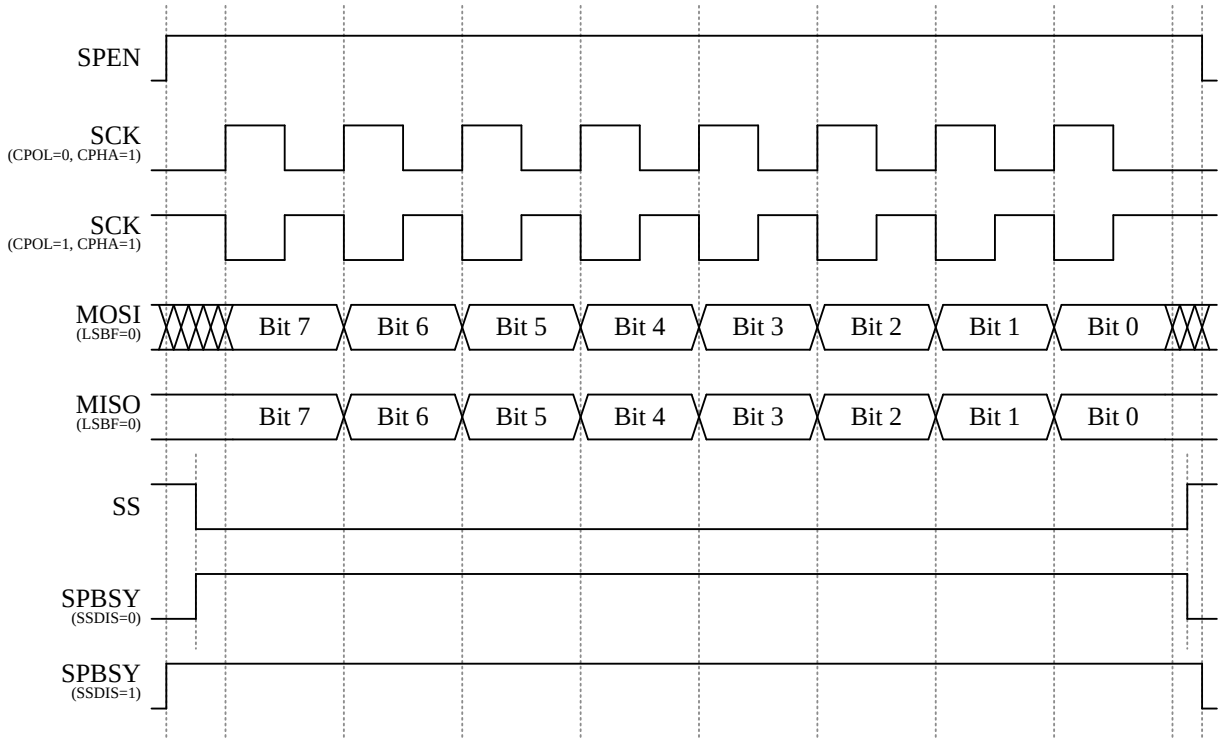
The SPI has four clock types by setting the CPOL and CPHA bits in the SPCON register. The CPOL bit defines the level of the SCK in SPI idle state. The level of the SCK in idle state is low when the CPOL bit is cleared, and is high when the CPOL bit is set. The CPHA bit defines the edges used to sample and shift data. The SPI sample data on the first edge of SCK period and shift data on the second edge of SCK period when the CPHA bit is cleared. The SPI sample data on the second edge of SCK period and shift data on first edge of SCK period when the CPHA bit is set. The figures below show the detail timing in Master and Slave modes. Both Master and Slave devices must be configured to use the same clock type before the SPEN bit is set. The SPCR controls the Master mode serial clock frequency. This register is ignored when operating in Slave mode. The SPI clock can select System clock divided by 2, 4, 8, or 16 in Master mode.



Master Mode Timing



Slave Mode Timing (CPHA=0)



Slave Mode Timing (CPHA=1)

In both Master and Slave modes, the SPIF bit is set by H/W at the end of a data transfer and generates an interrupt if SPI interrupt is enabled. The SPIF bit is cleared automatically when the program performs the interrupt service routines. S/W can also write 0 to clear this flag. If write data to SPDAT when the SPBSY is set, the WCOL bit will be set by H/W and generates an interrupt if SPI interrupt is enabled. When this occurs, the data write to SPDAT will be ignored, and shift register will not be written. Write 0 to this bit or when SPBSY is cleared and rewrite data to SPDAT will clear this flag. The MODF bit is set when SSDIS is cleared and SS pin is pulled low in Master mode. If SPI interrupt is enabled, an interrupt will be generated. When this bit is set, the SPEN and MSTR in SPCON will be cleared by H/W. Write 0 to this bit will clear this flag.

SFR **BCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPCON	SPEN	MSTR	CPOL	CPHA	SSDIS	LSBF	SPCR	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

BCh.7 **SPEN:** SPI enable
0: SPI disable
1: SPI enable

BCh.6 **MSTR:** Master mode enable
0: Slave mode
1: Master mode

BCh.5 **CPOL:** SPI clock polarity
0: SCK is low in idle state
1: SCK is high in idle state

BCh.4 **CPHA:** SPI clock phase
0: Data sample on first edge of SCK period
1: Data sample on second edge of SCK period

BCh.3 **SSDIS:** SS pin disable
0: Enable SS pin
1: Disable SS pin

BCh.2 **LSBF:** LSB first
0: MSB first
1: LSB first

BCh.1~0 **SPCR:** SPI clock rate
00: $F_{SYSCLK}/2$
01: $F_{SYSCLK}/4$
10: $F_{SYSCLK}/8$
11: $F_{SYSCLK}/16$

SFR **BDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPSTA	SPIF	WCOL	MODF	RCVOVF	RCVBF	SPBSY	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R	–	–
Reset	0	0	0	0	0	0	–	–

BDh.7 **SPIF:** SPI interrupt flag
This is set by H/W at the end of a data transfer. Cleared by H/W when an interrupt is vectored into. Writing 0 to this bit will clear this flag.

BDh.6 **WCOL:** Write collision interrupt flag
Set by H/W if write data to SPDAT when SPBSY is set. Write 0 to this bit or rewrite data to SPDAT when SPBSY is cleared will clear this flag.

BDh.5 **MODF:** Mode fault interrupt flag
Set by H/W when SSDIS is cleared and SS pin is pulled low in Master mode. Write 0 to this bit will clear this flag. When this bit is set, the SPEN and MSTR in SPCON will be cleared by H/W.

BDh.4 **RCVOVF:** Received buffer overrun flag
Set by H/W at the end of a data transfer and RCVBF is set. Write 0 to this bit or read SPDAT register will clear this flag.

BDh.3 **RCVBF:** Receive buffer full flag
Set by H/W at the end of a data transfer. Write 0 to this bit or read SPDAT register will clear this flag.

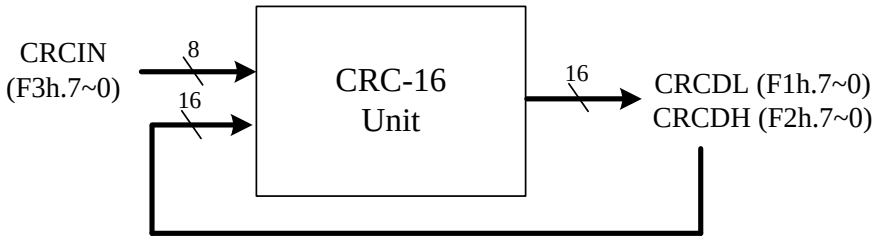
BDh.2 **SPBSY:** SPI busy flag
Set by H/W when a SPI transfer is in progress.

SFR **BEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPDAT	SPDAT							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

BEh.7~0 **SPDAT:** SPI transmit and receive data
The SPDAT register is used to transmit and receive data. Writing data to SPDAT place the data into shift register and start a transfer when in master mode. Reading SPDAT returns the contents of the receive buffer.

16. Cyclic Redundancy Check (CRC)

The chip supports an integrated 16-bit Cyclic Redundancy Check function. The Cyclic Redundancy Check (CRC) calculation unit is an error detection technique test algorithm and uses to verify data transmission or storage data correctness. The CRC calculation takes a 8-bit data stream or a block of data as input and generates a 16-bit output remainder. The data stream is calculated by the same generator polynomial.



CRC Block Diagram

The CRC generator provides the 16-bit CRC result calculation based on the CRC-16-IBM polynomial. In this CRC generator, there are only one polynomial available for the numeric values calculation. It can't support the 16-bit CRC calculations based on any other polynomials. Each write operation to the CRCIN register creates a combination of the previous CRC value stored in the CRCDH and CRCDL registers. It will take one MCU instruction cycle to calculate.

CRC-16-IBM (Modbus) Polynomial representation: $X^{16} + X^{15} + X^2 + 1$

SFR **F1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCDL	CRCDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

F1h.7~0 **CRCDL:** 16-bit CRC checksum data bit 7~0

SFR **F2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCDH	CRCDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

F2h.7~0 **CRCDL:** 16-bit CRC checksum data bit 15~8

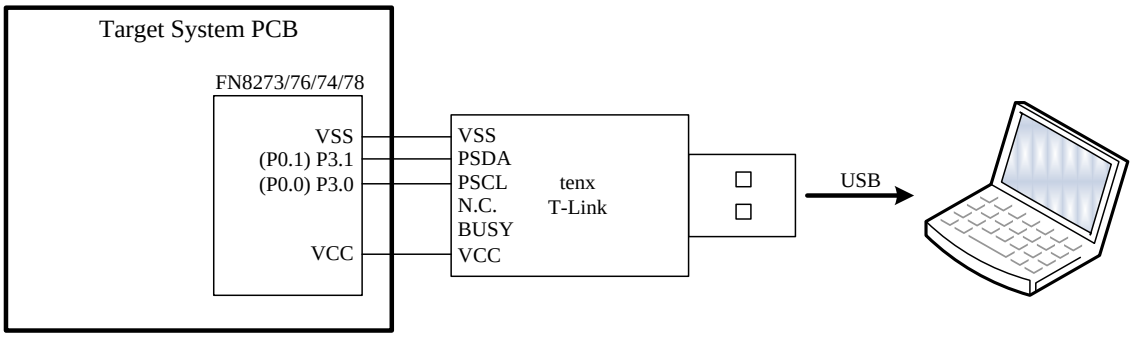
SFR **F3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCIN	CRCIN							
W	W							
Reset	–	–	–	–	–	–	–	–

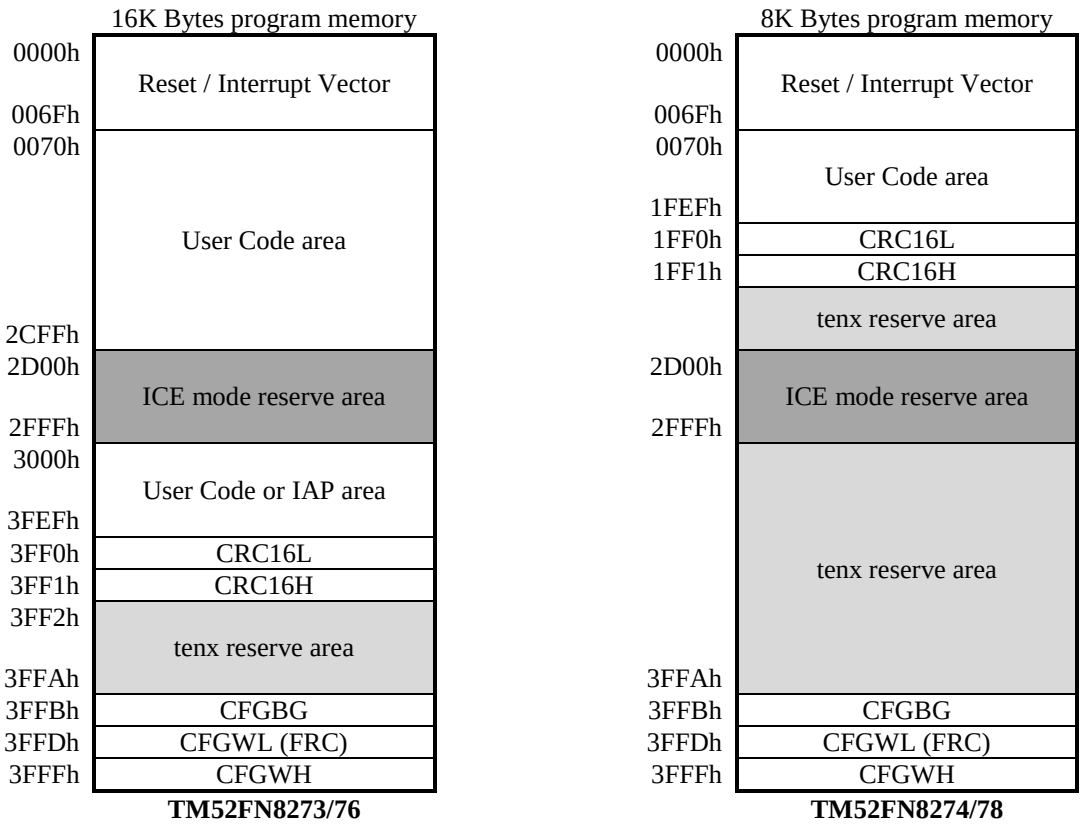
F3h.7~0 **CRCIN:** CRC input data register

17. In Circuit Emulation (ICE) Mode

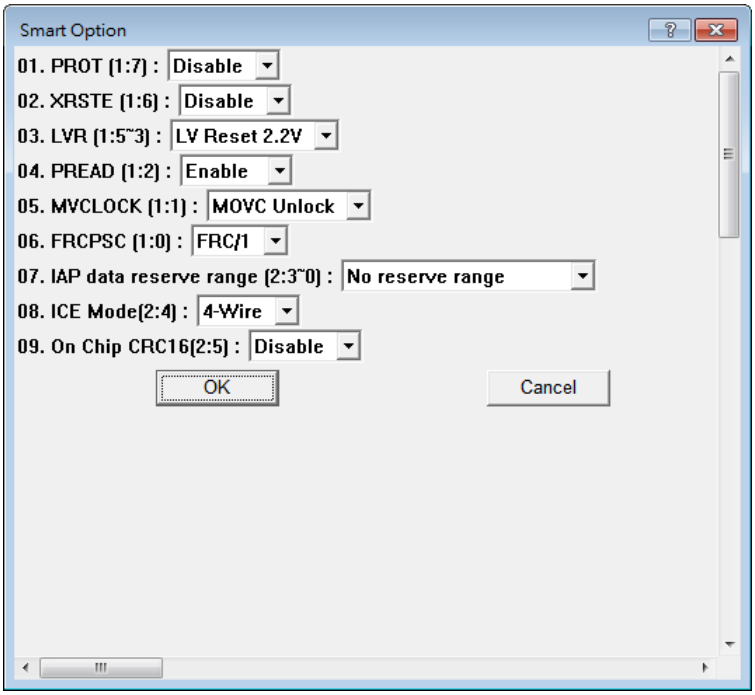
This device can support the In Circuit Emulation Mode. To use the ICE Mode, user just needs to connect P3.0 and P3.1 pin to the tenx proprietary EV Module. The benefit is that user can emulate the whole system without changing the on board target device. But there are some limits for the ICE mode as below.

1. The device must be un-protect.
2. The device's P3.0 and P3.1 pins must work in input Mode (P3MOD0 = 0/1 and P3MOD1=0/1).
3. The Program Memory's addressing space 2D00h~2FFFh and 0033h~003Ah are occupied by tenx EV module. So user Program cannot access these spaces.
4. The T-Link communication pin's function cannot be emulated.
5. The P3.0 and P3.1 pin's can be replaced by P0.0 and P0.1. (only in ICE Mode).
6. The V_{DD} level is controlled by T-Link module.





Introduction to ICE tool option settings：



No.	Item	Description
01	PROT	**Enable:** Flash code is protect, Writer cannot access the ROM code **Disable:** Flash code is not protect, Writer can access the ROM code (default)
02	XRSTE	**Enable:** P3.7 is external reset pin **Disable:** P3.7 is normal I/O pin (default)
03	LVRE	**LV Reset 4.3V:** LVR select 4.3V **LV Reset 4.0V:** LVR select 4.0V **LV Reset 3.7V:** LVR select 3.7V **LV Reset 3.4V:** LVR select 3.4V **LV Reset 3.1V:** LVR select 3.1V **LV Reset 2.8V:** LVR select 2.8V **LV Reset 2.5V:** LVR select 2.5V **LV Reset 2.2V:** LVR select 2.2V (default)
04	PREAD	Reserved
05	MVCLOCK	**MOVC Lock:** the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited. **MOVC Unlock:** the MOVC & MOVX instruction's accessibility to MOVC-Lock area is unlimited. (default)
06	FRCPSC	Reserved
07	IAP data reserve range	**No reserve range:** ROM range is not provided for IAP data (default) **16 bytes [3FE0~3FEF]:** Reserve 16 bytes ROM range for IAP data use **48 bytes [3FC0~3FEF]:** Reserve 48 bytes ROM range for IAP data use **240 bytes [3F00~3FEF]:** Reserve 240 bytes ROM range for IAP data use **496 bytes [3E00~3FEF]:** Reserve 496 bytes ROM range for IAP data use **1008 bytes [3C00~3FEF]:** Reserve 1008 bytes ROM range for IAP data use **2032 bytes [3800~3FEF]:** Reserve 2032 bytes ROM range for IAP data use **4080 bytes [3000~3FEF]:** Reserve 4080 bytes ROM range for IAP data use
08	ICE Mode	Reserved
09	On Chip CRC16	**Enable:** On chip CRC-16 function enable **Disable:** On chip CRC-16 function disable (default)

SFR & CFGW MAP

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h	0000-0000	**P0**	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
81h	0000-0111	**SP**	SP							
82h	0000-0000	**DPL**	DPL							
83h	0000-0000	**DPH**	DPH							
87h	0xxx-0000	**PCON**	SMOD	–	–	–	GF1	GF0	PD	IDL
88h	0000-0000	**TCON**	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89h	0000-0000	**TMOD**	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
8Ah	0000-0000	**TL0**	TL0							
8Bh	0000-0000	**TL1**	TL1							
8Ch	0000-0000	**TH0**	TH0							
8Dh	0000-0000	**TH1**	TH1							
8Eh	0100-0000	**SCON2**	SM	–	–	REN2	TB82	RB82	TI2	RI2
8Fh	xxxx-xxxx	**SBUF2**	SBUF2							
90h	1111-1111	**P1**	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
91h	0000-0000	**P0OE**	P0OE							
92h	0000-0000	**P0LOE**	P0LOE							
93h	xxxx-0101	**P2MOD**	–	–	–	–	P2MOD1		P2MOD0	
94h	0x00-00xx	**OPTION**	UART1W	–	WDTPSC		ADCKS		–	–
95h	xx00-x000	**INTFLG**	–	–	TKIF	ADIF	–	IE2	P1IF	TF3
96h	0000-0000	**P1WKUP**	–	–	–	–	P1WKUP			
97h	xxxx-xx00	**SWCMD**	IAPALL / SWRST / WDTO							
98h	0000-0000	**SCON**	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99h	xxxx-xxxx	**SBUF**	SBUF							
9Ah	1111-1111	**PWM0PRD**	PWM0PRD							
9Bh	1000-0000	**PWM0DH**	PWM0DH							
9Ch	1111-1111	**PWM1PRD**	PWM1PRD							
9Dh	1000-0000	**PWM1DH**	PWM1DH							
9Eh	1111-1111	**PWM2PRD**	PWM2PRD							
9Fh	1000-0000	**PWM2DH**	PWM2DH							
A0h	1111-1111	**P2**	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
A1h	1000-1000	**PWMCON**	PWM1CKS		PWM1DL		PWM0CKS		PWM0DL	
A2h	0101-0101	**P1MODL**	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
A3h	0101-0101	**P1MODH**	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
A4h	0101-0101	**P3MODL**	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
A5h	0101-0101	**P3MODH**	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
A6h	0000-1110	**PINMOD**	PWM1OE	PWM0OE	TCOE	T2OE	HSNK2EN	HSNK1EN	HSNK0EN	T0OE
A7h	xxx0-1000	**PWMCON2**	–	–	–	PWM2OE	PWM2CKS		PWM2DL	
A8h	0x00-0000	**IE**	EA	–	ET2	ES	ET1	EX1	ET0	EX0
A9h	xx00-0000	**INTE1**	–	–	ES2	SPIE	ADTKIE	EX2	P1IE	TM3IE
AAh	xxxx-xxxx	**ADTKDT**	ADCDL				TKDH			
ABh	xxxx-xxxx	**ADCDH**	ADCDH							
ACh	xxxx-xxxx	**TKDL**	TKDL							
ADh	x100-0000	**TKFREQ**	–	TKFREQ						
AEh	1x00-1111	**TKCON**	TKPD	TKEOC	TKIVCS	TKCHS				
AFh	0000-xxxx	**P0ADIE**	P0ADIE				–	–	–	–
B0h	1111-1111	**P3**	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
B1h	0000-0100	**LEDCON**	LEDEN		LEDPSC		LEDHOLD	LEDBRIT		
B2h	0100-x100	**LEDCON2**	LEDSMDIS	LEDBRIT2			–	LEDBRIT1		
B4h	1111-1111	**TKTMRL**	TKTMRL							
B5h	0100-0000	**TKCON2**	TKFJMP	TKFREQS	JMPVAL		TKTMRH			
B6h	xxxx-1111	**ADCHS**	–	–	–	–	ADCHS			
B7h	xxxx-xxxx	**TKDHH**	–	–	TKDHH					
B8h	xx00-0000	**IP**	–	–	PT2	PS	PT1	PX1	PT0	PX0
B9h	xx00-0000	**IPH**	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
BAh	xx00-0000	**IP1**	–	–	PS2	PSPI	PADTKI	PX2	PP1	PT3
BBh	xx00-0000	**IP1H**	–	–	PS2H	PSPIH	PADTKIH	PX2H	PP1H	PT3H
BCh	0000-0000	**SPCON**	SPEN	MSTR	CPOL	CPHA	SSDIS	LSBF	SPCR	
BDh	0000-0xxx	**SPSTA**	SPIF	WCOL	MODF	RCVOVF	RCVBF	SPBSY	–	–

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BEh	0000-0000	**SPDAT**	SPDAT							
C8h	0000-0000	**T2CON**	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
C9h	000x-xxxx	**IAPWE**	IAPWE / IAPTO / EEPWE							
CAh	0000-0000	**RCP2L**	RCP2L							
CBh	0000-0000	**RCP2H**	RCP2H							
CCh	0000-0000	**TL2**	TL2							
CDh	0000-0000	**TH2**	TH2							
D0h	0000-0000	**PSW**	CY	AC	F0	RS1	RS0	OV	F1	P
D1h	0000-0000	**P1LOE**	P1LOE							
D3h	0000-0000	**P3LOE**	P3LOE							
D8h	0010-0011	**CLKCON**	SCKTYPE	FCKTYPE	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
E0h	0000-0000	**ACC**	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
E5h	0000-0000	**EFTCON**	EFT2CS	EFT1CS	EFT1S		EFTSLOW	EFTWCPU	EFTWOUT	CKHLDE
EFh	xx00-0000	**AUX3**	–	–	TM3PSC			VBGEN	ADCVERFS	
F0h	0000-0000	**B**	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
F1h	1111-1111	**CRCDL**	CRCDL							
F2h	1111-1111	**CRCDH**	CRCDH							
F3h	0000-0000	**CRCIN**	CRCIN							
F5h	xxxx-xxxx	**CFGBG**	–	–	–	BGTRIM				
F6h	xxxx-xxxx	**CFGWL**	–	FRCF						
F7h	0000-0110	**AUX2**	WDTE		PWRSAV	VBGOUT	–	IAPTE		LVRPD
F8h	0000-0000	**AUX1**	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL

Flash Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FFBh	**CFGBG**	–	–	–	BGTRIM				
3FFDh	**CFGWL**	–	FRCF						
3FFFh	**CFGWH**	PROT	XRSTE	LVRE			PREAD	MVCLOCK	FRCPSC

SFR & CFGW DESCRIPTION

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
80h	**P0**	7~0	P0	R/W	00h	Port0 data
81h	**SP**	7~0	SP	R/W	07h	Stack Point
82h	**DPL**	7~0	DPL	R/W	00h	Data Point low byte
83h	**DPH**	7~0	DPH	R/W	00h	Data Point high byte
87h	**PCON**	7	SMOD	R/W	0	Set 1 to enable UART1 double baud rate
		3	GF1	R/W	0	General purpose flag bit
		2	GF0	R/W	0	General purpose flag bit
		1	PD	R/W	0	Power down control bit, set 1 to enter Halt/Stop mode
		0	IDL	R/W	0	Idle control bit, set 1 to enter Idle mode
88h	**TCON**	7	TF1	R/W	0	Timer1 overflow flag Set by H/W when Timer/Counter 1 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		6	TR1	R/W	0	Timer1 run control. 1: timer runs; 0: timer stops
		5	TF0	R/W	0	Timer0 overflow flag Set by H/W when Timer/Counter 0 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		4	TR0	R/W	0	Timer0 run control. 1:timer runs; 0:timer stops
		3	IE1	R/W	0	External Interrupt 1 (INT1 pin) edge flag Set by H/W when an INT1 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		2	IT1	R/W	0	External Interrupt 1 control bit 0: Low level active (level triggered) for INT1 pin 1: Falling edge active (edge triggered) for INT1 pin
		1	IE0	R/W	0	External Interrupt 0 (INT0 pin) edge flag Set by H/W when an INT0 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		0	IT0	R/W	0	External Interrupt 0 control bit 0: Low level active (level triggered) for INT0 pin 1: Falling edge active (edge triggered) for INT0 pin
89h	**TMOD**	7	GATE1	R/W	0	Timer1 gating control bit 0: Timer1 enable when TR1 bit is set 1: Timer1 enable only while the INT1 pin is high and TR1 bit is set
		6	CT1N	R/W	0	Timer1 Counter/Timer select bit 0: Timer mode, Timer1 data increases at 2 System clock cycle rate 1: Counter mode, Timer1 data increases at T1 pin's negative edge
		5~4	TMOD1	R/W	00	Timer1 mode select 00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 11: Timer1 stops
		3	GATE0	R/W	0	Timer0 gating control bit 0: Timer0 enable when TR0 bit is set 1: Timer0 enable only while the INT0 pin is high and TR0 bit is set
		2	CT0N	R/W	0	Timer0 Counter/Timer select bit 0: Timer mode, Timer0 data increases at 2 System clock cycle rate 1: Counter mode, Timer0 data increases at T0 pin's negative edge
		1~0	TMOD0	R/W	00	Timer0 mode select 00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.
8Ah	**TL0**	7~0	TL0	R/W	00h	Timer0 data low byte
8Bh	**TL1**	7~0	TL1	R/W	00h	Timer1 data low byte
8Ch	**TH0**	7~0	TH0	R/W	00h	Timer0 data high byte
8Dh	**TH1**	7~0	TH1	R/W	00h	Timer1 data high byte

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
8Eh	**SCON2**	7	SM	R/W	0	UART2 Serial port mode select bit 0: Mode1: 8 bit UART2, Baud Rate is variable 1: Mode3: 9 bit UART2, Baud Rate is variable
		4	REN2	R/W	0	UART2 reception enable 0: Disable reception 1: Enable reception
		3	TB82	R/W	0	Transmit Bit 8, the ninth bit to be transmitted in Mode3
		2	RB82	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode3
		1	TI2	R/W	0	Transmit interrupt flag Set by H/W at the beginning of the stop bit in Mode 1 & 3. Must be cleared by S/W.
		0	RI2	R/W	0	Receive interrupt flag Set by H/W at the sampling point of the stop bit in Mode 1 & 3. Must be cleared by S/W.
8Fh	**SBUF2**	7~0	SBUF2	R/W	–	UART2 transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
90h	**P1**	7~0	P1	R/W	FFh	Port1 data
91h	**P0OE**	7~0	P0OE	R/W	00h	Port0 CMOS Push-Pull output enable control 0: Disable 1: Enable
92h	**P0LOE**	7~0	P0LOE	R/W	00h	Port0 LCD 1/2 bias output enable control 0: Disable 1: Enable
93h	**P2MOD**	3~2	P2MOD1	R/W	01	P2.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: not defined
		1~0	P2MOD0	R/W	01	P2.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: not defined
94h	**OPTION**	7	UART1W	R/W	0	Set 1 to enable one wire UART1 mode, both TXD/RXD use P3.1 pin.
		5~4	WDTPSC	R/W	00	Watchdog Timer pre-scalar time select 00: 400ms WDT overflow rate 01: 200ms WDT overflow rate 10: 100ms WDT overflow rate 11: 50ms WDT overflow rate
		3~2	ADCKS	R/W	00	ADC clock rate select 00: F_{SYSCLK}/32 01: F_{SYSCLK}/16 10: F_{SYSCLK}/8 11: F_{SYSCLK}/4
95h	**INTFLG**	5	TKIF	R/W	0	Touch Key Interrupt Flag Set by H/W at the end of TK conversion if SYSCLK is fast enough. S/W writes DFh to INTFLG or sets the TKSOC bit to clear this flag.
		4	ADIF	R/W	0	ADC interrupt flag Set by H/W at the end of ADC conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.
		2	IE2	R/W	0	External Interrupt 2 (INT2 pin) edge flag Set by H/W when a falling edge is detected on the INT2 pin, no matter the EX2 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine. S/W can write FBh to INTFLG to clear this bit.
		1	P1IF	R/W	0	P1.0~P1.3 pin change Interrupt flag Set by H/W when a P1.0~P1.3 pin state change is detected and its interrupt enable bit is set (P1WKUP). P1IE does not affect this flag's setting. It is cleared automatically when the program performs the interrupt service routine. S/W can write FDh to INTFLG to clear this bit.
		0	TF3	R/W	0	Timer3 Interrupt Flag Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
96h	**P1WKUP**	7~4	-	R/W	0000	Reserved, Keep 0
		3~0	P1WKUP	R/W	0000	P1.3~P1.0 pin individual Wake-up/Interrupt enable control 0: Disable; 1: Enable.
97h	**SWCMD**	7~0	SWRST	W		Write 56h to generate S/W Reset
		7~0	IAPALL	W		Write 65h to set IAPALL control flag; Write other value to clear IAPALL flag. It is recommended to clear it immediately after IAP access.
		1	WDTO	R	0	WatchDog Time-Out flag
		0	IAPALL	R	0	Flag indicates Flash memory sectors can be accessed by IAP or not. This bit combines with MVCLOCK to define the accessible IAP area.
98h	**SCON**	7	SM0	R/W	0	UART1 Serial port mode select bit 0, 1 (SM0, SM1) = 00: Mode0: 8 bit shift register, Baud Rate=F_{SYSCLK}/2 01: Mode1: 8 bit UART1, Baud Rate is variable 10: Mode2: 9 bit UART1, Baud Rate=F_{SYSCLK}/32 or /64 11: Mode3: 9 bit UART1, Baud Rate is variable
		6	SM1	R/W	0	
		5	SM2	R/W	0	Serial port mode select bit 2 SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.
		4	REN	R/W	0	Set 1 to enable UART1 Reception
		3	TB8	R/W	0	Transmitter bit 8, ninth bit to transmit in Modes 2 and 3
		2	RB8	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit is Mode 1 if SM2=0
		1	TI	R/W	0	Transmit Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W
		0	RI	R/W	0	Receive Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.
99h	**SBUF**	7~0	SBUF	R/W	–	UART1 transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
9Ah	**PWM0PRD**	7~0	PWM0PRD	R/W	FFh	PWM0 8-bit period register
9Bh	**PWM0DH**	7~0	PWM0DH	R/W	80h	bits 9~2 of the PWM0 10-bit duty register
9Ch	**PWM1PRD**	7~0	PWM1PRD	R/W	FFh	PWM1 8-bit period register
9Dh	**PWM1DH**	7~0	PWM1DH	R/W	80h	bits 9~2 of the PWM1 10-bit duty register
9Eh	**PWM2PRD**	7~0	PWM2PRD	R/W	FFh	PWM2 8-bit period register
9Fh	**PWM2DH**	7~0	PWM2DH	R/W	80h	bits 9~2 of the PWM2 10-bit duty register
A0h	**P2**	7~2	P2.7~P2.2	R/W	3Fh	P2.7~P2.2 have no pin out, so these bits are used as general purpose register
		1~0	P2.1~P2.0	R/W	11	P2.1~P2.0 data
A1h	**PWMCON**	7~6	PWM1CKS	R/W	10	PWM1 clock source 00: F_{SYSCLK}/4 01: F_{SYSCLK}/2 10: F_{SYSCLK} 11: FRC
		5~4	PWM1DL	R/W	00	bits 1~0 of the PWM1 10-bit duty register
		3~2	PWM0CKS	R/W	10	PWM0 clock source 00: F_{SYSCLK}/4 01: F_{SYSCLK}/2 10: F_{SYSCLK} 11: FRC
		1~0	PWM0DL	R/W	00	bits 1~0 of the PWM0 10-bit duty register
A2h	**P1MODL**	7~6	P1MOD3	R/W	01	P1.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.3 is ADC input
		5~4	P1MOD2	R/W	01	P1.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.2 is ADC input

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		3~2	P1MOD1	R/W	01	P1.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.1 is ADC input
		1~0	P1MOD0	R/W	01	P1.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.0 is ADC input
A3h	**P1MODH**	7~6	P1MOD7	R/W	01	P1.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3
		5~4	P1MOD6	R/W	01	P1.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3
		3~2	P1MOD5	R/W	01	P1.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.5 is ADC input
		1~0	P1MOD4	R/W	01	P1.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.4 is ADC input
A4h	**P3MODL**	7~6	P3MOD3	R/W	01	P3.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.3 is ADC input
		5~4	P3MOD2	R/W	01	P3.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.2 is ADC input
		3~2	P3MOD1	R/W	01	P3.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.1 is ADC input
		1~0	P3MOD0	R/W	01	P3.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.0 is ADC input
A5h	**P3MODH**	7~6	P3MOD7	R/W	01	P3.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3
		5~4	P3MOD6	R/W	01	P3.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3
		3~2	P3MOD5	R/W	01	P3.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3
		1~0	P3MOD4	R/W	01	P3.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3
A6h	**PINMOD**	7	PWM1OE	R/W	0	PWM1 control 0: PWM1 disable 1: PWM1 enable and signal output to P1.3 pin
		6	PWM0OE	R/W	0	PWM0 control 0: PWM0 disable 1: PWM0 enable and signal output to P1.2 pin
		5	TCOE	R/W	0	Set 1 to enable "System clock divided by 2" (CKO) output to P1.4 pin
		4	T2OE	R/W	0	Set 1 to enable "Timer2 overflow divided by 2" (T2O) output to P1.0 pin
		3	HSNK2EN	R/W	1	Pin H-sink enable (Group 2: P06, P07, P22~P25, P30~P33) 0: Group 2 High-sink disable 1: Group 2 High-sink enable
		2	HSNK1EN	R/W	1	Pin H-sink enable (Group 1: P04, P05, P10~P17) 0: Group 1 High-sink disable 1: Group 2 High-sink enable
		1	HSNK0EN	R/W	1	Pin H-sink enable (Group 0: P00~P03, P20, P21, P34~P37) 0: Group 0 High-sink disable 1: Group 2 High-sink enable
		0	T0OE	R/W	0	Set 1 to enable "Timer0 overflow divided by 64" (T0O) output to P3.4 pin

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
A7h	**PWMCON2**	4	PWM2OE	R/W	0	PWM2 control 0: PWM2 disable 1: PWM2 enable and signal output to P1.6 pin
		3~2	PWM2CKS	R/W	10	PWM2 clock source 00: $F_{SYSCLK}/4$ 01: $F_{SYSCLK}/2$ 10: F_{SYSCLK} 11: FRC
		1~0	PWM2DL	R/W	00	bits 1~0 of the PWM2 10-bit duty register
A8h	**IE**	7	EA	R/W	0	Global interrupt enable control. 0: Disable all Interrupts. 1: Each interrupt is enabled or disabled by its own interrupt control bit.
		5	ET2	R/W	0	Set 1 to enable Timer2 interrupt
		4	ES	R/W	0	Set 1 to enable Serial Port (UART1) Interrupt
		3	ET1	R/W	0	Set 1 to enable Timer1 Interrupt
		2	EX1	R/W	0	Set 1 to enable external INT1 pin Interrupt & Halt/Stop mode wake up capability
		1	ET0	R/W	0	Set 1 to enable Timer0 Interrupt
		0	EX0	R/W	0	Set 1 to enable external INT0 pin Interrupt & Halt/Stop mode wake up capability
A9h	**INTE1**	5	ES2	R/W	0	Set 1 to enable Serial Port (UART2) interrupt
		4	SPIE	R/W	0	Set 1 to enable SPI interrupt
		3	ADTKIE	R/W	0	Set 1 to enable ADC/Touch Key Interrupt
		2	EX2	R/W	0	Set 1 to enable external INT2 pin Interrupt & Halt/Stop mode wake up capability
		1	P1IE	R/W	0	Set 1 to enable P1.0~P1.3 Pin Change Interrupt
		0	TM3IE	R/W	0	Set 1 to enable Timer3 Interrupt
AAh	**ADTKDT**	7~4	ADCDL	R	–	ADC data bit 3~0
		3~0	TKDH	R	–	Touch Key counter data bit 11~8
ABh	**ADCDH**	7~0	ADCDH	R	–	ADC data bit 11~4
ACh	**TKDL**	7~0	TKDL	R	–	Touch Key counter data bit 7~0
ADh	**TKFREQ**	6~0	TKFREQ	R/W	40h	Touch Key oscillation capacitor adjustment 00: TKDATA is smallest … 7F: TKDATA is biggest
AEh	**TKCON**	7	TKPD	R/W	1	Touch Key Power Down 0: Touch Key enable 1: Touch Key disable
		6	TKEOC	R	1	Touch Key end of conversion flag 0: Indicates conversion is in progress 1: Indicates conversion is finished
		5	TKIVCS	R/W	0	Touch Key internal LDO voltage control 0: 1.4V 1: 1.8V
		4~0	TKCHS	R/W	01111	Touch Key channel select 00000: TK0 (P3.3) 01010: TK10 (P0.4) 00001: TK1 (P3.2) 01011: TK11 (P0.5) 00010: TK2 (P3.1) 01100: TK12 (P0.6) 00011: TK3 (P3.0) 01101: TK13 (P3.4) 00100: TK4 (P1.0) 01110: TK14 (P1.5) 00101: TK5 (P1.1) 01111: internal reference key 00110: TK6 (P1.2) 10000: TK16 (P1.7) 00111: TK7 (P1.3) 10001: TK17 (P3.6) 01000: TK8 (P1.4) 10010: TK18 (P3.5) 01001: TK9 (P1.6) 10011: TK19 (P3.7)

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
AFh	**P0ADIE**	7~4	P0ADIE	R/W	0000	ADC channel input Enable 0000: P0.7~P0.4 are digital input 1xxx: P0.7 is ADC input x1xx: P0.6 is ADC input xx1x: P0.5 is ADC input xxx1: P0.4 is ADC input
B0h	**P3**	7~0	P3	R/W	FFh	Port3 data
B1h	**LEDCON**	7~6	LEDEN	R/W	00	LED enable and duty select 00: LED disable 01: LED 1/8 duty (4COM x 4SEG) 10: Reserved 11: LED 1/10 duty (4COM x 6SEG)
		5~4	LEDPSC	R/W	00	LED clock prescaler select 00: LED clock is FRC divided by 64 01: LED clock is FRC divided by 32 10: LED clock is FRC divided by 16 11: LED clock is FRC divided by 8
		3	LEDHOLD	R/W	0	LED hold function 0:Release to run LED scanning 1: Hold LED scanning, all LED pins state are Hi-Z
		2~0	LEDBRIT	R/W	100	LED COM0+ ~ COM3+ & SEG0+ ~ SEG3+ (LED number 0~31, 40~47) brightness select 000: Level 0 (Darkest) … 111: Level 7 (Brightest)
B2h	**LENCON2**	7	LEDSMDIS	R/W	0	LED brightness smooth control 0: Brightness smooth enable 1: Brightness smooth disable
		6~4	LEDBRIT2	R/W	100	LED SEG5+ (LED number 33, 35, 37, 39) brightness select 000: Level 0 (Darkest) … 111: Level 7 (Brightest)
		2~0	LEDBRIT1	R/W	100	LED SEG4+ (LED number 32, 34, 36, 38) brightness select 000: Level 0 (Darkest) … 111: Level 7 (Brightest)
B4h	**TKTMRL**	7~0	TKTMRL	R/W	FFh	Touch Key reference counter bit 7~0
B5h	**TKCON2**	7	TKFJMP	R/W	0	Touch Key clock frequency auto-change selection 0: fix frequency 1: auto-change
		6	TKFREQS	R/W	0	Touch Key reference clock frequency select slow or fast
		5~4	JMPVAL	R/W	00	Touch Key clock frequency fine tune **(only available in TKFJMP=0)** 00: frequency slowest 11: frequency fastest
		3~0	TKTMRH	R/W	0	Touch Key reference counter bit 11~8
B6h	**ADCHS**	3~0	ADCHS	R/W	1111	ADC channel select 0000: AD0 (P3.3) 0001: AD1 (P3.2) 0010: AD2 (P3.1) 0011: AD3 (P3.0) 0100: AD4 (P1.0) 0101: AD5 (P1.1) 0110: AD6 (P1.2) 0111: AD7 (P1.3) 1000: AD8 (P1.4) 1001: AD9 (P1.5) 1010: AD10 (P0.7) 1011: V_{BG} (Internal Bandgap Reference Voltage) 1100: AD12 (P0.4) 1101: AD13 (P0.5) 1110: AD14 (P0.6) 1111: V_{CC}/4

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
B7h	**TKDHH**	5~0	TKDHH	R	–	Touch Key counter data bit 13~8
B8h	**IP**	5	PT2	R/W	0	Timer2 Interrupt Priority Low bit
		4	PS	R/W	0	Serial Port (UART1) Interrupt Priority Low bit
		3	PT1	R/W	0	Timer1 Interrupt Priority Low bit
		2	PX1	R/W	0	External INT1 Pin Interrupt Priority Low bit
		1	PT0	R/W	0	Timer0 Interrupt Priority Low bit
		0	PX0	R/W	0	External INT0 Pin Interrupt Priority Low bit
B9h	**IPH**	5	PT2H	R/W	0	Timer2 Interrupt Priority High bit
		4	PSH	R/W	0	Serial Port (UART1) Interrupt Priority High bit
		3	PT1H	R/W	0	Timer1 Interrupt Priority High bit
		2	PX1H	R/W	0	External INT1 Pin Interrupt Priority High bit
		1	PT0H	R/W	0	Timer0 Interrupt Priority High bit
		0	PX0H	R/W	0	External INT0 Pin Interrupt Priority High bit
BAh	**IP1**	5	PS2	R/W	0	Serial Port (UART2) interrupt priority low bit
		4	PSPI	R/W	0	SPI interrupt priority low bit
		3	PADTKI	R/W	0	ADC/Touch Key Interrupt Priority Low bit
		2	PX2	R/W	0	External INT2 Pin Interrupt Priority Low bit
		1	PP1	R/W	0	P1.0~P1.3 pin change Interrupt Priority Low bit
		0	PT3	R/W	0	Timer3 Interrupt Priority Low bit
BBh	**IP1H**	5	PS2H	R/W	0	Serial Port (UART2) interrupt priority high bit
		4	PSPIH	R/W	0	SPI interrupt priority high bit
		3	PADTKIH	R/W	0	ADC/Touch Key Interrupt Priority High bit
		2	PX2H	R/W	0	External INT2 Pin Interrupt Priority High bit
		1	PP1H	R/W	0	P1.0~P1.3 Interrupt Priority High bit
		0	PT3H	R/W	0	Timer3 Interrupt Priority High bit
BCh	**SPCON**	7	SPEN	R/W	0	SPI enable 0: SPI disable 1: SPI enable
		6	MSTR	R/W	0	Master mode enable 0: Slave mode 1: Master mode
		5	CPOL	R/W	0	SPI clock polarity 0: SCK is low in idle state 1: SCK is high in idle state
		4	CPHA	R/W	0	SPI clock phase 0: Data sample on first edge of SCK period 1: Data sample on second edge of SCK period
		3	SSDIS	R/W	0	SS pin disable 0: Enable SS pin 1: Disable SS pin
		2	LSBF	R/W	0	LSB first 0: MSB first 1: LSB first
		1~0	SPCR	R/W	00	SPI clock rate 00: $F_{SYSCLK}/2$ 01: $F_{SYSCLK}/4$ 10: $F_{SYSCLK}/8$ 11: $F_{SYSCLK}/16$
BDh	**SPSTA**	7	SPIF	R/W	0	SPI interrupt flag This is set by H/W at the end of a data transfer. Cleared by H/W when an interrupt is vectored into. Writing 0 to this bit will clear this flag.
		6	WCOL	R/W	0	Write collision interrupt flag Set by H/W if write data to SPDAT when SPBSY is set. Write 0 to this bit or rewrite data to SPDAT when SPBSY is cleared will clear this flag.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		5	MODF	R/W	0	Mode fault interrupt flag Set by H/W when SSDIS is cleared and SS pin is pulled low in Master mode. Write 0 to this bit will clear this flag. When this bit is set, the SPEN and MSTR in SPCON will be cleared by H/W.
		4	RCVOVF	R/W	0	Received buffer overrun flag Set by H/W at the end of a data transfer and RCVBF is set. Write 0 to this bit or read SPDAT register will clear this flag.
		3	RCVBF	R/W	0	Receive buffer full flag Set by H/W at the end of a data transfer. Write 0 to this bit or read SPDAT register will clear this flag.
		2	SPBSY	R	0	SPI busy flag Set by H/W when a SPI transfer is in progress.
BEh	**SPDAT**	7~0	SPDAT	R/W	0	SPI transmit and receive data The SPDAT register is used to transmit and receive data. Writing data to SPDAT place the data into shift register and start a transfer when in master mode. Reading SPDAT returns the contents of the receive buffer.
C8h	**T2CON**	7	TF2	R/W	0	Timer2 overflow flag Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.
		6	EXF2	R/W	0	T2EX interrupt pin falling edge flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.
		5	RCLK	R/W	0	UART receive clock control bit 0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3 1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3
		4	TCLK	R/W	0	UART transmit clock control bit 0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3 1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3
		3	EXEN2	R/W	0	T2EX pin enable 0: T2EX pin disable 1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0
		2	TR2	R/W	0	Timer2 run control 0:timer stops 1:timer runs
		1	CT2N	R/W	0	Timer2 Counter/Timer select bit 0: Timer mode, Timer2 data increases at 2 System clock cycle rate 1: Counter mode, Timer2 data increases at T2 pin's negative edge
		0	CPRL2N	R/W	0	Timer2 Capture/Reload control bit 0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1. 1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1. If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.
C9h	**IAPWE**	7~0	IAPWE	W	–	Write 47h to set IAPWE control flag; Write other value to clear IAPWE and EEPWE flag. It is recommended to clear it immediately after IAP write.
		7~0	EEPWE	W	–	Write E2h to set EEPWE control flag; Write other value to clear IAPWE and EEPWE flag. It is recommended to clear it immediately after EEPROM write.
		7	IAPWE	R	0	Flag indicates Flash memory can be written by IAP or not 0: IAP Write disable 1: IAP Write enable
		6	IAPTO	R	0	IAP (or EEPROM write) Time-Out flag Set by H/W when IAP (or EEPROM write) Time-out occurs. Cleared by H/W when IAPWE=0 (or EEPWE=0).
		5	EEPWE	R	0	Flag indicates EEPROM memory can be written or not 0: EEPROM Write disable 1: EEPROM Write enable

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
CAh	**RCP2L**	7~0	RCP2L	R/W	00h	Timer2 reload/capture data low byte
CBh	**RCP2H**	7~0	RCP2H	R/W	00h	Timer2 reload/capture data high byte
CCh	**TL2**	7~0	TL2	R/W	00h	Timer2 data low byte
CDh	**TH2**	7~0	TH2	R/W	00h	Timer2 data high byte
D0h	**PSW**	7	CY	R/W	0	ALU carry flag
		6	AC	R/W	0	ALU auxiliary carry flag
		5	F0	R/W	0	General purpose user-definable flag
		4	RS1	R/W	0	Register Bank Select bit 1
		3	RS0	R/W	0	Register Bank Select bit 0
		2	OV	R/W	0	ALU overflow flag
		1	F1	R/W	0	General purpose user-definable flag
		0	P	R/W	0	Parity flag
D1h	**P1LOE**	7~0	P1LOE	R/W	00h	Port1 LCD 1/2 bias output enable control 0: Disable 1: Enable
D3h	**P3LOE**	7~0	P3LOE	R/W	00h	Port3 LCD 1/2 bias output enable control 0: Disable 1: Enable
D8h	**CLKCON**	7	SCKTYPE	R/W	0	Slow clock Type. This bit can be changed only in Fast mode (SELFCK=1) 0: SRC 1: SXT, P2.0 and P2.1 are crystal pins
		6	FCKTYPE	R/W	0	Fast clock type. This bit can be changed only in Slow mode (SELFCK=0). 0: FRC 1: FXT, P2.0 and P2.1 are crystal pins, oscillator gain is high for FXT
		5	STPSCK	R/W	1	Set 1 to stop Slow clock in Stop mode.
		4	STPPCK	R/W	0	Set 1 to stop UART/Timer0/1/2 clock in Idle mode for current reducing.
		3	STPFCK	R/W	0	Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.
		2	SELFCK	R/W	0	System clock select. This bit can be changed only when STPFCK=0. 0: Slow clock 1: Fast clock
		1~0	CLKPSC	R/W	11	System clock prescaler. Effective after 16 clock cycles (Max.) delay. 00: System clock is Fast/Slow clock divided by 16 01: System clock is Fast/Slow clock divided by 4 10: System clock is Fast/Slow clock divided by 2 11: System clock is Fast/Slow clock divided by 1
E0h	**ACC**	7~0	ACC	R/W	00h	Accumulator
E5h	**EFTCON**	7	EFT2CS	R/W	0	EFT2 Detector enable 0: Disable EFT2 1: Enable EFT2
		6	EFT1CS	R/W	0	EFT1 Detector enable 0: Disable EFT1 1: Enable EFT1
		5~4	EFT1S	R/W	00	EFT1 Detector sensitivity adjustment
		3	EFTSLOW	R/W	0	Force F_{SYSCLK} to Slow clock while EFT detected 0: Disable 1: Enable
		2	EFTWCPU	R/W	0	CPU enter wait state while EFT detected 0: Disable 1: Enable
		1	EFTWOUT	R/W	0	EFTWAIT output to pin 0: P0.7 = normal I/O 1: P0.7 = EFTWAIT

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		0	CKHLDE	R/W	0	Clock Hold enable 0: Disable 1: Enable
EFh	**AUX3**	5~3	TM3PSC	R/W	000	Timer3 Interrupt rate 000: Timer3 Interrupt rate is 32768 Slow clock cycle 001: Timer3 Interrupt rate is 16384 Slow clock cycle 010: Timer3 Interrupt rate is 8192 Slow clock cycle 011: Timer3 Interrupt rate is 4096 Slow clock cycle 100: Timer3 Interrupt rate is 2048 Slow clock cycle 101: Timer3 Interrupt rate is 1024 Slow clock cycle 110: Timer3 Interrupt rate is 512 Slow clock cycle 111: Timer3 Interrupt rate is 256 Slow clock cycle
		2	VBGEN	R/W	0	Bandgap voltage enable control 0: V_{BG}/VBGO disable at Idle/Halt/Stop mode 1: Force V_{BG}/VBGO to be enabled, included in Idle mode, but disabled in Halt/Stop mode
		1	–	–	0	Reserved, Keep 0
		0	ADCVREFS	R/W	0	ADC reference voltage (V_{REF}) select 0: V_{CC} 1: 2.5V
F0h	**B**	7~0	B	R/W	00h	B register
F1h	**CRCDL**	7~0	CRCDL	R/W	FFh	16-bit CRC data bit 7~0
F2h	**CRCDH**	7~0	CRCDH	R/W	FFh	16-bit CRC data bit 15~8
F3h	**CRCIN**	7~0	CRCIN	W	–	CRC input data
F5h	**CFGBG**	4~0	BGTRIM	R/W	–	Bandgap voltage trimming value
F6h	**CFGWL**	6~0	FRCF	R/W	–	FRC frequency adjustment 00h: lowest frequency … 7Fh: highest frequency
F7h	**AUX2**	7~6	WDTE	R/W	–	Watchdog Timer Reset control 0x: WDT disable 10: WDT enable in Fast/Slow mode, disable in Idle/Halt/Stop mode 11: WDT always enable
		5	PWRSAV	R/W	–	Set 1 to reduce the chip's power consumption at Idle/Halt/Stop mode.
		4	VBGOUT	R/W	0	Bandgap voltage output control 0: P3.2 as normal I/O 1: Bandgap voltage output to P3.2 pin, when ADCHS = 1011b
		3	–	–	0	Reserved, Keep 0
		2~1	IAPTE	R/W	11	IAP (or EEPROM write) watchdog timer enable 00: Disable 01: wait 1.5ms trigger watchdog time-out flag 10: wait 5.8ms trigger watchdog time-out flag 11: wait 11.7ms trigger watchdog time-out flag
		0	LVRPD	R/W	0	LVR power down 0: LVR enable 1: LVR disable
F8h	**AUX1**	7	CLRWDT	R/W	0	Set 1 to clear WDT, H/W auto clear it at next clock cycle
		6	CLRTM3	R/W	0	Set 1 to clear Timer3, HW auto clear it at next clock cycle.
		5	TKSOC	R/W	0	Touch Key Start of Conversion Set 1 to start Touch Key conversion. If SYSCLK is fast enough, this bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
		4	ADSOC	R/W	0	ADC Start of Conversion Set 1 to start ADC conversion. Cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
		3	CLRPWM0	R/W	0	PWM0 clear enable 0: PWM0 is running 1: PWM0 is cleared and held

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		2	T2SEL	R/W	0	Timer2 Counter mode, T2 pin input select 0: P1.0 (T2) 1: Slow clock/16
		1	T1SEL	R/W	0	Timer1 Counter mode, T1 pin input select 0: P3.5 (T1) 1: Slow clock/16
		0	DPSEL	R/W	0	Active DPTR Select

Adr	Flash	Bit#	Bit Name	Description
3FFBh	**CFGBG**	4~0	BGTRIM	Bandgap voltage adjustment. V_{BG} is trimmed to 1.20V in chip manufacturing. BGTRIM records the adjustment data.
3FFDh	**CFGWL**	6~0	FRCF	FRC frequency adjustment. FRC is trimmed to 14.7456 MHz in chip manufacturing. FRCF records the adjustment data.
3FFFh	**CFGWH**	7	PROT	Flash Code Protect, 1=Protect
		6	XRSTE	External Pin Reset enable, 1=enable.
		5~3	LVRE	Low Voltage Reset function select 000: Set LVR at 2.2V 001: Set LVR at 2.5V 010: Set LVR at 2.8V 011: Set LVR at 3.1V 100: Set LVR at 3.4V 101: Set LVR at 3.7V 110: Set LVR at 4.0V 111: Set LVR at 4.3V
		2	PREAD	Reserved
		1	MVCLOCK	If 1, the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited.
		0	FRCPSC	Reserved

INSTRUCTION SET

Instructions are 1, 2 or 3 bytes long as listed in the 'byte' column below. Each instruction takes 1~8 System clock cycles to execute as listed in the 'cycle' column below.

ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ADD A,Rn	Add register to A	1	2	28-2F
ADD A,dir	Add direct byte to A	2	2	25
ADD A,@Ri	Add indirect memory to A	1	2	26-27
ADD A,#data	Add immediate to A	2	2	24
ADDC A,Rn	Add register to A with carry	1	2	38-3F
ADDC A,dir	Add direct byte to A with carry	2	2	35
ADDC A,@Ri	Add indirect memory to A with carry	1	2	36-37
ADDC A,#data	Add immediate to A with carry	2	2	34
SUBB A,Rn	Subtract register from A with borrow	1	2	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	2	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	2	04
INC Rn	Increment register	1	2	08-0F
INC dir	Increment direct byte	2	2	05
INC @Ri	Increment indirect memory	1	2	06-07
DEC A	Decrement A	1	2	14
DEC Rn	Decrement register	1	2	18-1F
DEC dir	Decrement direct byte	2	2	15
DEC @Ri	Decrement indirect memory	1	2	16-17
INC DPTR	Increment data pointer	1	4	A3
MUL AB	Multiply A by B	1	8	A4
DIV AB	Divide A by B	1	8	84
DA A	Decimal Adjust A	1	2	D4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ANL A,Rn	AND register to A	1	2	58-5F
ANL A,dir	AND direct byte to A	2	2	55
ANL A,@Ri	AND indirect memory to A	1	2	56-57
ANL A,#data	AND immediate to A	2	2	54
ANL dir,A	AND A to direct byte	2	2	52
ANL dir,#data	AND immediate to direct byte	3	4	53
ORL A,Rn	OR register to A	1	2	48-4F
ORL A,dir	OR direct byte to A	2	2	45
ORL A,@Ri	OR indirect memory to A	1	2	46-47
ORL A,#data	OR immediate to A	2	2	44
ORL dir,A	OR A to direct byte	2	2	42
ORL dir,#data	OR immediate to direct byte	3	4	43
XRL A,Rn	Exclusive-OR register to A	1	2	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	2	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	2	66-67
XRL A,#data	Exclusive-OR immediate to A	2	2	64
XRL dir,A	Exclusive-OR A to direct byte	2	2	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	4	63
CLR A	Clear A	1	2	E4
CPL A	Complement A	1	2	F4
SWAP A	Swap Nibbles of A	1	2	C4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
RL A	Rotate A left	1	2	23
RLC A	Rotate A left through carry	1	2	33
RR A	Rotate A right	1	2	03
RRC A	Rotate A right through carry	1	2	13

DATA TRANSFER				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MOV A,Rn	Move register to A	1	2	E8-EF
MOV A,dir	Move direct byte to A	2	2	E5
MOV A,@Ri	Move indirect memory to A	1	2	E6-E7
MOV A,#data	Move immediate to A	2	2	74
MOV Rn,A	Move A to register	1	2	F8-FF
MOV Rn,dir	Move direct byte to register	2	4	A8-AF
MOV Rn,#data	Move immediate to register	2	2	78-7F
MOV dir,A	Move A to direct byte	2	2	F5
MOV dir,Rn	Move register to direct byte	2	4	88-8F
MOV dir,dir	Move direct byte to direct byte	3	4	85
MOV dir,@Ri	Move indirect memory to direct byte	2	4	86-87
MOV dir,#data	Move immediate to direct byte	3	4	75
MOV @Ri,A	Move A to indirect memory	1	2	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	4	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	2	76-77
MOV DPTR,#data	Move immediate to data pointer	3	4	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	8	93
MOVC A,@A+PC	Move code byte relative PC to A	1	8	83
MOVX A,@Ri	Move external data(A8) to A	1	8	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	8	E0
MOVX @Ri,A	Move A to external data(A8)	1	8	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	8	F0
PUSH dir	Push direct byte onto stack	2	4	C0
POP dir	Pop direct byte from stack	2	4	D0
XCH A,Rn	Exchange A and register	1	2	C8-CF
XCH A,dir	Exchange A and direct byte	2	2	C5
XCH A,@Ri	Exchange A and indirect memory	1	2	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2	D6-D7

BOOLEAN				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
CLR C	Clear carry	1	2	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	2	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	2	B3
CPL bit	Complement direct bit	2	2	B2
ANL C,bit	AND direct bit to carry	2	4	82
ANL C,/bit	AND direct bit inverse to carry	2	4	B0
ORL C,bit	OR direct bit to carry	2	4	72
ORL C,/bit	OR direct bit inverse to carry	2	4	A0
MOV C,bit	Move direct bit to carry	2	2	A2
MOV bit,C	Move carry to direct bit	2	4	92

BRANCHING				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ACALL addr 11	Absolute jump to subroutine	2	6	11-F1
LCALL addr 16	Long jump to subroutine	3	6	12
RET	Return from subroutine	1	6	22
RETI	Return from interrupt	1	6	32
AJMP addr 11	Absolute jump unconditional	2	6	01-E1
LJMP addr 16	Long jump unconditional	3	6	02
SJMP rel	Short jump (relative address)	2	6	80
JC rel	Jump on carry = 1	2	4 (or 6)	40
JNC rel	Jump on carry = 0	2	4 (or 6)	50
JB bit,rel	Jump on direct bit = 1	3	4 (or 6)	20
JNB bit,rel	Jump on direct bit = 0	3	4 (or 6)	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	4 (or 6)	10
JMP @A+DPTR	Jump indirect relative DPTR	1	6	73
JZ rel	Jump on accumulator = 0	2	4 (or 6)	60
JNZ rel	Jump on accumulator ≠ 0	2	4 (or 6)	70
CJNE A,dir,rel	Compare A,direct, jump not equal relative	3	4 (or 6)	B5
CJNE A,#data,rel	Compare A,immediate, jump not equal relative	3	4 (or 6)	B4
CJNE Rn,#data,rel	Compare register,immediate, jump not equal relative	3	4 (or 6)	B8-BF
CJNE @Ri,#data,rel	Compare indirect,immediate, jump not equal relative	3	4 (or 6)	B6-B7
DJNZ Rn,rel	Decrement register, jump not zero relative	2	4 (or 6)	D8-DF
DJNZ dir,rel	Decrement direct byte, jump not zero relative	3	4 (or 6)	D5

MISCELLANEOUS				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
NOP	No operation	1	2	00

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11-F1 (for example), are used for absolute jumps and calls with the top 3 bits of the code being used to store the top three bits of the destination address.

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (T_A=25℃)

Parameter	Rating	Unit
Supply voltage	V_{SS} –0.3 ~ V_{SS} +5.5	V
Input voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output current high per all PIN	–80	mA
Output current low per all PIN	+150	
Maximum Operating Voltage	5.5	V
Operating temperature	–40 ~ +105	℃
Storage temperature	–65 ~ +150	

2. DC Characteristics (T_A=25 ℃, V_{CC}=2.2V ~ 5.5V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Operating Voltage	V_{CC}	F_{SYSCLK}=14.7456 MHz		2.2	–	5.5	V
Input High Voltage	V_{IH}	All Input	V_{CC}=5V	0.6V_{CC}	–	–	V
			V_{CC}=3V	0.6V_{CC}	–	–	V
Input Low Voltage	V_{IL}	All Input	V_{CC}=5V	–	–	0.2V_{CC}	V
			V_{CC}=3V	–	–	0.2V_{CC}	V
I/O Port Source Current	I_{OH}	All Output LEDSMDIS=1	V_{CC}=5V, V_{OH}=0.9V_{CC}	6	12	–	mA
			V_{CC}=5V, V_{OH}=0.6V_{CC}	19	38	–	
			V_{CC}=3V, V_{OH}=0.9V_{CC}	2.5	5	–	
			V_{CC}=3V, V_{OH}=0.6V_{CC}	7.5	15	–	
		LED Pins (P0.0~P0.3, P2.0~P2.1, P3.4~P3.7) LEDSMDIS=0	V_{CC}=5V, V_{OH}=0.9V_{CC}	6	12	–	
			V_{CC}=5V, V_{OH}=0.6V_{CC}	11	22	–	
			V_{CC}=3V, V_{OH}=0.9V_{CC}	2.5	5	–	
			V_{CC}=3V, V_{OH}=0.6V_{CC}	4.5	9	–	
I/O Port Sink Current	I_{OL}	All Output,	V_{CC}=5V, V_{OL}=0.1V_{CC} HSNKxEN=1	64	80	–	mA
			V_{CC}=5V, V_{OL}=0.1V_{CC} HSNKxEN=0	32	40	–	
			V_{CC}=3V, V_{OL}=0.1V_{CC} HSNKxEN=1	32	40	–	
			V_{CC}=3V, V_{OL}=0.1V_{CC} HSNKxEN=0	10	20	–	

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Supply Current	I_{DD}	Fast mode V_{CC}=5V	FRC=14.7456 MHz	–	8	–	mA
			FRC=7.3728 MHz	–	5.7	–	
		Fast mode V_{CC}=3V	FRC=14.7456 MHz	–	4.5	–	
			FRC=7.3728 MHz	–	3.3	–	
		Slow mode SRC	V_{CC}=3V	–	2.5	–	
			V_{CC}=5V	–	1.6	–	
		Idle mode PWRSAV=0	SRC, V_{CC}=5V	–	90	–	µA
			SRC, V_{CC}=3V	–	65	–	
		Idle mode PWRSAV=1	SRC, V_{CC}=5V	–	40	–	
			SRC, V_{CC}=3V	–	16	–	
		Stop mode PWRSAV=1	V_{CC}=5V	0.4	–	–	
			V_{CC}=3V	0.1	–	–	
		Halt mode PWRSAV=1	V_{CC}=5V (Timer3=0.5 sec)	23	–	–	
			V_{CC}=3V (Timer3=0.5 sec)	5.5	–	–	
System Clock Frequency	F_{SYSCLK}	V_{CC} >LVR_{TH}	V_{CC}=2.2V	–	–	14.7456	MHz
LVR Reference Voltage	V_{LVR}	T_A=25°C		–	4.3	–	V
				–	4.0	–	
				–	3.7	–	
				–	3.4	–	
				–	3.1	–	
				–	2.8	–	
				–	2.5	–	
				–	2.2	–	
LVR Hysteresis Voltage	V_{HYST}	T_A=25°C		–	±0.1	–	V
Low Voltage Detection time	t_{LVR}	T_A=25°C		100	–	–	µs
Pull-Up Resistor	R_P	V_{IN}=0V	V_{CC}=5V	–	30	–	KΩ
			V_{CC}=3V		50		

3. Clock Timing (T_A= –40°C ~ +105°C)

Parameter	Condition	Min	Typ	Max	Unit
FRC Frequency	25°C, V_{CC}=5.0V	–1%	14.7456	+1%	MHz
	0°C ~ 105°C, V_{CC}=5.0V	–1.5%	14.7456	+1.5%	
	–40°C ~ 105°C, V_{CC}=3.0 ~ 5.5V	–3%	14.7456	+3%	

4. Reset Timing Characteristics (T_A= –40°C ~ +105°C)

Parameter	Conditions	Min	Typ	Max	Unit
RESET Input Low width	Input V_{CC}=5V ± 10 %	30	–	–	μs
WDT wakeup time	V_{CC}=5V, WDTPSC=11	–	50	–	ms
	V_{CC}=3V, WDTPSC=11	–	56	–	

5. ADC Electrical Characteristics (T_A= 25°C, V_{CC}= 3.0V ~ 5.5V, V_{SS}= 0V)

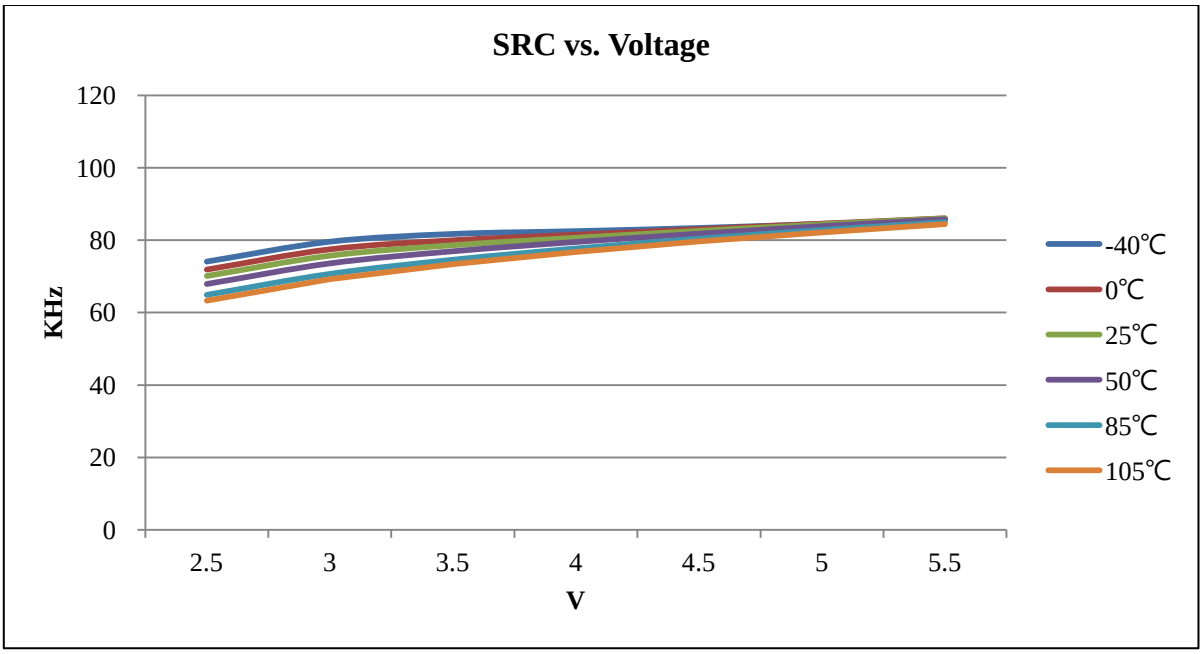
Parameter	Conditions	Min	Typ	Max	Unit
Total Accuracy	V_{CC}=5.12 V, V_{SS}=0V	–	±2.5	±4	LSB
Integral Non-Linearity		–	±3.2	±5	
Max Input Clock (f_{ADC}) Total Accuracy	Source impedance（Rs < 10K omh）	–	–	2	MHz
	Source impedance（Rs < 20K omh）	–	–	1	
	Source impedance（Rs < 50K omh）	–	–	0.5	
	Source is V_{BG}（ADCHS=1011b）	–	–	2.3	
Integral Non-Linearity	F_{ADC} = 1MHz	–	50	–	μs
BandGap Voltage Reference (V_{BG})	-40°C ~105°C, V_{CC}=3V~5.5V	-1.5%	1.20	+1.5%	V
ADC reference voltage (V_{REF})	-40°C ~105°C, V_{CC}=3V~5.5V (ADCVREFS=1)	-1.5%	2.5	+1.5%	
V_{CC}/4 reference voltage	V_{CC}=5V, 25°C	-0.8%	1.26	+0.8%	
	V_{CC}=3.6V, 25°C	-0.8%	0.907	+0.8%	
Input Voltage	–	V_{SS}	–	V_{CC}	

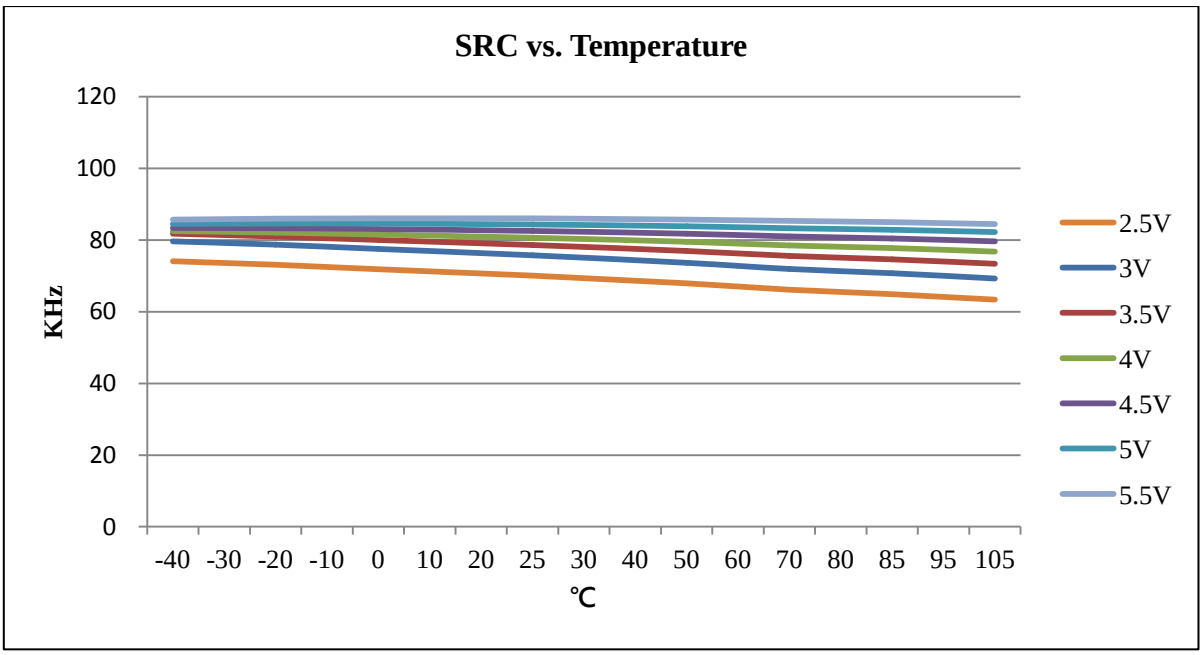
6. EEPROM Characteristics

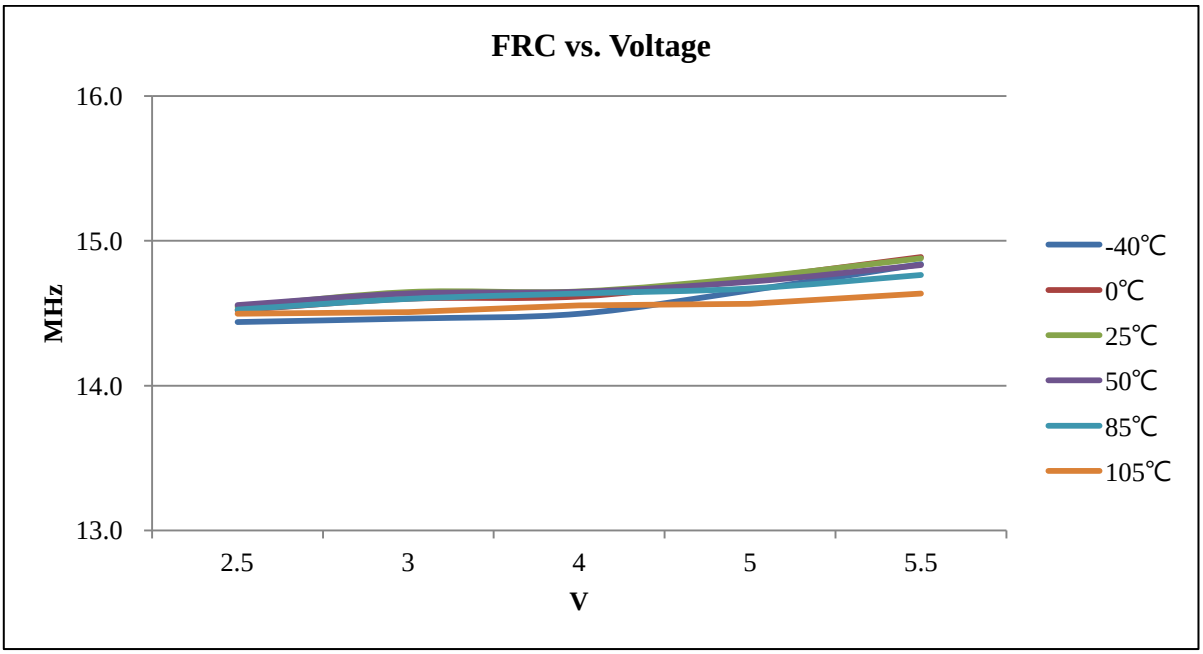
Parameter	Conditions	Min	Typ	Max	Unit
Write Voltage	-20°C ~ 85°C	3.0	5	5.5	V
	0°C ~ 105°C	4.5	5	5.5	
Write Endurance*	V_{CC} = 5 V, -20°C	30K	–	–	cycles
	V_{CC} = 5 V, -10°C	50K	–	–	
	V_{CC} = 3.0V ~ 5V, 85°C	50K	–	–	
	V_{CC} = 4.5V, 0°C ~ 105°C	50K	–	–	

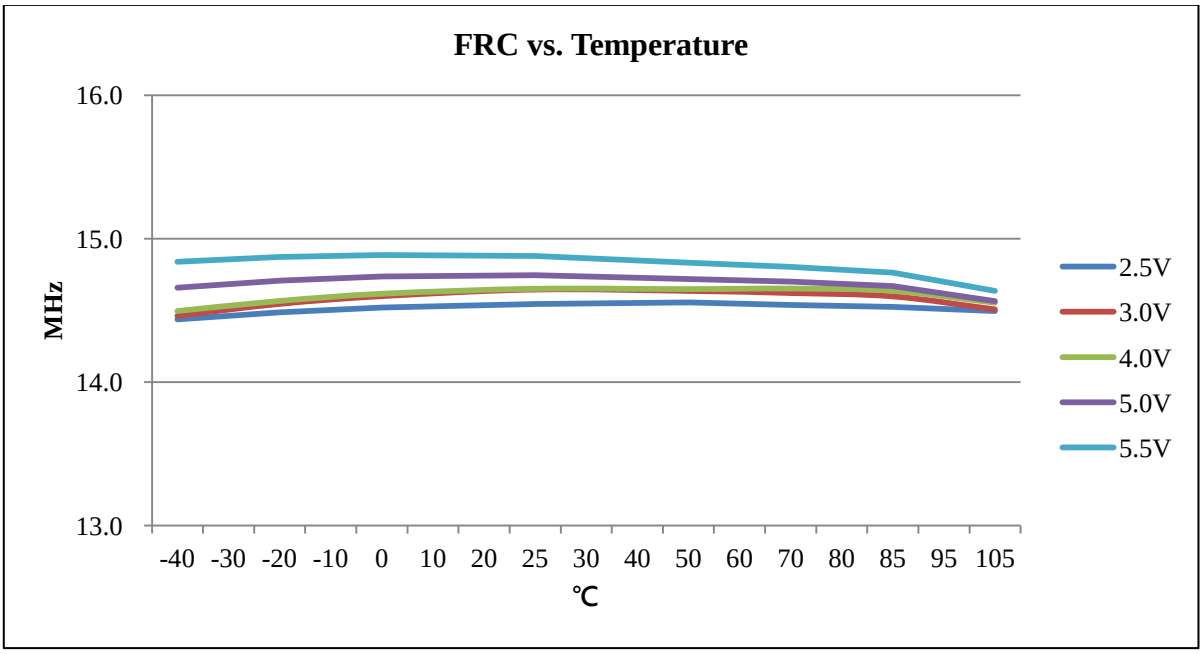
Note: The value of this parameter is based on the characteristics of tested samples.

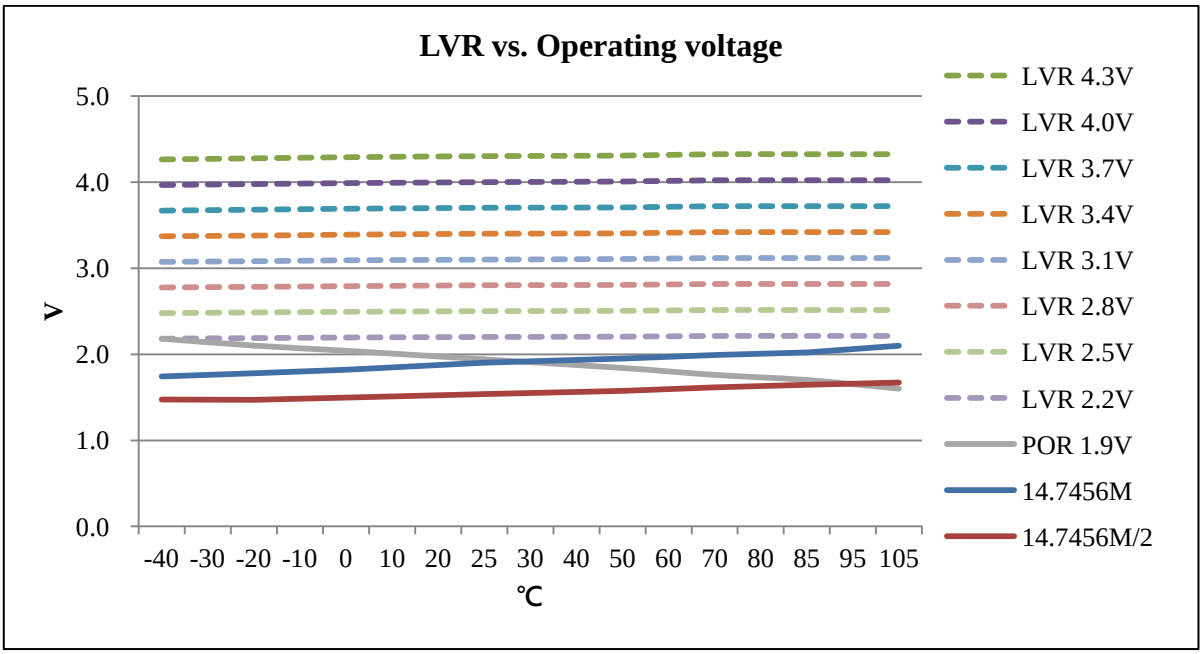
7. Characteristic Graphs

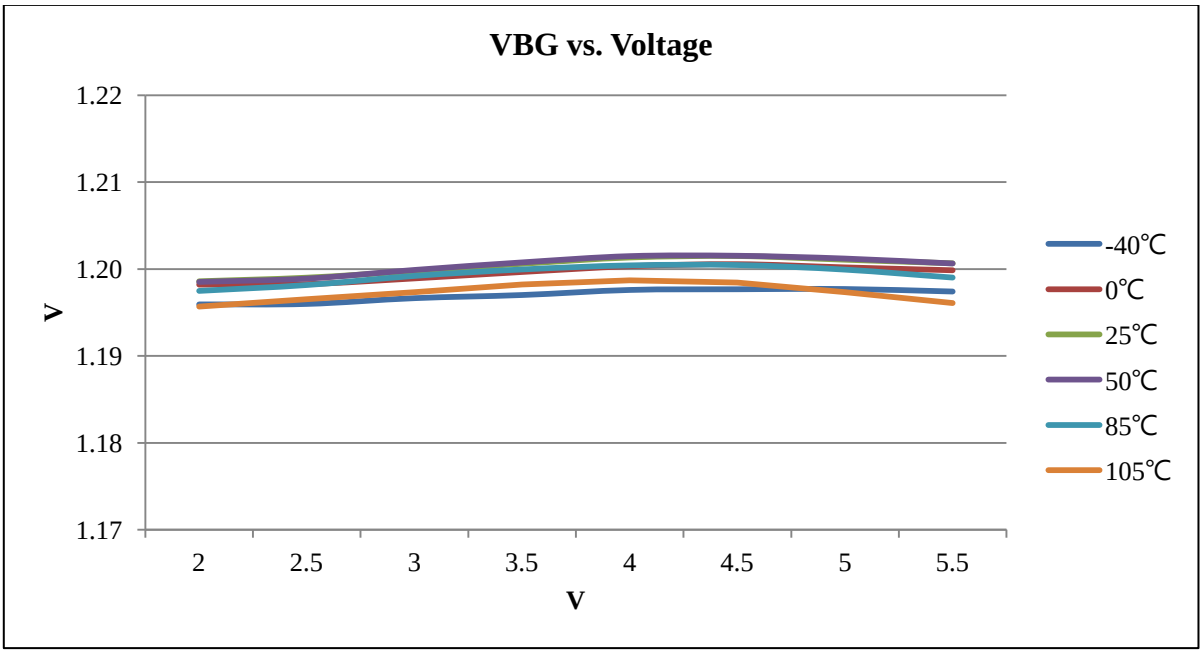





FRC vs. Voltage
16.0
15.0
14.0
13.0
MHz
2.5
3
4
5
5.5
V
-40℃
0℃
25℃
50℃
85℃
105℃


FRC vs. Temperature
16.0
15.0
14.0
13.0
MHz
-40 -30 -20 -10 0 10 20 25 30 40 50 60 70 80 85 95 105
℃
2.5V
3.0V
4.0V
5.0V
5.5V


LVR vs. Operating voltage
5.0
4.0
3.0
2.0
1.0
0.0
V
-40 -30 -20 -10 0 10 20 25 30 40 50 60 70 80 85 95 105
℃
LVR 4.3V
LVR 4.0V
LVR 3.7V
LVR 3.4V
LVR 3.1V
LVR 2.8V
LVR 2.5V
LVR 2.2V
POR 1.9V
14.7456M
14.7456M/2


VBG vs. Voltage
1.22
1.21
1.20
1.19
1.18
1.17
V
2 2.5 3 3.5 4 4.5 5 5.5
V
-40℃
0℃
25℃
50℃
85℃
105℃

Package and Dice Information

Please note that the package information provided is for reference only. Since this information is frequently updated, users can contact Sales to consult the latest package information and stocks.

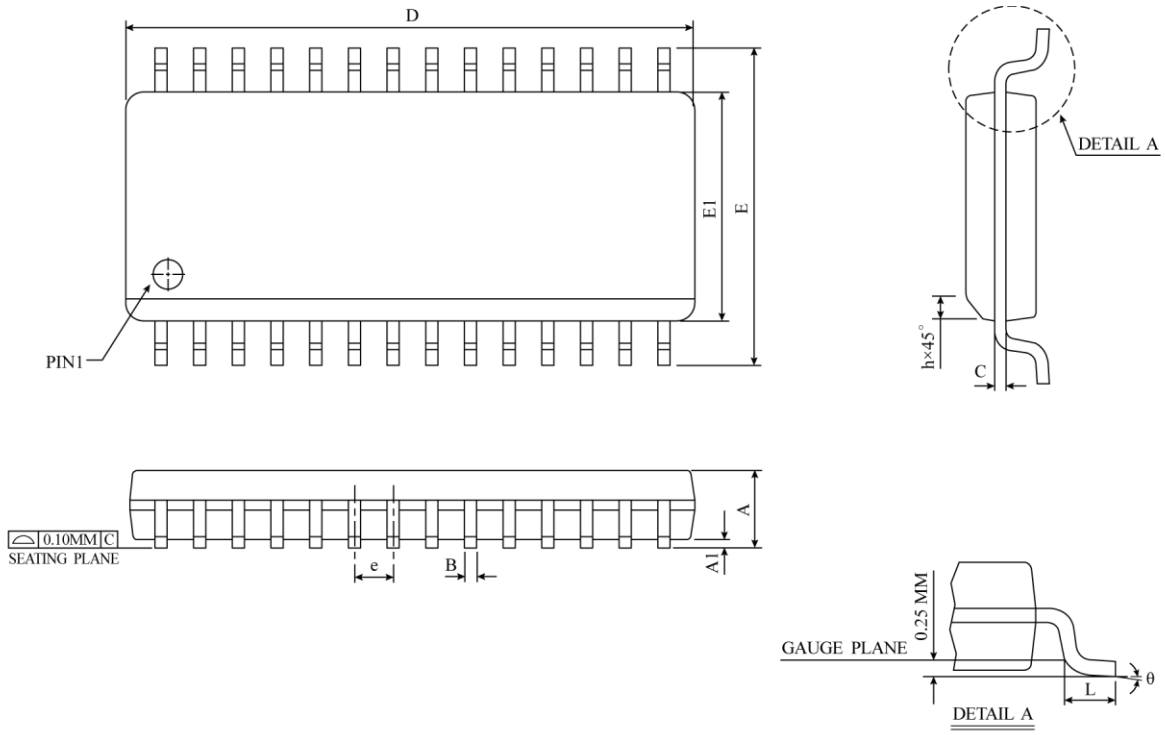
Ordering information

Ordering number	Package
TM52FN8273-MTP	Wafer/Dice blank chip
TM52FN8276-MTP	
TM52FN8274-MTP	
TM52FN8278-MTP	
TM52FN8273-COD	Wafer/Dice with code
TM52FN8276-COD	
TM52FN8274-COD	
TM52FN8278-COD	
TM52FN8273-MTP-23	SOP 28-pin (300 mil)
TM52FN8276-MTP-23	
TM52FN8274-MTP-23	
TM52FN8278-MTP-23	
TM52FN8273-MTP-29	SSOP 28-pin (150 mil)
TM52FN8276-MTP-29	
TM52FN8274-MTP-29	
TM52FN8278-MTP-29	
TM52FN8273-MTP-C3	QFN 28-pin (4x4x0.75-0.4 mm)
TM52FN8276-MTP-C3	
TM52FN8274-MTP-C3	
TM52FN8278-MTP-C3	

TM52FN8273-MTP-28	SSOP 24-pin (150 mil)
TM52FN8276-MTP-28	
TM52FN8274-MTP-28	
TM52FN8278-MTP-28	
TM52FN8273-MTP-21	SOP 20-pin (300 mil)
TM52FN8276-MTP-21	
TM52FN8274-MTP-21	
TM52FN8278-MTP-21	
TM52FN8273-MTP-D1	QFN 20-pin (3x3x0.75-0.4 mm) (L=0.25mm)
TM52FN8276-MTP-D1	
TM52FN8274-MTP-D1	
TM52FN8278-MTP-D1	
TM52FN8273-MTP-16	SOP 16-pin (150 mil)
TM52FN8276-MTP-16	
TM52FN8274-MTP-16	
TM52FN8278-MTP-16	

Package Information

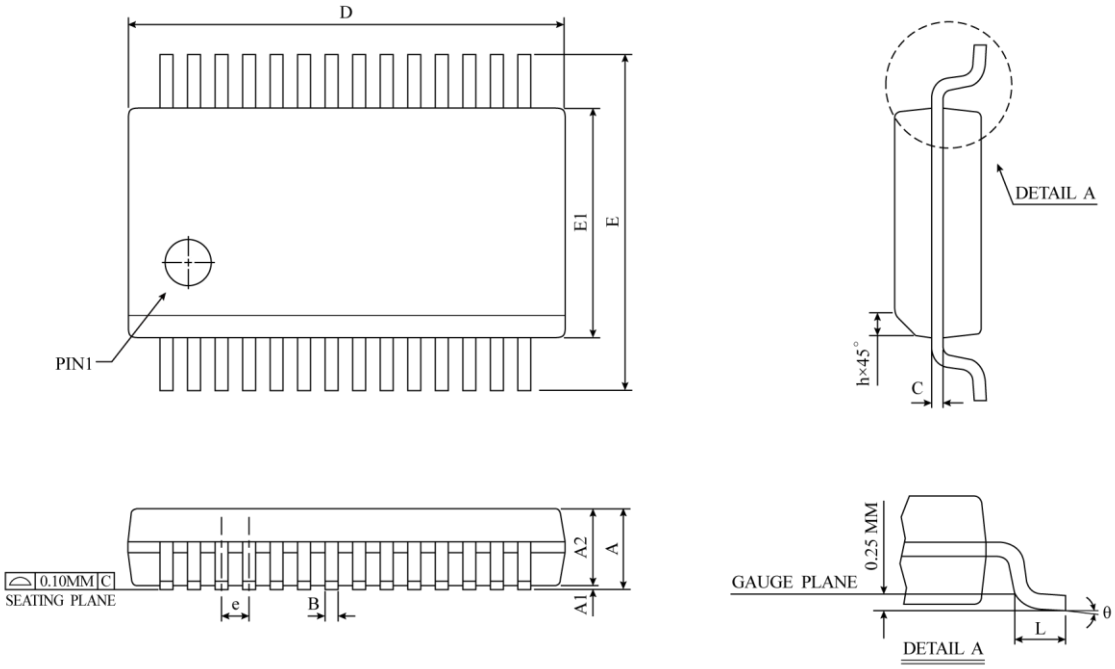
SOP-28 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	17.70	17.90	18.10	0.6969	0.7047	0.7125
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AE)					

* NOTES：DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

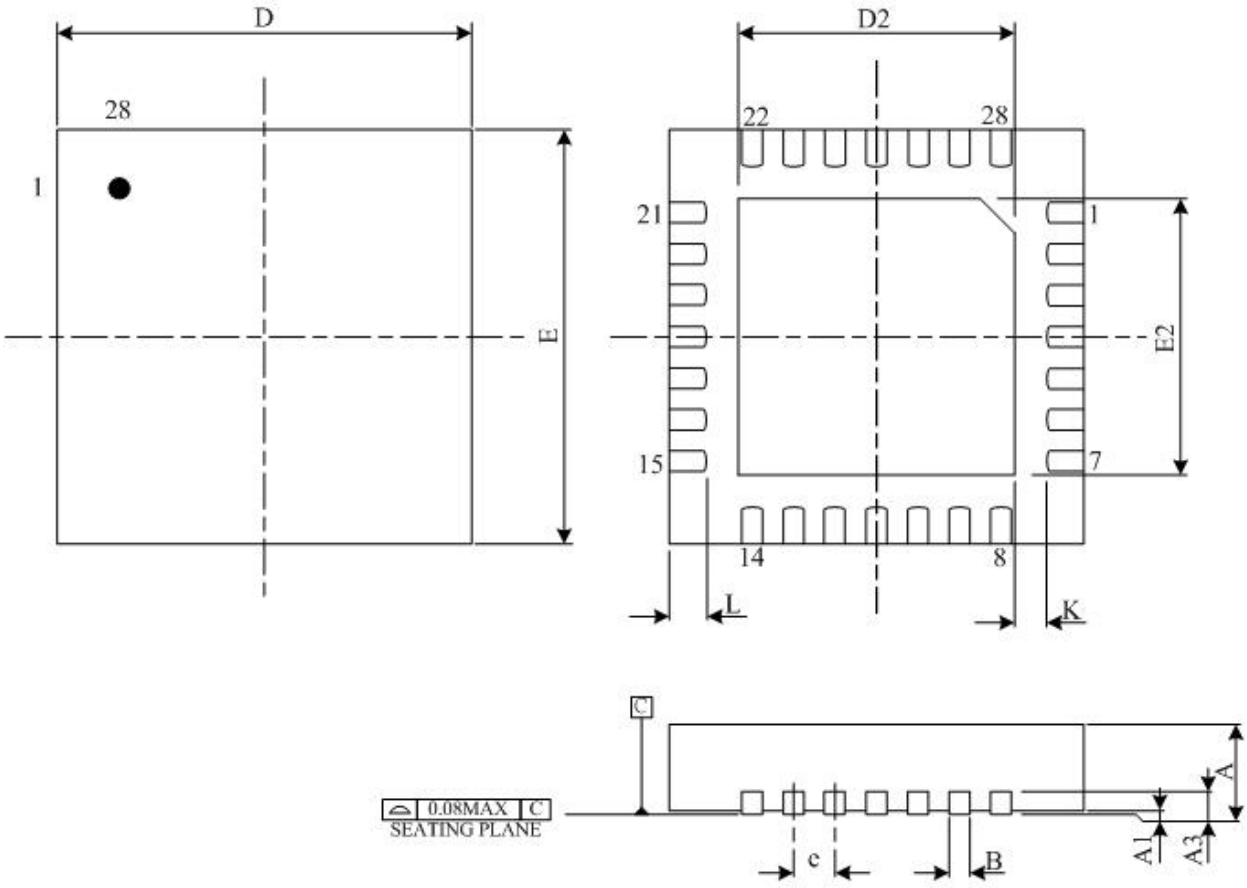
SSOP-28 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.65	1.80	0.06	0.06	0.07
A1	0.102	0.176	0.249	0.004	0.007	0.010
A2	1.40	1.475	1.55	0.06	0.06	0.06
B	0.20	0.25	0.30	0.01	0.01	0.01
C	0.2TYP			0.008TYP		
e	0.635TYP			0.025TYP		
D	9.804	9.881	9.957	0.386	0.389	0.392
E	5.842	6.020	6.198	0.230	0.237	0.244
E1	3.86	3.929	3.998	0.152	0.155	0.157
L	0.406	0.648	0.889	0.016	0.026	0.035
θ	0°	4°	8°	0°	4°	8°
JEDEC	M0-137(AF)					

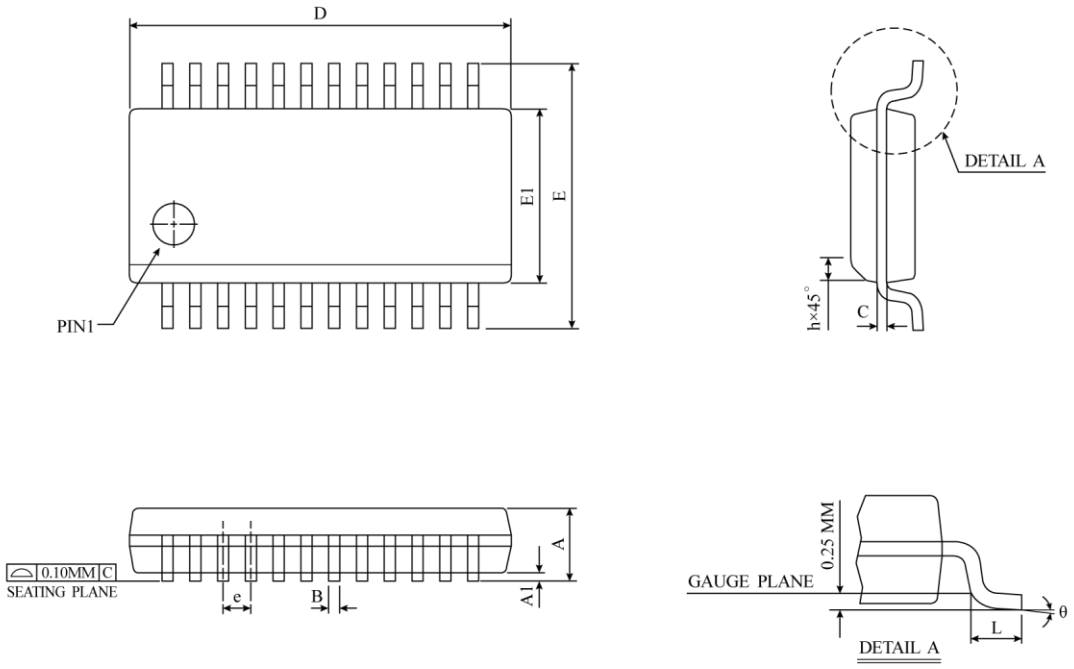
△B *NOTES：DIMENSION “D” DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE.

QFN-28 (4x4x0.75-0.4mm) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.7	0.75	0.8	0.028	0.030	0.031
A1	0	0.02	0.05	0	0.001	0.002
A3	0.203 REF			0.008 REF		
B	0.15	0.2	0.25	0.006	0.008	0.010
D	4 BSC			0.157		
E	4 BSC			0.157		
D2	2.2	2.3	2.4	0.087	0.091	0.094
E2	2.2	2.3	2.4	0.087	0.091	0.094
e	0.4 BSC			0.016		
L	0.3	0.4	0.5	0.012	0.016	0.020
K	0.45 REF			0.018		
JEDEC	MO-220					

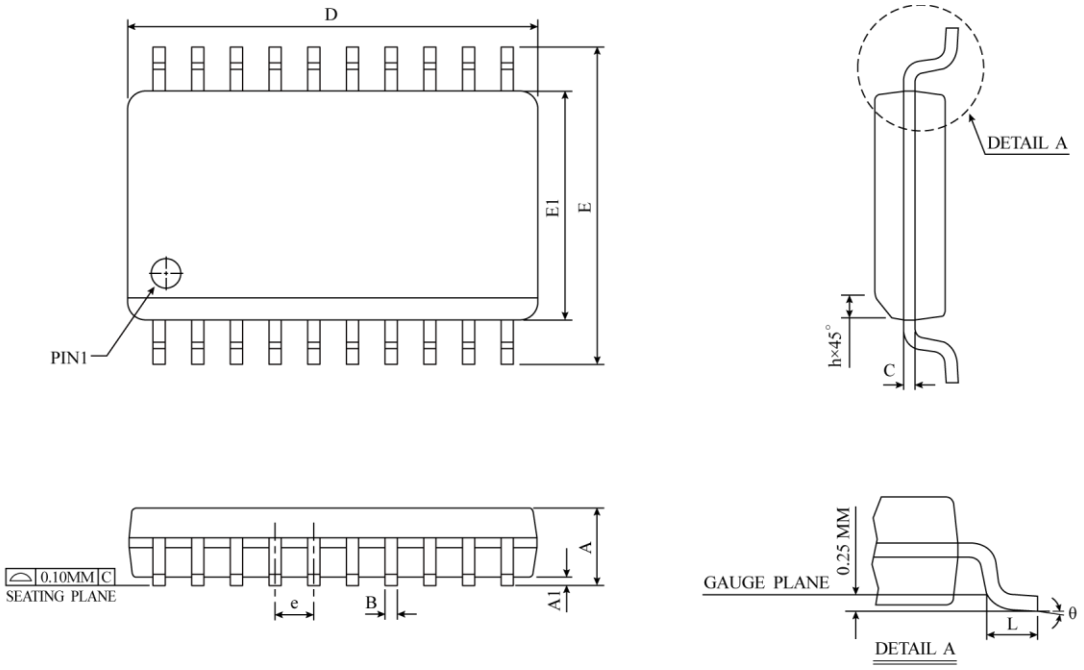
SSOP-24 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.18	0.25	0.004	0.007	0.010
A2	-	-	1.50	-	-	0.059
B	0.20	0.25	0.30	0.008	0.010	0.012
C	0.18	0.22	0.25	0.007	0.009	0.010
D	8.56	8.65	8.74	0.337	0.341	0.344
E	5.79	6.00	6.20	0.228	0.236	0.244
E1	3.81	3.90	3.99	0.150	0.154	0.157
e	0.635 BSC			0.025 BSC		
L	0.41	0.84	1.27	0.016	0.033	0.050
θ	0°	4°	8°	0°	4°	8°
JEDEC	M0-137 (AE)					

Ⓑ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD PROTRUSIONS OR GAT BURRS.
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE.

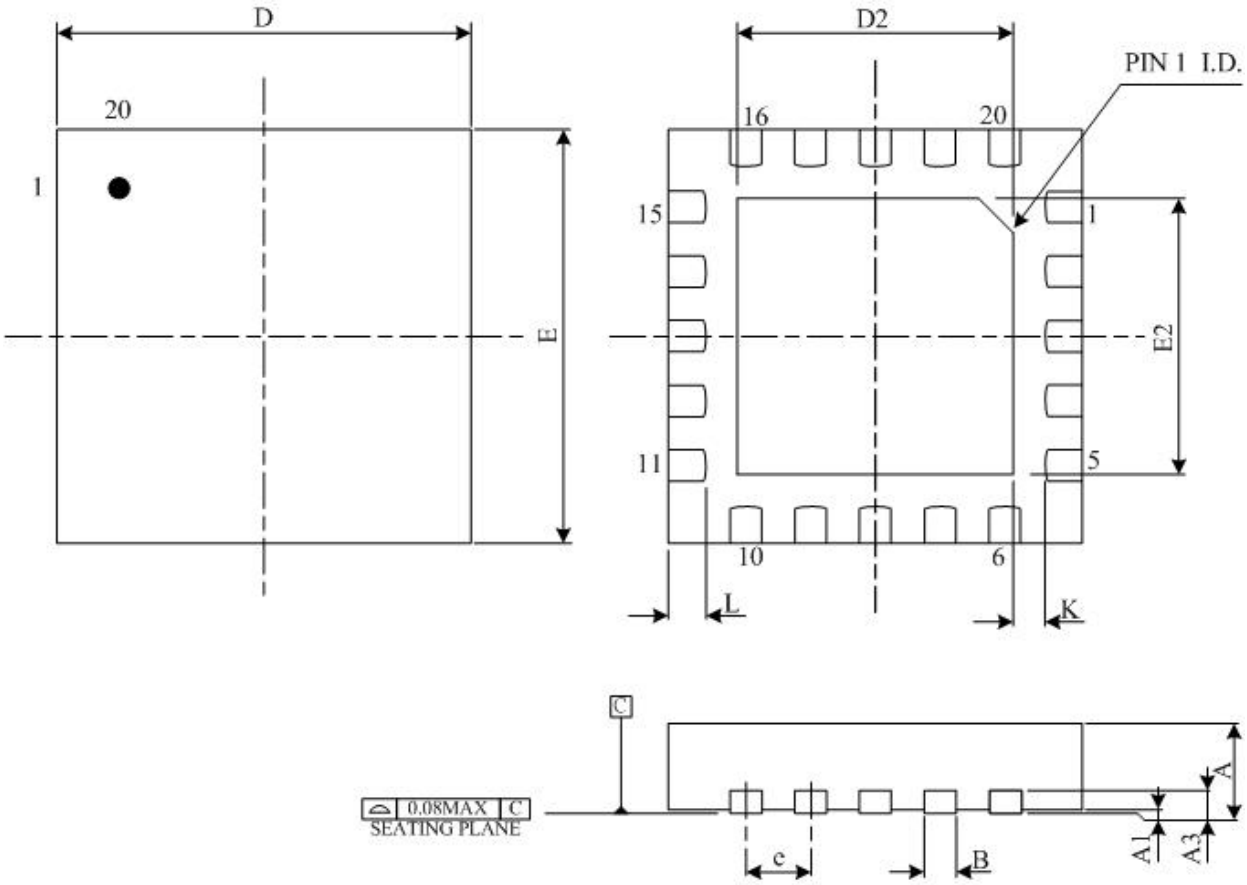
SOP-20 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	12.60	12.80	13.00	0.4961	0.5040	0.5118
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AC)					

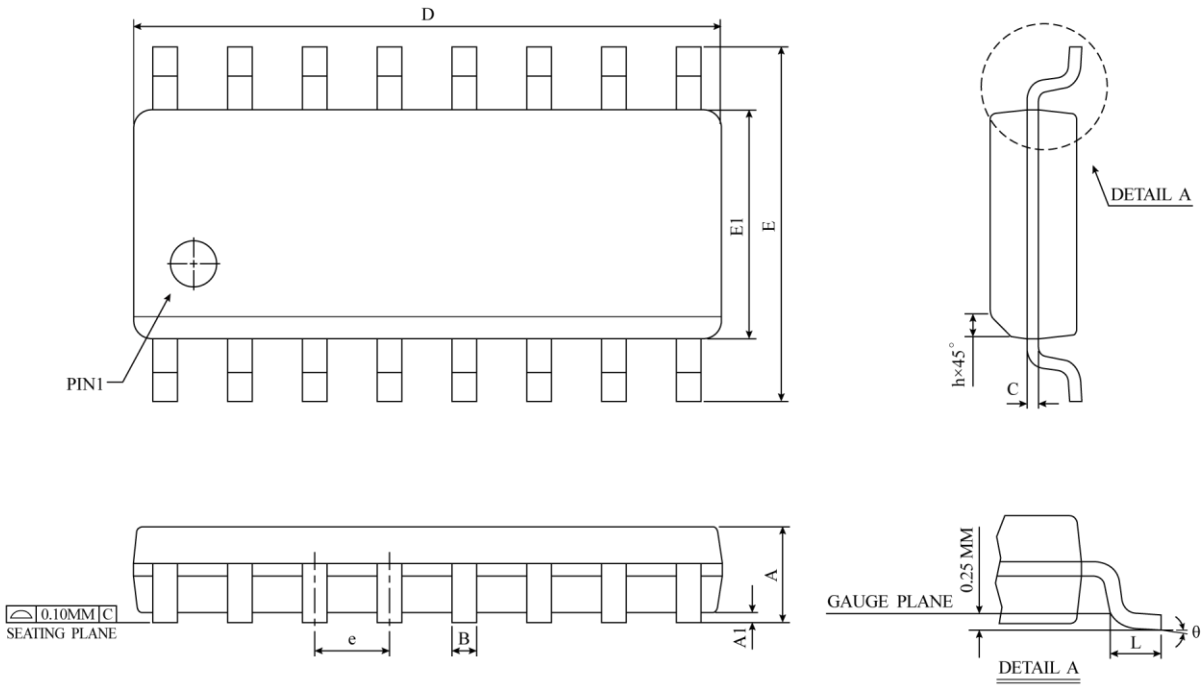
⚠ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

QFN-20 (3x3x0.75-0.4mm) (L=0.25mm) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.00	0.001	0.002
A3		0.203 REF			0.008 REF	
B	0.15	0.20	0.25	0.006	0.008	0.010
D		3 BSC			0.118 BSC	
E		3 BSC			0.118 BSC	
D2	1.80	1.90	2.00	0.071	0.075	0.079
E2	1.80	1.90	2.00	0.071	0.075	0.079
e		0.40 BSC			0.016 BSC	
L	0.15	0.25	0.35	0.006	0.010	0.014
K		0.30 REF			0.012 REF	
JEDEC		MO-220				

SOP-16 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	9.80	9.90	10.00	0.3859	0.3898	0.3937
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AC)					

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