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TM57MA29NE

DATA SHEET

Rev 0.92

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AMENDMENT HISTORY

Version	Date	Description
0.90	Aug, 2022	New release.
0.91	Sep, 2022	1. Modify VBG2.57V to VBG2.60V 2. Add PA4 for programming pin (p.14) 3. Modify SIRC 2K to SIRC 120K (p.76)
0.92	Oct, 2022	1. Add VCC=105°C related information, update VBG characteristics, update DC characteristic curve

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FAMILY OVERVIEW

P/N	ROM	GPIO (max)	Timer	PWM	ADC	1/2 VCC for LCD	Natural Reset	Timepiece current
TM57MA28/28B	2K MTP	18	8-bit*2 15-bit*1	(8+2) bit*2	12-bit 11-ch Vref = VCC	Y	N	3uA
TM57MA28MB	2K MTP	18	8-bit*2 15-bit*1	(8+2) bit*2	12-bit 11-ch Vref = VCC	Y	N	4uA
TM57MA29C	2K MTP	18	8-bit*2 15-bit*1	(8+2) bit*2	12-bit 11-ch Vref = VCC or VBG2.57v	Y	Y	4uA
TM57MA29NE	2K MTP	18	8-bit*2 15-bit*1	(8+2) bit*2	12-bit 11-ch Vref = VCC or VBG2.60v	Y	Y	15uA

*Natural Reset: Natural reset for protect ROM when low operating voltage.

*Timepiece current: IDLE mode, under VCC=3V, CPUCLK(Fsys) closed, LVR2.3V, PWRSV enable condition.

	EV2781C	TM57MA29C	TM57MA29NE
EV board	-	EV2781C	EV2781C
SRAM	Common: 20~27	Common: 20~27	Common: 20~27
	Bank0: 28~7F	Bank0: 28~7F	Bank0: 28~7F
	Bank1: 28~7F		
Fast-clock	FXT / XRC / FIRC	FIRC	FIRC
Slow-clock	SXT/ XRC / SIRC (140 KHz@5V)	SIRC (120 KHz@5V)	SIRC (120 KHz@5V)
INT0 (PA6) edge interrupt event	Only support falling edge emulation	Falling or rising select by the INT0EDGE of SYSCFG	Falling or rising select by the INT0EDGE of SYSCFG
Internal VBG	1.25V+/-10%	1.25V+/-2%	1.25V+/-2%
Touch Key	Y	N	N
Buzzer	Y	N	N
WKT	14~113ms @5V	17~136ms @5V	17~136ms @5V
WDT	110~1680 ms @5V	137~2192 ms @5V	137~2192 ms @5V
1/2 bias LCD	Yes	Yes, SYSCFG[9] option	Yes, SYSCFG[9] option
PA4 Vih (typ) @5V	3.6V	2.7V	2.8V
PA4 Vil (typ) @5V	0.8V	1.5V	1.3V
PA3 Vih (typ) @5V	3.0V	2.7V	2.8V
IO R _{UP} @5V	140Kohm	40Kohm	32Kohm
I/O	18 I/O + ICE I/F	18 I/O	18 I/O
	LQFP128	PA7~0, PB1~0, PD7~0	PA7~0, PB1~0, PD7~0
ADC Reference Voltage	VCC	VCC or VBG2.57V	VCC or VBG2.60V
Natural reset	N	Y	Y
Reserved SFR	N	F1C.1~0 = Natural Reset F1D.5~3=3'b110(fixed) F1D.2=ADCVREFS F1F.6~0=IRCF R16.7~0=LVR20OFF	F1C.1~0 = Natural Reset F1D.5~3=3'b110(fixed) F1D.2=ADCVREFS F1F.6~0=IRCF R16.7~0=LVR20OFF

FEATURES

1. **ROM: 2K x 14 bits MTP (Multi Time Programmable ROM)**
2. **RAM: 96 x 8 bits**
3. **STACK: 6 Levels**
4. **System Oscillation Sources (Fsys)**
 - Fast-clock
 - FIRC (Fast Internal RC): 1.5M/4M/6M/12MHz
 - Slow-clock
 - SIRC (Slow Internal RC): 120KHz/30KHz/7.5KHz/1.875KHz
5. **Dual System Clock**
 - FIRC+SIRC
6. **Power Saving Operation Mode**
 - FAST Mode: Slow-clock can be disabled or enabled; Fast-clock keeps CPU running
 - SLOW Mode: Fast-clock can be disabled or enabled; Slow-clock keeps CPU running
 - IDLE Mode: Fast-clock and CPU stop. Slow-clock, T2, or Wake-up Timer keep running
 - STOP Mode: All Clocks stop, T2 and Wake-up Timer stop
7. **3 Independent Timers**
 - Timer0
 - 8-bit timer divided by 1~256 prescaler option, Counter/Interrupt/Stop function
 - Timer1
 - 8-bit timer divided by 1~256 prescaler option, Reload/Interrupt/Stop function
 - Overflow and Toggle out
 - T2
 - 15-bit timer with 4 interrupt interval time options
 - IDLE mode wake-up timer or used as one simple 15-bit time base
 - Clock source: Slow-clock (SIRC), Fsys/128
8. **Interrupt**
 - Three External Interrupt pins
 - 2 pins are falling edge wake-up triggered & interrupts
 - 1 pin is rising or falling edge wake-up triggered & interrupt
 - Timer0/Timer1/T2/WKT (wake-up) Interrupts

9. Wake-up (WKT) Timer

- Clocked by built-in RC oscillator with 4 adjustable interrupt times
 - 17 ms/34 ms/68 ms/136 ms

10. Watchdog Timer

- Clocked by built-in RC oscillator with 4 adjustable reset times
 - 137 ms/274 ms/1096 ms/2192 ms
- Watchdog can be disabled in IDLE/STOP mode (R15.5)

11. 2 Independent PWMs

- PWM0:
 - 8+2 bits, duty-adjustable, period-adjustable controlled PWM
 - PWM0 clock source: Fast-clock or Fast-clock-pre(12MHz)*, with 1~64 prescaler
- PWM1:
 - 8+2 bits, duty-adjustable controlled PWM
 - PWM1 clock source: Fast-clock or Fast-clock-pre*

*Note: **Fast-clock-pre** is the original fast clock, Fast-clock is the divided clock of Fast-clock-pre.

12. 12-bit ADC Converter with 11 input channels(CH0~CH10)

- Internal reference voltage 1.25V \pm 2% on channel-11 when ADC reference source = VCC.
- ADC reference voltage source: VCC or VBG 2.60V.

13. Built-in 1/2 bias VCC/2 voltage generator to PD3~PD0 maximum 4x13 dots for LCD display**14. Reset Sources**

- Power On Reset/Watchdog Reset/Low Voltage Reset/External Pin Reset

15. Four kinds of Low Voltage Reset option:

- LVR2.0V, LVR2.0V(off in IDLE/STOP mode), LVR2.3V, LVR2.9V

16. Enhanced Power Noise Rejection**17. Operating Voltage: Low Voltage Reset Level to 5.5V****18. Operating Temperature Range: -40°C to +105°C****19. Table Read Instruction: 14-bit ROM data lookup table.****20. Instruction set: 38 Instructions****21. Instruction Execution Time**

- 2 oscillation clocks per instruction except branch

22. I/O ports: Maximum 18 programmable I/O pins

- Pseudo-Open-Drain Output (PA2~PA0)
- Open-Drain Output
- CMOS Push-Pull Output
- Schmitt Trigger Input with pull-up resistor option

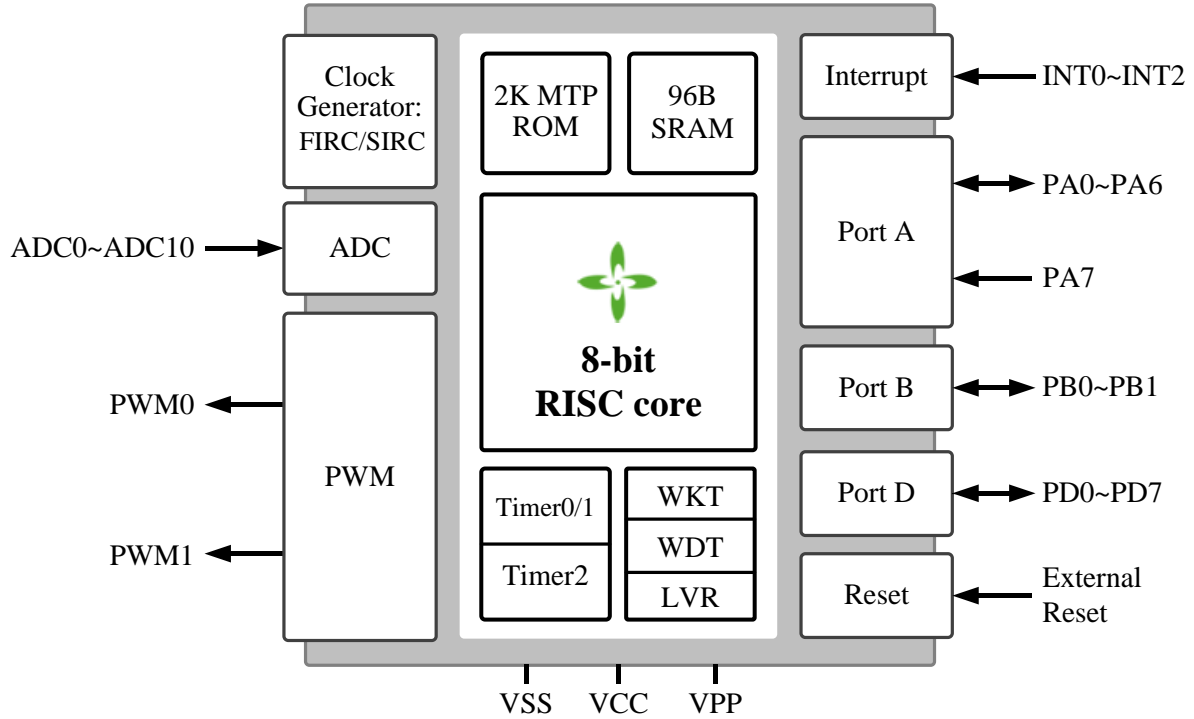
23. Programming connectivity support 6-wire (ISP) or 8-wire program.**24. Package Types:**

- 20-pin DIP (300 mil), SOP (300 mil) , SSOP (150 mil),TSSOP(173mil) , QFN (3x3x0.75mm)
- 16-pin DIP(300 mil), SOP (150 mil) , SSOP (150mil)
- 14-pin SOP (150 mil)
- 10-pin MSOP (118 mil)
- 8-pin SOP (150 mil)
- 6-pin SOT23

25. Supported EV board on ICE

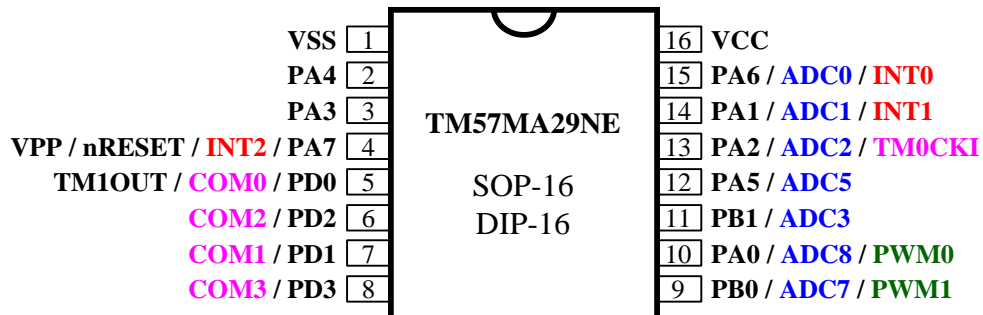
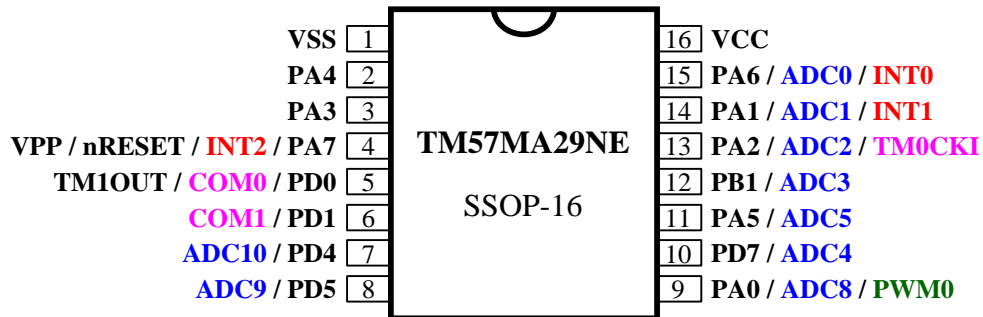
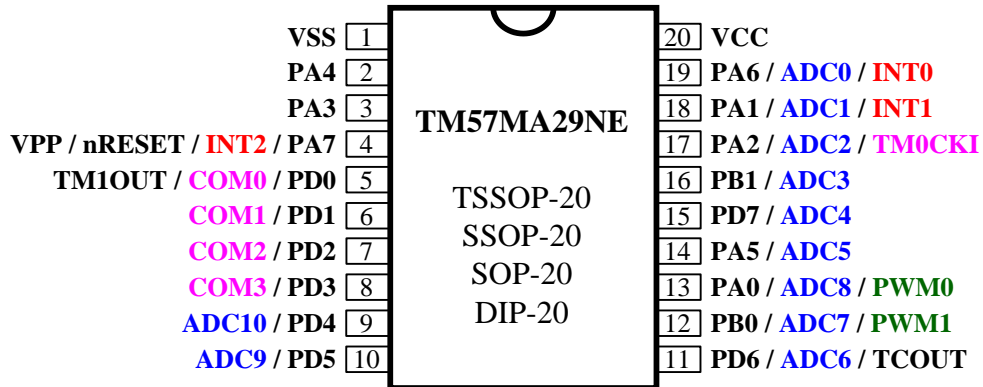
EV board: EV2781C

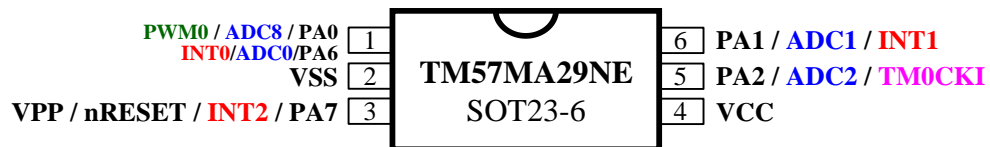
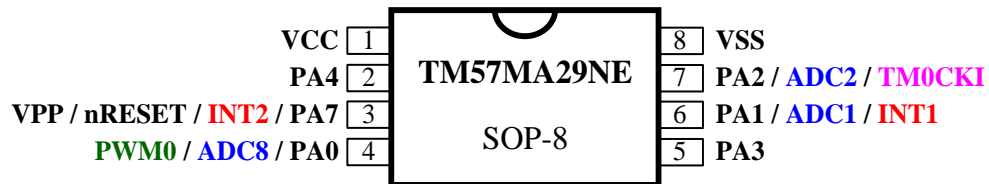
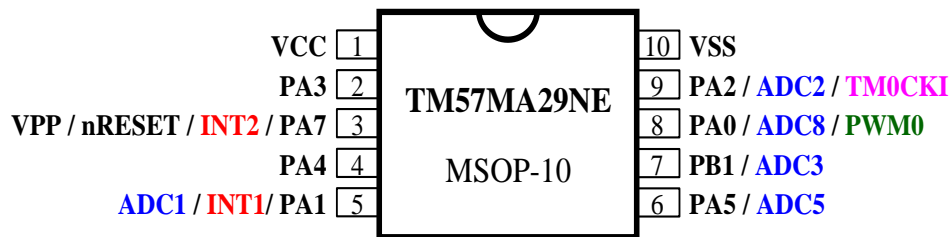
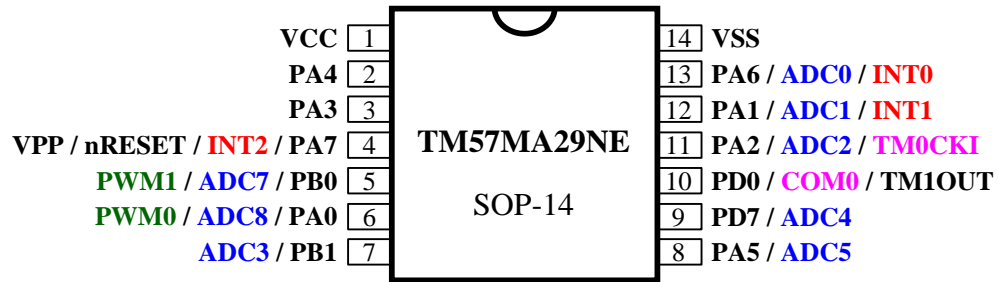
BLOCK DIAGRAM

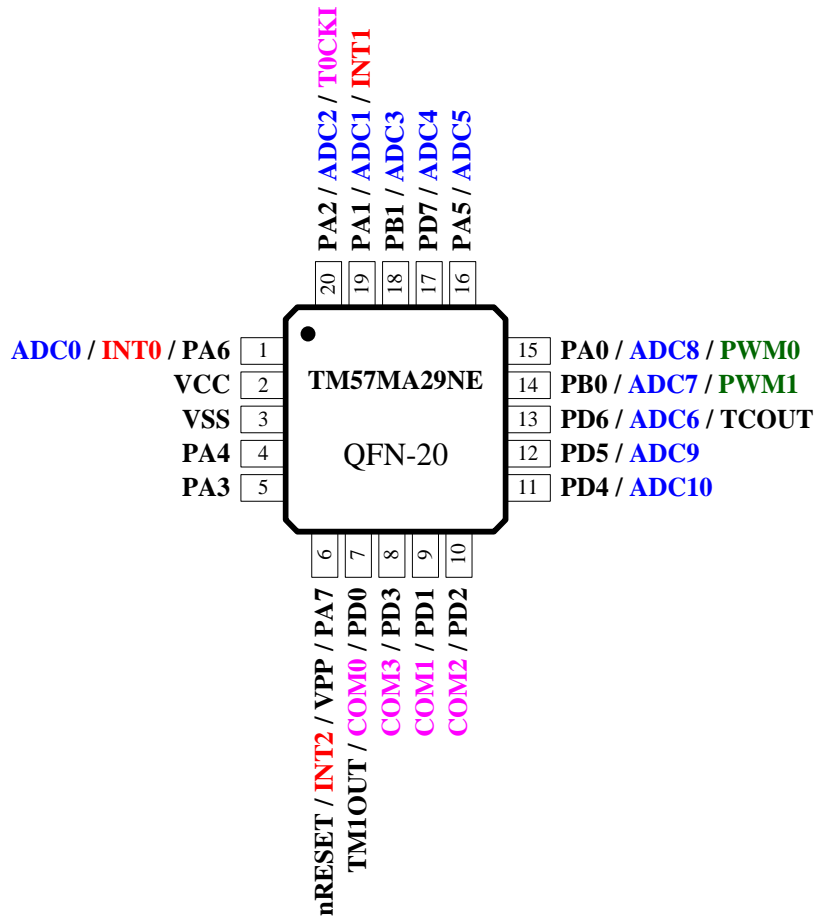


TM57MA29NE Block Diagram

PIN ASSIGNMENT







PIN DESCRIPTIONS

Name	In/Out	Pin Description
PA0-PA2	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS “ push-pull ” output or “ pseudo-open-drain ” output. Pull-up resistors are assignable by software.
PA3-PA6 PB0-PB1 PD0-PD7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS “ push-pull ” output or “ open-drain ” output. Pull-up resistors are assignable by software.
PA7	I	Schmitt-trigger input with pull-high
nRESET	I	External active low reset, internal pull-high
VCC, VSS	P	Power Voltage input pin and ground
VPP	I	PROM programming high voltage input
INT0-INT2	I	External interrupt input
TM0CKI	I	Timer0’s input in counter mode
TM1OUT	O	Timer1 match output, TM1OUT toggles when Timer1 overflow occurs.
TCOUT	O	Instruction cycle clock divided by N output. Where N is 1,2,4,8. The instruction clock frequency is system clock frequency divided by two ($F_{sys}/2$).
PWM0/PWM1	O	(8+2) bit PWM output
ADC10~ADC0	I	A/D channels input
COM3~COM0	O	1/2 bias VCC/2 provide for LCD display

Note: Programming pins are list below. It is better to remove the PCB components connected to these pins during In-Circuit-Programming.

8- wire mode: VCC/VSS/PA0/PA1/PA2/PA3/PA4/PA7(VPP)

6- wire mode: VCC/VSS/PA0/PA1/PA4/PA7(VPP)

PIN SUMMARY

20-SOP/DIP	16-SOP/DIP	Pin Name	Type	GPIO					Function After Reset	Alternate Function			
				Input		Output				PWM	LCD	ADC	MISC
				Weak Pull-up	Ext. Interrupt	P.O.D	O.D	P.P					
1	1	VSS	P										
2	2	PA4	I/O	○			○	○					
3	3	PA3	I/O	○			○	○					
4	4	VPP/nRESET/INT2/PA7	I	○	○				SYS				nRESET
5	5	TM1OUT/PD0	I/O	○			○	○	PD0		○		TM1OUT
6	6	PD1	I/O	○			○	○	PD1		○		
7	-	PD2	I/O	○			○	○	PD2		○		
8	-	PD3	I/O	○			○	○	PD3		○		
9	7	ADC10/PD4	I/O	○			○	○	PD4			○	
10	8	ADC9/PD5	I/O	○			○	○	PD5			○	
11	-	PD6/ADC6/TCOUT	I/O	○			○	○	PD6			○	TCOUT
12	-	PB0/ADC7/PWM1	I/O	○			○	○	PB0	○		○	
13	9	PA0/ADC8/PWM0	I/O	○		○		○	PA0	○		○	
14	11	PA5/ADC5	I/O	○			○	○	PA5			○	
15	10	PD7/ADC4	I/O	○			○	○	PD7			○	
16	12	PB1/ADC3	I/O	○			○	○	PB1			○	
17	13	PA2/ADC2/TM0CKI	I/O	○		○		○	PA2			○	TM0CKI
18	14	PA1/ADC1/INT1	I/O	○	○	○		○	PA1			○	
19	15	PA6/ADC0/INT0	I/O	○	○		○	○	PA6			○	
20	16	VCC	P										

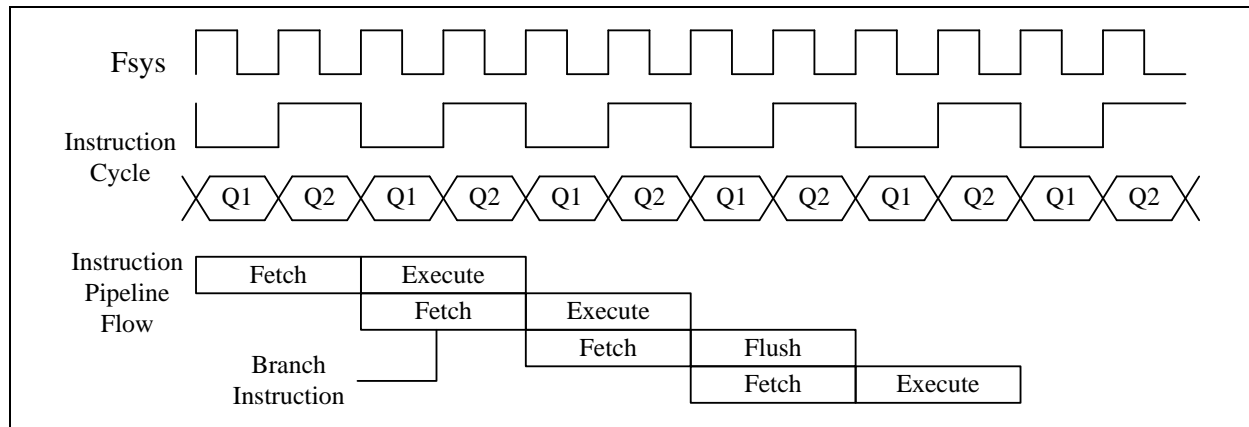
Symbol : P.P. = Push-Pull Output
 P.O.D. = Pseudo Open Drain
 O.D. = Open Drain
 SYS = by SYSCFG bit

FUNCTIONAL DESCRIPTION

1. CPU Core

1.1 Clock Scheme and Instruction Cycle

The system clock is internally divided by two to generate Q1 state and Q2 state for each instruction cycle. The Programming Counter (PC) is updated at Q1 and the instruction is fetched from program ROM and latched into the instruction register in Q2. It is then decoded and executed during the following Q1-Q2 cycle. Branch instructions take two cycles since the fetch instruction is ‘flushed’ from the pipeline, while the new instruction is being fetched and then executed.



When $F_{sys}=4$ MHz, the two instruction cycles time (CALL, RET...) =1uS, single instruction cycle time (MOVWF...) =0.5uS

Terminology definitions:

- (1) **Fast-clock-pre:** The clock source that contains one fast frequency oscillation: Fast Internal RC oscillator (FIRC).
- (2) **Fast-clock:** The words means the all set of fast clocks, its clock frequency can be Fast-clock-pre divided by 1, 2, 3, 8.
- (3) **Slow-clock:** The clock source that contains Slow Internal RC oscillator (SIRC).
- (4) **Fsys:** System clock. The main clock that drive the core logic and most peripherals. The clock source can be either Fast-clock or Slow-clock which can be set by registers.
- (5) **Instruction Cycle**= $F_{sys}/2$

FXT: Fast Crystal

SXT: Slow Crystal (32 KHz)

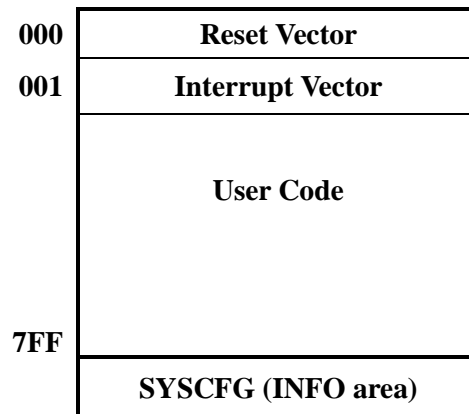
FIRC: Fast Internal RC oscillator

XRC: Fast or Slow External RC oscillator

SIRC: Slow Internal RC oscillator

1.2 Program ROM (PROM)

The MTP Program ROM of this device is 2K words, with an extra INFO area to store the SYSCFG. The ROM can be written multi-times and can be read as long as the PROTECT bit of SYSCFG is not set. The SYSCFG can be read no matter PROTECT is set or cleared, but can be written only when PROTECT is not set or ROM is erased. That is, unprotect the PROTECT bit needs the erased ROM.



1.3 Programming Counter (PC) and Stack

The Programming Counter is 11-bit wide capable of addressing a 2Kx14 MTP ROM. As a program instruction is executed, the PC will contain the address of the next program instruction to be executed. The PC value is normally increased by one except the followings. The Reset Vector (000h) and the Interrupt Vector (001h) are provided for PC initialization and Interrupt. For CALL/GOTO instructions, PC loads 11 bits address from instruction word. For RET/RETI/RETLW instructions, PC retrieves its content from the top level STACK. For the other instructions updating PC [7:0], the PC [10:8] keeps unchanged. The STACK is 11-bit wide and 6-level in depth. The CALL instruction and hardware interrupt will push STACK level in order. While the RET/RETI/RETLW instruction pops the STACK level in order.

For table lookup, the device offer the powerful table read instructions TABRL, TABRH to return the 14-bit ROM data into W by setting the DPTR= {DPH, DPL} F-Plane registers.

◇Example: To look up the PROM data located “TABLE” & “TABLE2”.

```

ORG      000H          ; Reset Vector
GOTO    START

START:
MOVLW   00H
MOVWF   INDEX          ; Set lookup table's address.

LOOP:
MOVFW   INDEX          ; Move index value to W register.
CALLTABLE          ; To lookup data, W=55H.
.....
INCF   INDEX, 1        ; Increment the index address for next address
.....
GOTO    LOOP          ; Go to LOOP label.
.....
MOVLW   (TABLE2>>8) &0xff
MOVWF   DPH            ; DPH register (F0F.2~0)
MOVLW   (TABLE2) &0xff
MOVWF   DPL            ; DPL register (F13.7~0)
TABRL           ; W=86H
TABRH           ; W=19H
.....

TABLE:
ADDWF   PCL, 1        ; Add the W with PCL, the result back in PCL.
RETLW   55H           ; W=55h when return
RETLW   56H           ; W=56H when return
RETLW   58H           ; W=58H when return
.....
ORG     768H

TABLE2:
.DT    0x1986, 0x3719, 0x2983... ; 14-bit ROM data

```

1.4 ALU and Working (W) Register

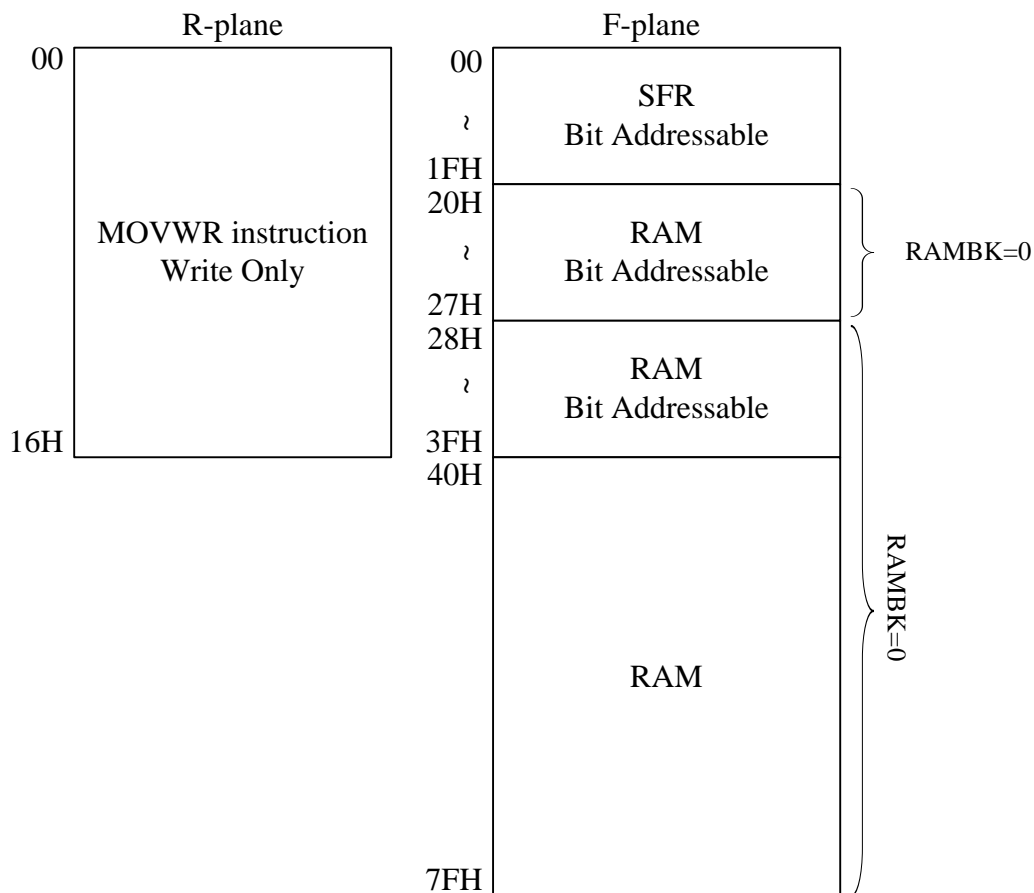
The ALU is 8-bit wide and capable of addition, subtraction, shift and logical operations. In two-operand instructions, typically one operand is the W register, which is an 8-bit non-addressable register used for ALU operations. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either W register or a file register. Depending on the instruction executed, the ALU may affect the values of Carry (C), Digit Carry (DC), and Zero (Z) Flags in the STATUS register. The C and DC flags operate as a/Borrow and /Digit Borrow, respectively, in subtraction.

Note: /Borrow represents inverted of Borrow register.

/Digit Borrow represents inverted of Digit Borrow register.

1.5 RAM Addressing Mode

There are two Data Memory Planes in CPU, R-Plane and F-Plane. The registers in R-Plane are write-only. The “MOVWR” instruction copies the W-register’s content to R-Plane registers by direct addressing mode. The lower locations of F-Plane are reserved for the SFR. Above the SFR is General Purpose Data Memory, implemented as static RAM. F-Plane can be addressed directly or indirectly. Indirect Addressing is made by INDF register. The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a pointer). The first half of F-Plane is bit-addressable, while the second half of F-Plane is not bit-addressable.



◇Example: Write immediate data into R-Plane register.

```
MOVLW    AAH           ; Move immediate AAH into W register.
MOVWR    05H           ; Move W value into R-Plane location 05H data register.
```

◇Example: Move the immediate data 55H to W register and F-Plane location 20H.

```
MOVLW    55H           ; Move immediate 55H into W register.
MOVWF    20H           ; To get a content of W and save in F-Plane location 20H.
```

◇Example: Move F-Plane location 20H data into W register.

```
MOVFW    20H           ; To get a content of F-Plane location 20H and save in W.
```

◇ Example: Indirectly addressing mode with FSR/INDF register. (F-Plane 04H/00H)

```
MOVLW    20H
MOVWF    FSR           ; Move immediate 20H into FSR register.
MOVLW    55H
MOVWF    INDF          ; Use data pointer FSR write a data into F-Plane location
                        ; 20H. 55H into F-plane 20H.
INCF     FSR, 1        ; Increment the index address for next address.
MOVFW    INDF          ; Use data pointer FSR read a data from F-Plane location
                        ; 21H. W data from F-Plane 21H
```

1.6 STATUS Register (F-Plane 03H)

This register contains the arithmetic status of ALU and the reset status. The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the STATUS register because these instructions do not affect those bits.

STATUS	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R	R	R/W	R/W	R/W
Bit	Description							
7	GB0: General Purpose Bit 0							
6	GB1: General Purpose Bit 1							
5	Reserved							
4	TO: Time Out Flag 0: after Power On Reset, LVR Reset, or CLRWDT/SLEEP instruction 1: WDT time out occurs							
3	PD: Power Down Flag 0: after Power On Reset, LVR Reset, or CLRWDT instruction 1: after SLEEP instruction							
2	Z: Zero Flag 0: the result of a logic operation is not zero 1: the result of a logic operation is zero							
1	DC: Decimal Carry Flag or Decimal /Borrow Flag							
	ADD instruction				SUB instruction			
	0: no carry 1: a carry from the low nibble bits of the result occurs				0: a borrow from the low nibble bits of the result occurs 1: no borrow			
0	C: Carry Flag or/Borrow Flag							
	ADD instruction				SUB instruction			
	0: no carry 1: a carry occurs from the MSB				0: a borrow occurs from the MSB 1: no borrow			

◇Example: Write immediate data into STATUS register.

```
MOVLW    00H
MOVWF    STATUS    ; Clear STATUS register.
```

◇Example: Bit addressing set and clear STATUS register.

```
BSF      STATUS, 0    ; Set C=1.
BSF      03H, 7      ; Set GB0=1
BCF      STATUS, 0    ; Clear C=0.
BCF      03H, 7      ; Clear GB0=0
```

◇Example: Determine the C flag by BTFSS instruction.

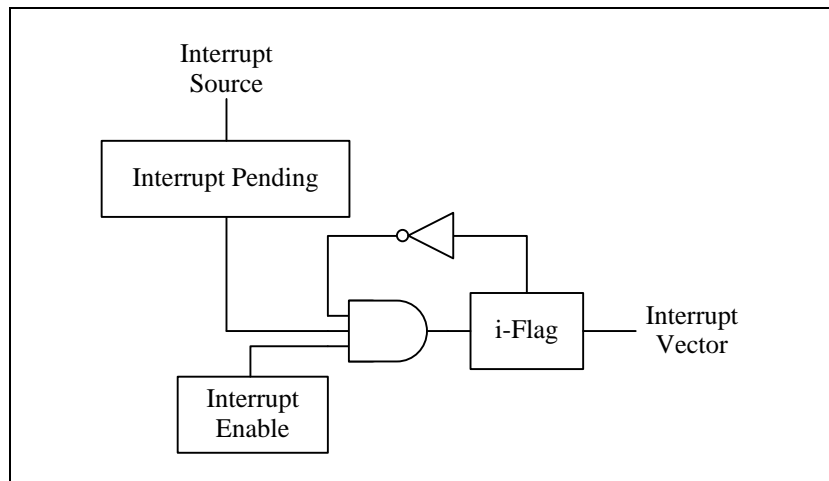
```
BTFSS    STATUS, 0    ; Check the carry flag
GOTO     LABEL_1     ; If C=0, goto label_1
GOTO     LABEL_2     ; If C=1, goto label_2
```

1.7 Interrupt

This device has 1 level, 1 vector and 7 interrupt sources. Each interrupt source has its own enable control bit. An interrupt event will set its individual pending flag; no matter its interrupt enable control bit is 0 or 1. Because device has only 1 vector, there is not an interrupt priority register. The interrupt priority is determined by F/W.

If the corresponding interrupt enable bit has been set (INTIE), it would trigger CPU to service the interrupt. CPU accepts interrupt in the end of current executed instruction cycle. In the mean while, a “CALL 001” instruction is inserted to CPU, and i-flag is set to prevent recursive interrupt nesting.

The i-flag is cleared in the instruction after the “RETI” instruction. That is, at least one instruction in main program is executed before service the pending interrupt. The interrupt event is level triggered. F/W must clear the interrupt event register while serving the interrupt routine.



◇Example: Setup INT1 (PA1) interrupt request and rising edge trigger.

```

ORG      000H          ; Reset vector.
GOTO     START        ; Goto user program address.

ORG      01H          ; All interrupt vector.
GOTO     INT_SUBROUTINE ; If INT1 (PA1) input occurred rising edge.

ORG      02H

                                START:
MOV LW   1111101B
MOV WR   PAPUN          ; Enable INT1 (PA1) input pull up resistor.
MOV LW   00010000B
MOV WR   R0B           ; Set INT1 interrupt trigger as rising edge.
MOV LW   1111101B
MOV WF   INT1IF        ; Clear INT1 interrupt request flag
MOV LW   00000010B
MOV WR   INTIE         ; Enable INT1 interrupt.

MAIN:
...
GOTO     MAIN

INT_SUBROUTINE:
MOV WF   GPR0          ; Push routine to Save W and STATUS data to buffers.
MOV WF   STATUS        ; F-Plane 03H
MOV WF   GPR1

BTFSS   INT1IF        ; Check INT1IF bit.
GOTO    EXIT_INT      ; INT1IF=0, exit interrupt vector.
...
MOV LW   1111101B
MOV WF   INTIF        ; Clear INT1 interrupt request flag
GOTO    EXIT_INT

EXIT_INT:
MOV FW   GPR1          ; POP Routine W and STATUS data from buffers.
MOV WF   STATUS
MOV FW   GPR0
RETI

```

2. Chip Operation Mode

2.1 Reset (000H)

This device can be RESET in four ways.

- Power-On-Reset
- Low Voltage Reset (LVR)
- External Pin Reset (PA7)
- Watchdog Reset (WDT)

After Power-On-Reset, all system and peripheral control registers are then set to their default hardware Reset values. The clock source, LVR level and chip operation mode are selected by the SYSCFG register value.

The Low Voltage Reset features static reset when supply voltage is below a threshold level. There are three threshold levels can be selected. The LVR's operation mode is defined by the SYSCFG register. See the following LVR Selection Table; user must also consider the lowest operating voltage of operating frequency.

Slow-clock needs to be turned on when using LVR.

LVR Selection Table:

LVR level
LVR2.9
LVR2.3
LVR2.0

Different Fsys have different system minimum operating voltage, reference to Operating Voltage of DC characteristics, if current system voltage is lower than minimum operating voltage and the lower LVR is selected, then the system maybe enter dead-band and error occur.

The External Pin Reset and Watchdog Reset can be disabled or enabled by the SYSCFG register. These two resets also set all the control registers to their default reset value. The TO/PD flags are not affected by these resets.

◇ Example: Defining Reset Vector

```

ORG      000H
GOTO     START      ; Jump to user program address.

ORG      010H

START:
...      ; 010H, The head of user program
...
GOTO     START
    
```

2.2 System Configuration Register (SYSCFG)

The System Configuration Register (SYSCFG) is located at Info ROM address 0001. The SYSCFG determines the option for initial condition of MCU. It is written by PROM Writer only. User can select clock source, LVR threshold voltage and chip operation mode by SYSCFG register. The default value of SYSCFG is 3FFFh. The 13th bit of SYSCFG is code protection selection bit. If this bit is 1, the data in PROM will be protected, when user reads PROM.

Bit	13~0	
Default Value	111111111111	
Bit	Description	
13	PROTECT: Code protection selection	
	1	Enable Code protection.
	0	Disable Code protection.
12	PWRSV: Power Saving Mode (affect power consumption for STOP/IDLE mode)	
	1	Enable Power Saving Mode. LVR2.3V/2.9V disable in IDLE mode.
	0	Disable Power Saving Mode.
11-10	LVR: Low Voltage Reset Mode	
	11	LVR2.0V
	10	LVR2.0V, disabled in STOP/IDLE mode. (if MODE3V =1, IDE tool will force LVR=2'b10)
	01	LVR2.3V
	00	LVR2.9V
9	PD30IOE: PD[3:0] I/O Mode Enable	
	1	PD [3:0] as I/O mode
	0	PD [3:0] as LCD mode (PDE [3:0] will be invalid)
8	INT0EDGE: INT0 (PA6) trigger edge (Notice: EV2781C only support falling edge emulation)	
	1	Rising edge
	0	Falling edge
7	XRSTE: External Pin (PA7) Reset Enable	
	1	Enable
	0	Disable (i.e.: PA7 as input pin)
6	WDTE: WDT Reset Enable	
	1	Enable
	0	Disable
5	MODE3V: Operating Voltage Selection	
	1	Set CPUCLK default is Slow-CLK and force LVR2.3V/2.9V disable.
	0	Set CPUCLK default is Fast-CLK.
4-0	Tenx Reserved	

SYSCFG setting & power consumption relationship:
If R-plane register 16h \neq 0x37

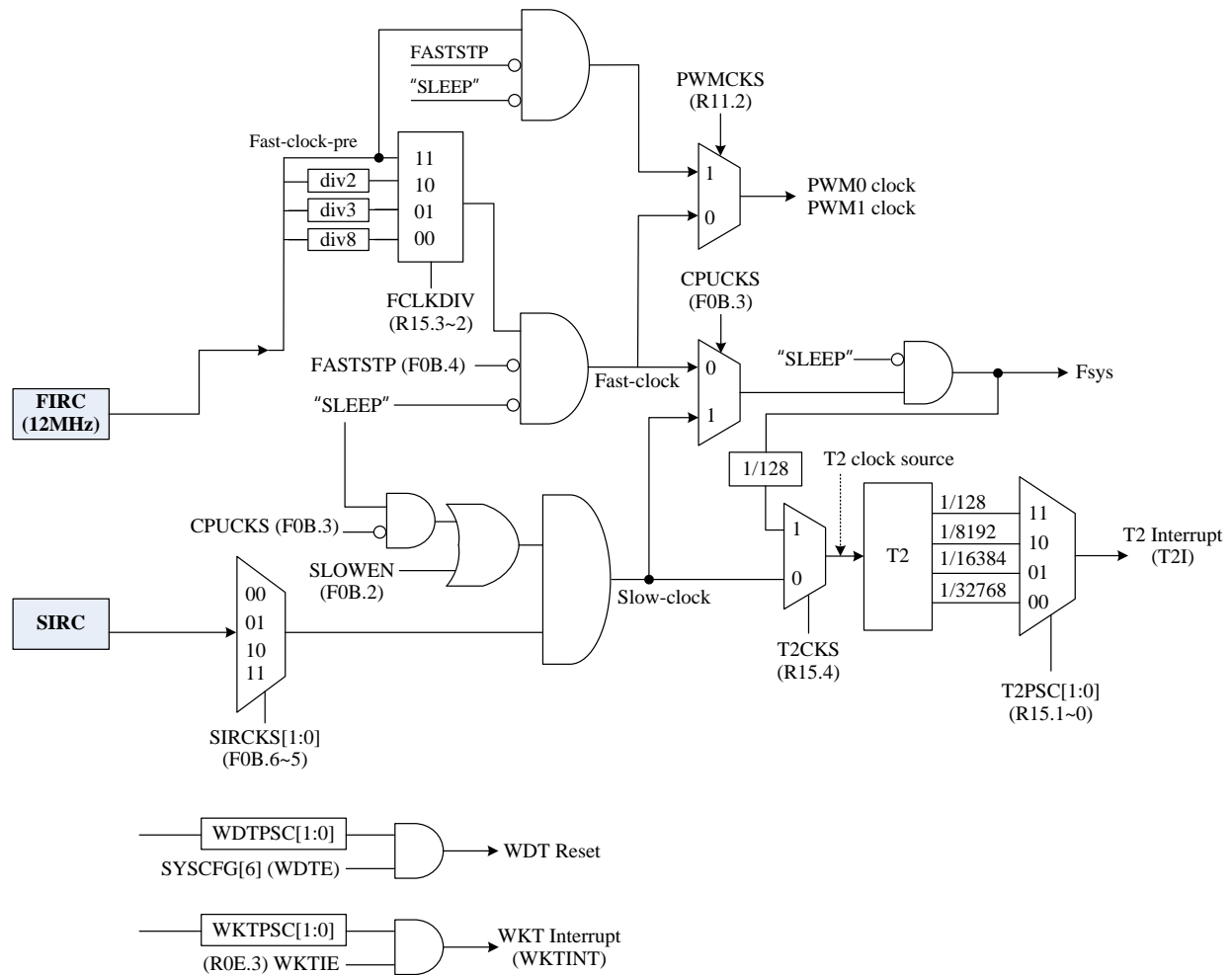
MODE3V (SYSCFG.5)	PWRSVAV (SYSCFG.12)	LVR[1:0] (SYSCFG 11~10)	FAST/SLOW mode	STOP/IDLE mode
0	0	11	LVR2.0V	LVR2.0V
0	0	10	LVR2.0V	All LVR disabled
0	0	01	LVR2.3V	LVR2.3V
0	0	00	LVR2.9V	LVR2.9V
0	1	11	LVR2.0V	LVR2.0V
0	1	10	LVR2.0V	All LVR disabled
0	1	01	LVR2.3V	LVR2.0V
0	1	00	LVR2.9V	LVR2.0V
1	0	11	LVR2.0V	LVR2.0V
1	0	10	LVR2.0V	All LVR disabled
1	0	01	LVR2.0V	LVR2.0V
1	0	00	LVR2.0V	LVR2.0V
1	1	11	LVR2.0V	LVR2.0V
1	1	10	LVR2.0V	All LVR disabled
1	1	01	LVR2.0V	LVR2.0V
1	1	00	LVR2.0V	LVR2.0V

If R-plane register 16h = 0x37 (Disable LVR2.0V)

MODE3V (SYSCFG.5)	PWRSVAV (SYSCFG.12)	LVR[1:0] (SYSCFG 11~10)	FAST/SLOW mode	STOP/IDLE mode
0	0	11	All LVR disabled	All LVR disabled
0	0	10	All LVR disabled	All LVR disabled
0	0	01	LVR2.3V	LVR2.3V
0	0	00	LVR2.9V	LVR2.9V
0	1	11	All LVR disabled	All LVR disabled
0	1	10	All LVR disabled	All LVR disabled
0	1	01	All LVR2.3V	All LVR disabled
0	1	00	All LVR2.9V	All LVR disabled
1	0	11	All LVR disabled	All LVR disabled
1	0	10	All LVR disabled	All LVR disabled
1	0	01	All LVR disabled	All LVR disabled
1	0	00	All LVR disabled	All LVR disabled
1	1	11	All LVR disabled	All LVR disabled
1	1	10	All LVR disabled	All LVR disabled
1	1	01	All LVR disabled	All LVR disabled
1	1	00	All LVR disabled	All LVR disabled

2.3 Dual System Clock

The device is designed with dual-clock system. There are two kinds of clock source, i.e. SIRC (Slow Internal RC) and FIRC (Fast Internal RC). Each clock source can be applied to CPU kernel as system clock. When in IDLE mode, only Slow-clock can be configured to keep oscillating to provide clock source to T2 block. Refer to the figure below.



Clock Scheme Block Diagram

FAST Mode:

After power on or reset, if $\text{MODE3V}(\text{SYSCFG.5})=0$, device enters FAST mode, otherwise enters SLOW mode. User can set $\text{CPUCKS}=1$ to enter SLOW mode. Besides, firmware can also enable or disable the Slow-clock for the T2 system operating.

In this mode, the program is executed using Fast-clock as CPU clock (F_{sys}). The Timer0, Timer1 blocks are also driven by Fast-clock, The PWM0, and PWM1 block can driven by Fast-clock or Fast-clock-pre. T2 can also be driven by Fast-clock by setting $\text{T2CKS}=1$ and $\text{CPUCKS}=0$.

SLOW Mode:

After power-on or reset, if $\text{MODE3V}=1$, device enters SLOW mode. In this mode, the Fast-clock can stopped (by $\text{FASTSTP}=1$, for power saving) or running (by $\text{FASTSTP}=0$), and Slow-clock is enabled.

IDLE Mode:

If Slow-clock is enabled and $\text{T2CKS}=0$ before executing the SLEEP instruction, the CPU enters the IDLE mode. In this mode, the Slow-clock will continue running to provide clock to T2 block. CPU stop fetching code and all blocks are stop except T2 related circuits.

Another way to keep clock oscillation in IDLE mode is setting $\text{WKTIE}=1$ before executing the SLEEP instruction. In such condition, the WKT keeps working and wake up CPU periodically.

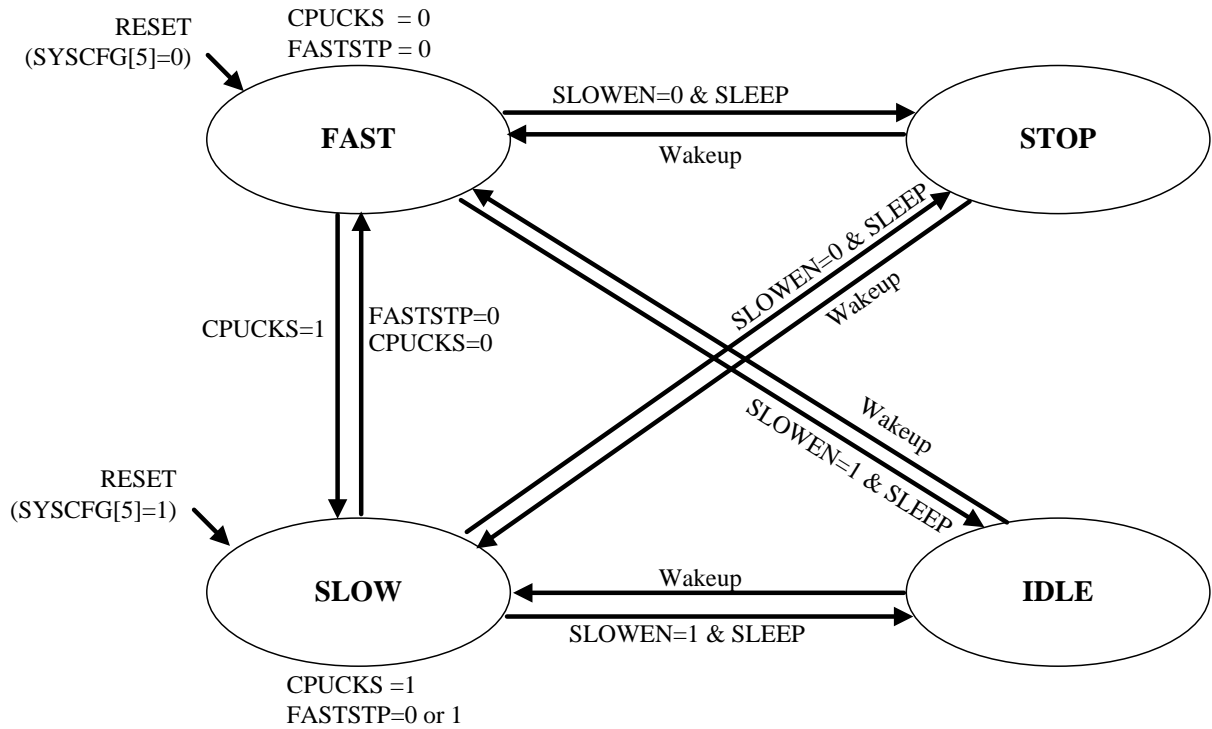
T2 and WKT/WDT are independent and have their own control registers. It is possible to keep both T2 and WKT working and wake-up in the IDLE mode.

STOP Mode:

If Slow-clock and WKT/WDT are disabled before executing the SLEEP instruction, every block is turned off and the device enters the STOP mode. STOP mode is similar to IDLE mode. The difference is all clock oscillators either Fast-clock or Slow-clock is power down and no clock is generated.

2.4 Dual System Clock Modes Transition

The device is operated in one of four modes: FAST mode, SLOW mode, IDLE mode, and STOP mode.



- Note:
- SLEEP denotes SLEEP instruction
 - Wakeup denotes wake-up events, such as External pin interrupt, WKT interrupt or T2 Interrupt.

CPU Operation Block Diagram

CPU Mode & Clock Functions Table:

Mode	Oscillator	Fsys	Fast-clock	Slow-clock	TM0/TM1	T2	Wakeup event
FAST	FIRC	Fast-clock	Run	Set by SLOWEN bit	Run	Run	-
SLOW	SIRC	Slow-clock	Set by FASTSTP bit	Run	Run	Run	-
IDLE	SIRC	Stop	Stop	Run	Stop	Run	WKT/IO/T2
STOP	Stop	Stop	Stop	Stop	Stop	Stop	IO

● **FAST mode switches to SLOW mode**

The following steps are suggested to be executed by order when FAST mode switches to SLOW mode:

- (1) Enable Slow-clock (SLOWEN=1)
- (2) Switch to Slow-clock (CPUCKS=1)
- (3) Stop Fast-clock (FASTSTP=1)

Note: Stop Fast-clock (FASTSTP=1) is optional. Stop Fast-clock can reduce power consumption.

◇ Example: Switch FAST mode to SLOW mode.

```

MOVLW    01100000B    ;
MOVWF    CLKS         ; Slow clock prescaler selection(2KHz).
BSF      SLOWEN       ; Enable Slow-clock.
BSF      CPUCKS       ; Fsys=Slow-clock.
BSF      FASTSTP      ; Disable Fast-clock.

```

● **SLOW mode switches to FAST mode**

SLOW mode can be enabled by SLOWEN bit and CPUCKS bit in F0B register of F-plane. The following steps are suggested to be executed by order when SLOW mode switches to FAST mode:

- (1) Enable Fast-clock (FASTSTP=0)
- (2) Switch to Fast-clock (CPUCKS=0)
- (3) Stop Slow-clock (SLOWEN=0)

Note: Stop Slow-clock (SLOWEN=0) is optional. Slow-clock can keep oscillating to provide T2 counter block in FAST mode.

◇ Example: Switch SLOW mode to FAST mode (The Fast-clock stop).

```

MOVLW    00001000B
MOVWR    MR15         ; Fast clock prescaler selection.
BCF      FASTSTP      ; Enable Fast-clock.
BCF      CPUCKS       ; Fsys = Fast-clock
BCF      SLOWEN       ; Disable Slow-clock

```

● **IDLE mode Setting**

The IDLE mode can be configured by following setting in order:

- (1) Enable Slow-clock (SLOWEN=1) or WKT(WKTIE=1)
- (2) Switch T2 clock source to Slow-clock (T2CKS=0)
- (3) Execute SLEEP instruction

IDLE mode can be woken up by External interrupt, WKT interrupt and T2 interrupt.

◇ Example: Switch FAST/SLOW mode to IDLE mode.


```

BSF      SLOWEN      ; Enable Slow-clock.
MOVLW   00000101B
MOVWR   MR15        ; T2 clock source = slow clock. T2 prescaler = div 16384
SLEEP                                ; Enter IDLE mode.

```

● **STOP Mode Setting**

The STOP mode can be configured by following setting in order:

- (1) Stop Slow-clock (SLOWEN=0)
- (2) Stop WKT/WDT (WKTIE=0, WDTSTP=1)
- (3) Execute SLEEP instruction

STOP mode can be woken up only by External pin interrupt.

◇ Example: Switch FAST/SLOW mode to STOP mode.

```

BCF      SLOWEN      ; Disable Slow-clock.
MOVLW   00000000B   ;
MOVWR   INTIE       ;Disable WKT counting
MOVLW   01100100B   ; Stop WDT counting in STOP mode
MOVWR   MR15
SLEEP                                ; Enter STOP mode.

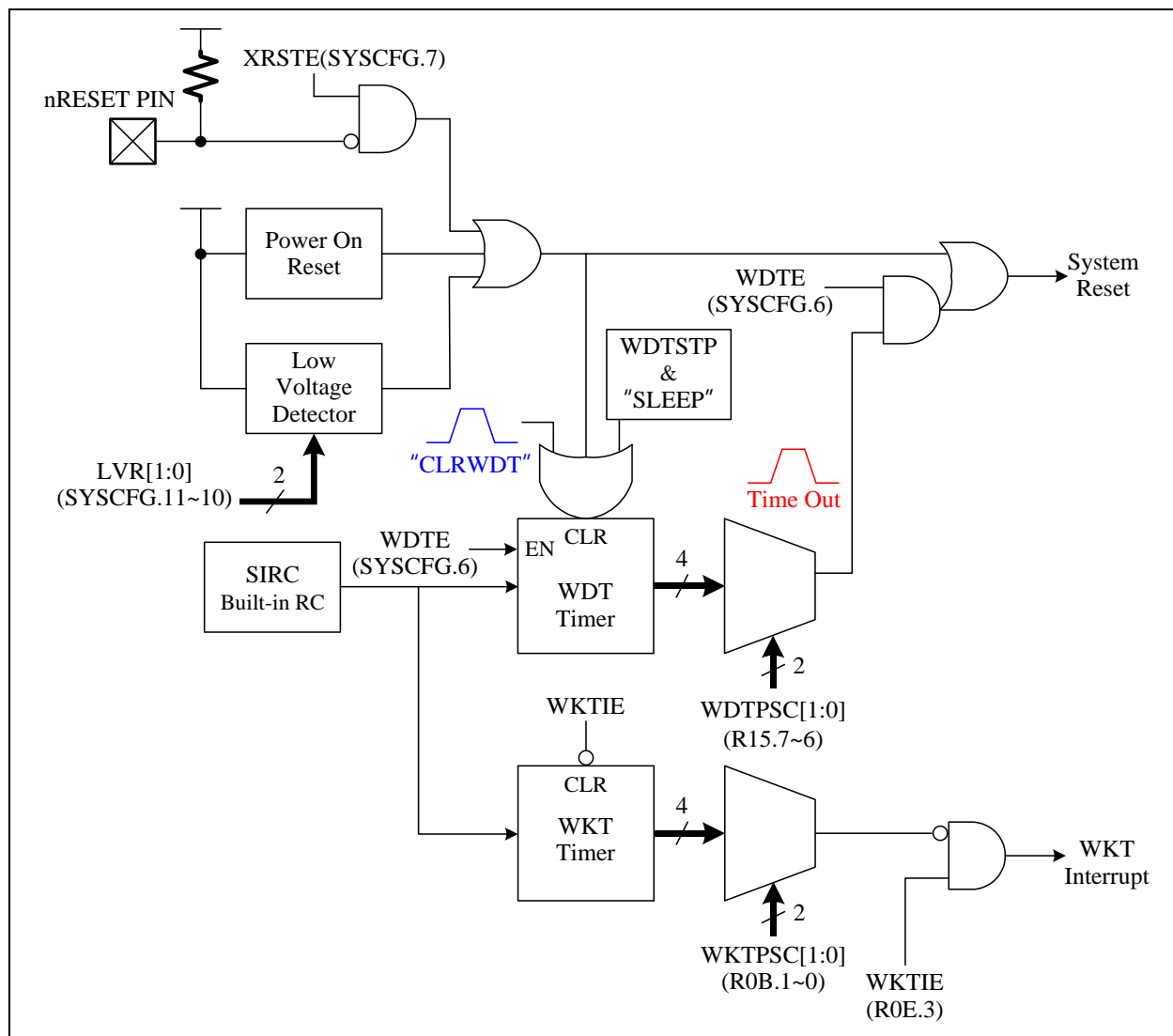
```

3. Peripheral Functional Block

3.1 Watchdog (WDT) /Wakeup (WKT) Timer

The WDT and WKT share the same built-in internal RC Oscillator and have individual own counters. The overflow period of WDT, WKT can be selected by individual prescaler (WDTPSC[1:0], WKTPSC[1:0]). The WDT timer is cleared by the CLRWDT instruction. If the Watchdog is enabled (SYSCFG[7]=WDTE=1), the WDT generates the chip reset signal. Set WDTSTP (R15.5) to '1' can let WDT timer stop counting after executing SLEEP instruction. If WDTSTP = 0, even if the SLEEP instruction is executed, the WDT timer will always keep counting.

The WKT timer is an interval timer, WKT time out will generate WKT Interrupt Flag (WKTIF). The WKT timer is cleared/stopped by WKTIE=0. Set WKTIE=1, the WKT timer will always count regardless at any CPU operating mode.



WDT/WKT Block Diagram

Watchdog clear is controlled by CLRWDT instruction and moving any value into WDTCLR is to clear watchdog timer.

◇ Example: Clear watchdog timer by CLRWDT instruction.

```

MAIN:
...                               ; Execute program.
CLRWDT                            ; Execute CLRWDT instruction.
...
GOTO      MAIN

```

◇ Example: Clear watchdog timer by write WDTCLR register.

```

MAIN:
...                               ; Execute program.
MOVWF    WDTCLR                   ; Write any value into WDTCLR register.
...
GOTO      MAIN

```

◇ Example: Set WDT time and disable after executing SLEEP instruction.

```

MOVLW    00100100B
MOVWR    MR15                     ; Set WDT period.
                                           ; Set WDT disable in IDLE/STOP mode.
SLEEP

```

◇ Example: Set WKT period and interrupt function.

```

MOVLW    000000010B
MOVWR    MR0B                     ; Select WKT period=60 ms @3V (default 120 ms).

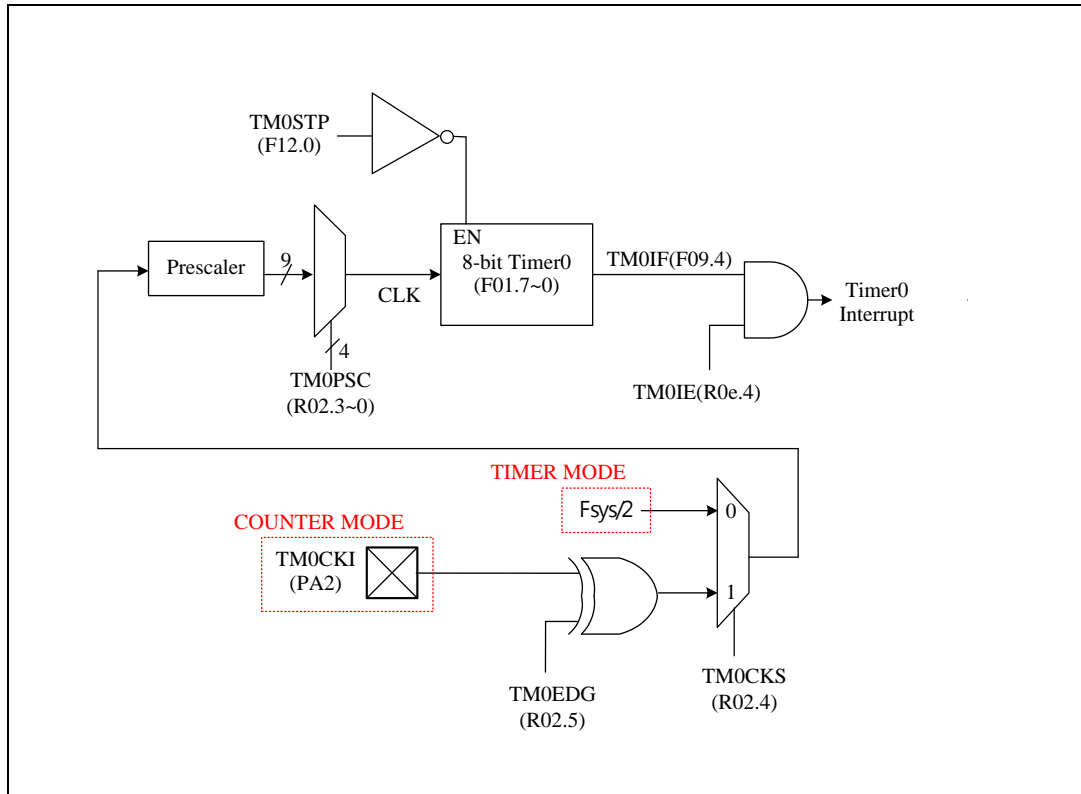
MOVLW    11110111B               ; Clear WKT interrupt flag by using byte operation.
MOVWF    INTIF                   ; Don't use bit operation "BCF WKTIF" clear interrupt flag

MOVLW    00001000B               ; Enable WKT interrupt function
MOVWR    MR0E

```

3.2 Timer0

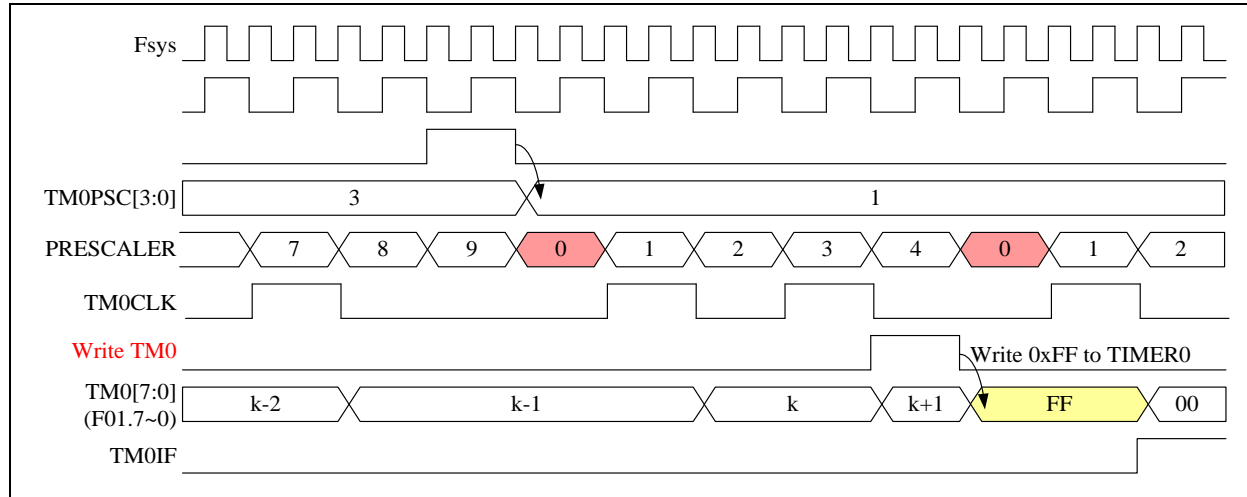
The Timer0 is an 8-bit wide register of F-Plane 01h (TM0). Timer0 increases itself periodically and automatically rolls over based on the prescaler clock source, which can be $F_{sys}/2$ or TM0CKI (PA2) rising/falling input. The Timer0 increase rate is determined by Timer0 prescaler (TM0PSC) register in R-Plane. The Timer0 always generates TM0IF when its count rolls over, it will generate Timer0 interrupt if (TM0IE) is set. Set the TM0STP bit will stop Timer0 counting.



Timer0 Block Diagram

The following timing diagram describes the Timer0 works in pure Timer mode.

When the Timer0 prescaler (TM0PSC) is written, the internal 8-bit prescaler will be cleared to 0 to make the counting period correct at the first Timer0 count. TM0CLK is the internal signal that causes the Timer0 to increase by 1 at the end of TM0CLK. TM0WR is also the internal signal that indicates the Timer0 is directly written by instruction; meanwhile, the internal 8-bit prescaler will be cleared. When Timer0 counts from FFh to 00h, TM0IF (Timer0 Interrupt Flag) will be set to 1 and generate interrupt if TM0IE (Timer0 Interrupt Enable) is set.



Timer0 works in Timer mode (TM0CKS=0)

The equation of TM0 interrupt time value is as following:

$$\text{TM0 interrupt frequency} = (\text{Fsys}/2)/\text{TM0PSC}/(256-\text{TM0})$$

◇Example: Setup TM0 work in Timer mode

```

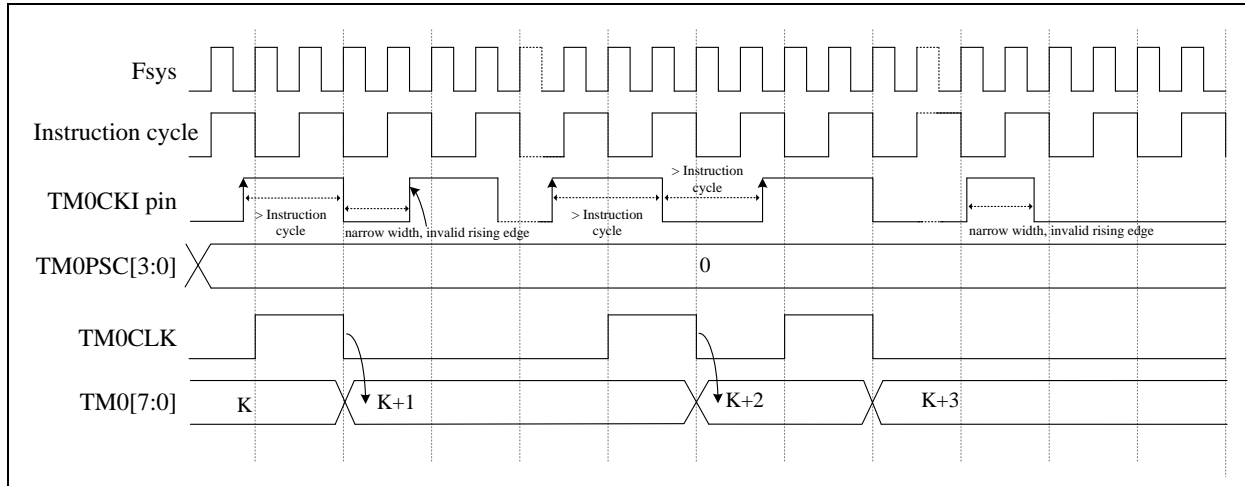
; Setup TM0 clock source and divider
    MOVLW    00000101B    ; R02.4=0, Setup TM0 clock = Fsys/2
    MOVWR    R02          ; R02.3~0=5 (TM0PSC)
                          ; TM0 clock prescaler = Fsys/64

; Set TM0 timer.
    BSF      TM0STP       ; Disable TM0 counting (Default "0").
    MOVLW    156
    MOVWF    TM0          ; Write 156 into TM0 register of F-Plane.(F01)

; Enable TM0 timer and interrupt function.
    MOVLW    11101111B    ; Clear TM0 request interrupt flag by byte operation
    MOVWF    INTIF        ; F-Plane 09H
    MOVLW    00010000B    ; Enable TM0 interrupt function
    MOVWR    INTIE        ; ROE
    BCF      TM0STP       ; Enable TM0 counting (Default "0").
    
```

The following timing diagram describes the Timer0 works in Counter mode.

If TM0CKS=1 then Timer0 counter source clock is from TM0CKI pin. TM0CKI signal is synchronized by instruction cycle that means the high/low time durations of TM0CKI must be longer than one instruction cycle time to guarantee each TM0CKI's change will be detected correctly by the synchronizer.



Timer0 works in Counter mode for TM0CKI (TM0EDG=0), TM0CKS=1

◇ Example: Setup TM0 work in Counter mode and clock source from TM0CKI pin (PA2)

; Setup TM0 clock source from TM0CKI pin (PA2) and divider.

```

MOVLW    00110000B
MOVWR    R02                ; R02.5=1, Select TM0 prescaler counting edge=falling
                                edge.
                                ; R02.4=1, Setup TM0 clock=TM0CKI pin(PA2)
                                ; R02.3~0=0 (TM0PSC)
                                ; TM0 clock prescaler=Fsys/2

```

; Set TM0 timer and stop TM0 counting.

```

BSF      TM0STP            ; Disable TM0 counting.
MOVLW    00H
MOVWF    TM0              ; Write 0 into TM0 register of F-Plane.

```

; Start TM0 count and read TM0 counter.

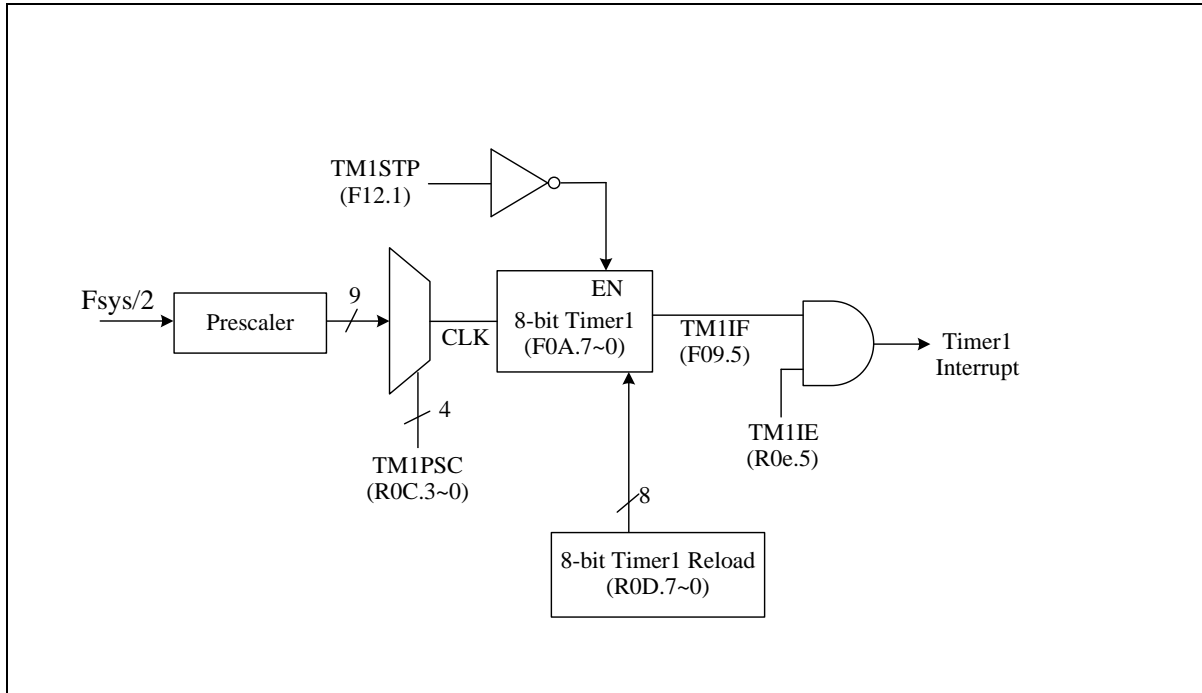
```

BCF      TM0STP            ; Enable TM0 counting.
NOP
NOP
NOP
BSF      TM0STP            ; Disable TM0 counting
MOVWF    TM0

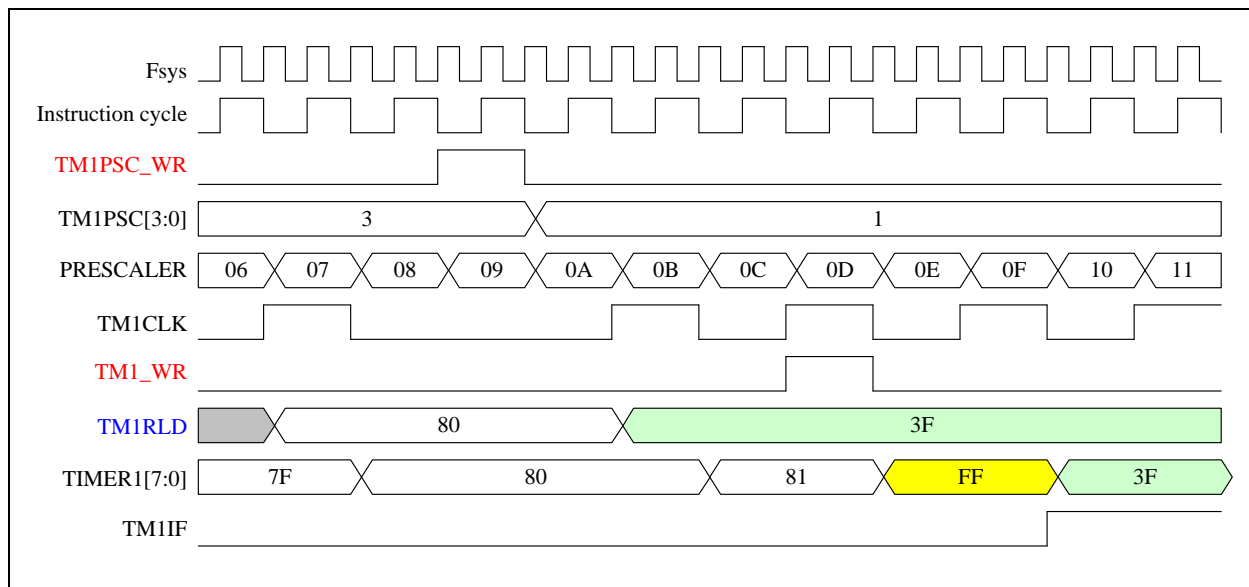
```

3.3 Timer1

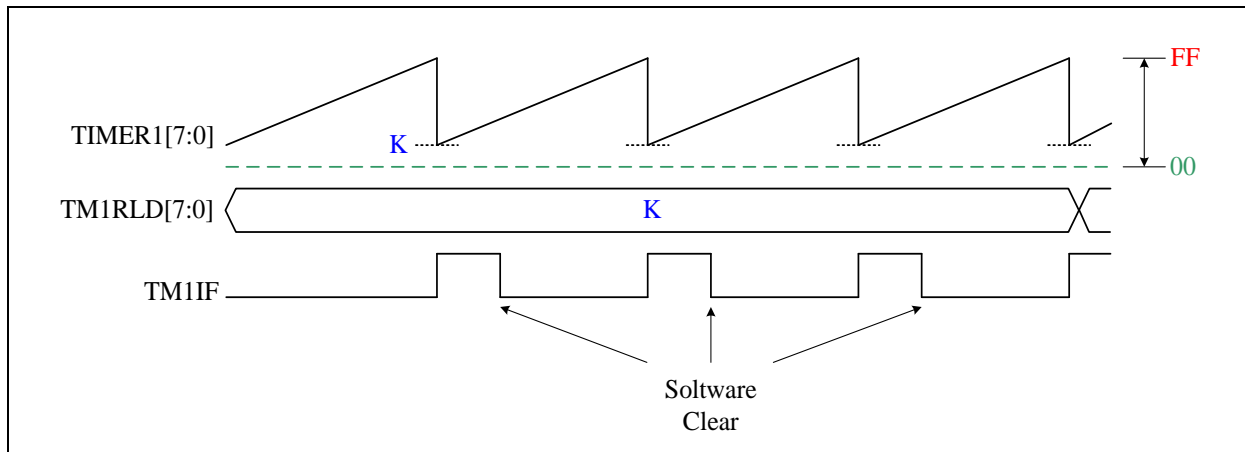
The Timer1 is an 8-bit wide register of F-Plane. Timer1 increases itself periodically and automatically reloads a new "offset value" (TM1RLD) while it rolls over based on the prescaler instruction clock. The Timer1 increase rate is determined by TM1PSC register in R-Plane. Set the TM1STP bit will stop Timer1 counting. TM1OUT is an output signal that toggles when Timer1 overflow.



Timer1 Block Diagram



Timer1 Timing Diagram


Timer1 Reload Diagram

◇Example: Setup TM0 work in Timer mode and counting overflow toggle out to TM1OUT (PD0) configuration.

; Setup TM1 clock source, divider and enable TM1OUT

```

MOV LW    00000101B
MOV WR    MR0C           ; R0C.3~0=5 (TM1PSC), Select TM1 clock=Fsys/64.
MOV LW    00000100B
MOV WR    MR0B           ; R0B.2=1, Enable TM1OUT function pin (PD0).
    
```

; Set TM1 timer offset and stops TM1 counting

```

BSF       TM1STP         ; Stop TM1 counting
MOV LW    F0H
MOV WF    TM1            ; Write F0H into TM1 counter
    
```

; Enable TM1 timer and interrupt function.

```

MOV LW    11011111B     ; Clear TM1 request interrupt flag by byte operation
MOV WF    INTIF         ; F-Plane 09H
    
```

```

MOV LW    00100000B     ; Enable TM1 interrupt function.
MOV WR    INTIE         ;
    
```

```

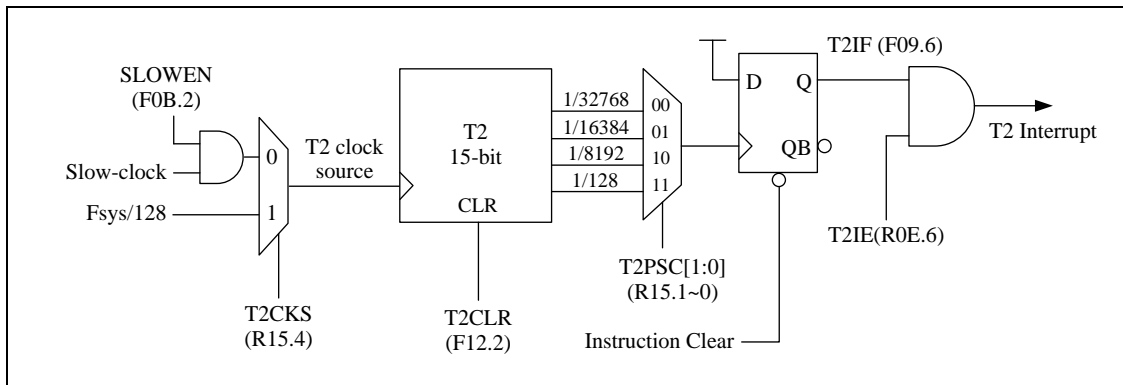
BCF       TM1STP         ; Enable TM1 counting
    
```

Example:

$F_{sys}=4 \text{ MHz}$, $TM1PSC=1$, $TM1 \text{ clock source}=F_{sys}/4=1 \text{ MHz}$
 $TM1RLD=0xF0$,
 $TM1 \text{ interrupt time}=(1/1 \text{ MHz}) * (0xFF - 0xF0) = 1 \text{ us} * 16 = 16 \text{ us}$
 $TM1OUT \text{ output time period}=16 \text{ us} * 2 = 32 \text{ us}$.
 $TM1OUT \text{ output frequency}=1/32 \text{ us}=31.250 \text{ KHz}$.

3.4 T2:15-bit Timer

The T2 is a 15-bit counter and the clock sources are from either $F_{sys}/128$ or Slow-clock. It is used to generate time base interrupt and T2 counter block clock. The T2 content cannot be read by instructions. It generates interrupt flag T2IF (F09.6) with the clock divided by 32768/16384/8192/128 depends on T2PSC[1:0] (R15.1~0) register bits. The following figure shows the block diagram of T2.



T2 Block Diagram

Example:

[CPU running at FAST mode, F_{sys} =Fast-clock=FIRC 6 MHz]

◇Example:

```

; Setup T2 clock source and divider.
MOVLW    xxx11001B    ; R15.4 (T2CKS) =1, T2 clock source=Fsys/128
MOVWR    MR15         ; R15.3~2 (FCLKDIV) =2,
                    ; Fsys=Fast-clock=Fast-clock-pre/2
                    ; Fsys=Fast-clock=12 MHz/2=6 MHz
                    ; R15.1~0 (T2PSC) =1, Divided by 16384
BSF      T2CLR        ; F12.2 (T2CLR), Stop T2 counting.

; Enable T2 timer and interrupt function.
MOVLW    10111111B    ; Clear T2 request interrupt flag by byte operation
MOVWF    INTIF        ; F-Plane 09H

MOVLW    01000000B    ;
MOVWR    INTIE        ; Enable T2 interrupt function.

BCF      T2CLR        ; Enable T2 counting.
    
```

T2 clock source is $F_{sys}/128=6\text{ MHz}/128=46875\text{ Hz}$, $T2PSC=1/16384$

T2 frequency= $46875\text{ Hz}/16384=2.86\text{ Hz}$

Example:

[CPU running at SLOW mode, Fsys=Slow-clock=32768 Hz]

◇Example:

; Setup T2 clock source and divider

```
MOVLW    xxx0xx00B    ; R15.4 (T2CKS) =0, T2 clock source=Slow-clock
MOVWR    MR15         ; Fsys=Slow-clock=32768 Hz
                        ; R15.1~0 (T2PSC) =0, Divided by 32768
```

```
BSF      T2CLR        ; Stop T2 counting.
```

; Enable T2 timer and interrupt function.

```
MOVLW    10111111B    ; Clear T2 request interrupt flag
MOVWF    INTIF        ; F-Plane 09H
```

```
MOVLW    01000000B    ; Enable T2 interrupt function.
MOVWR    INTIE        ; R0E
```

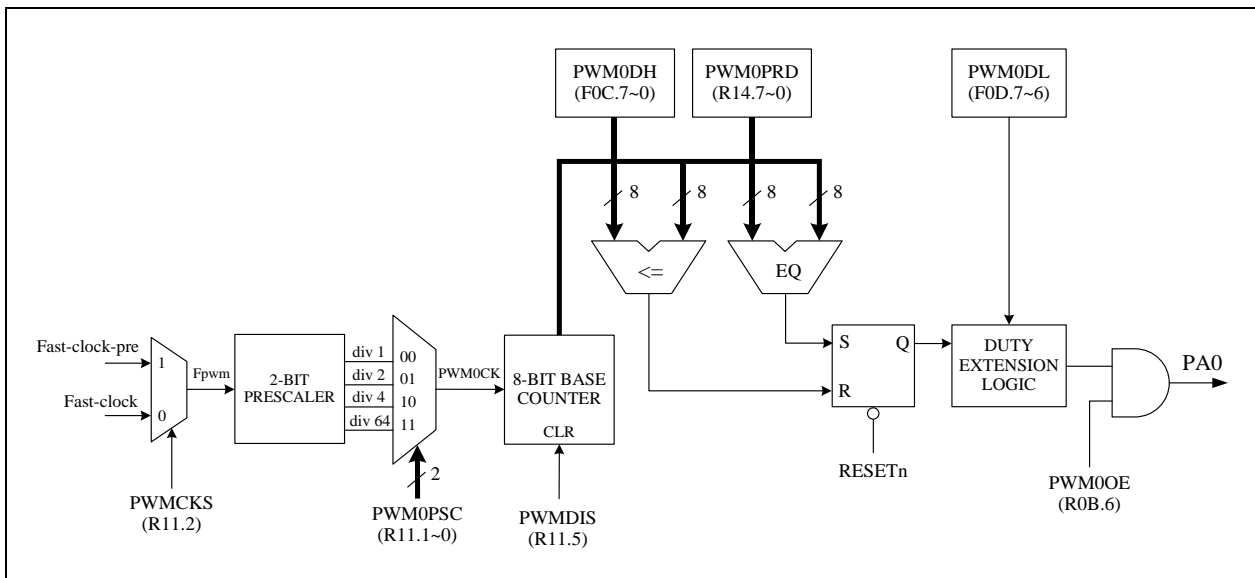
```
BCF     T2CLR        ; Enable T2 counting.
```

T2 clock source is Slow-clock=32768 Hz, T2PSC=/32768,
T2 frequency=32768 Hz/32768=1 Hz

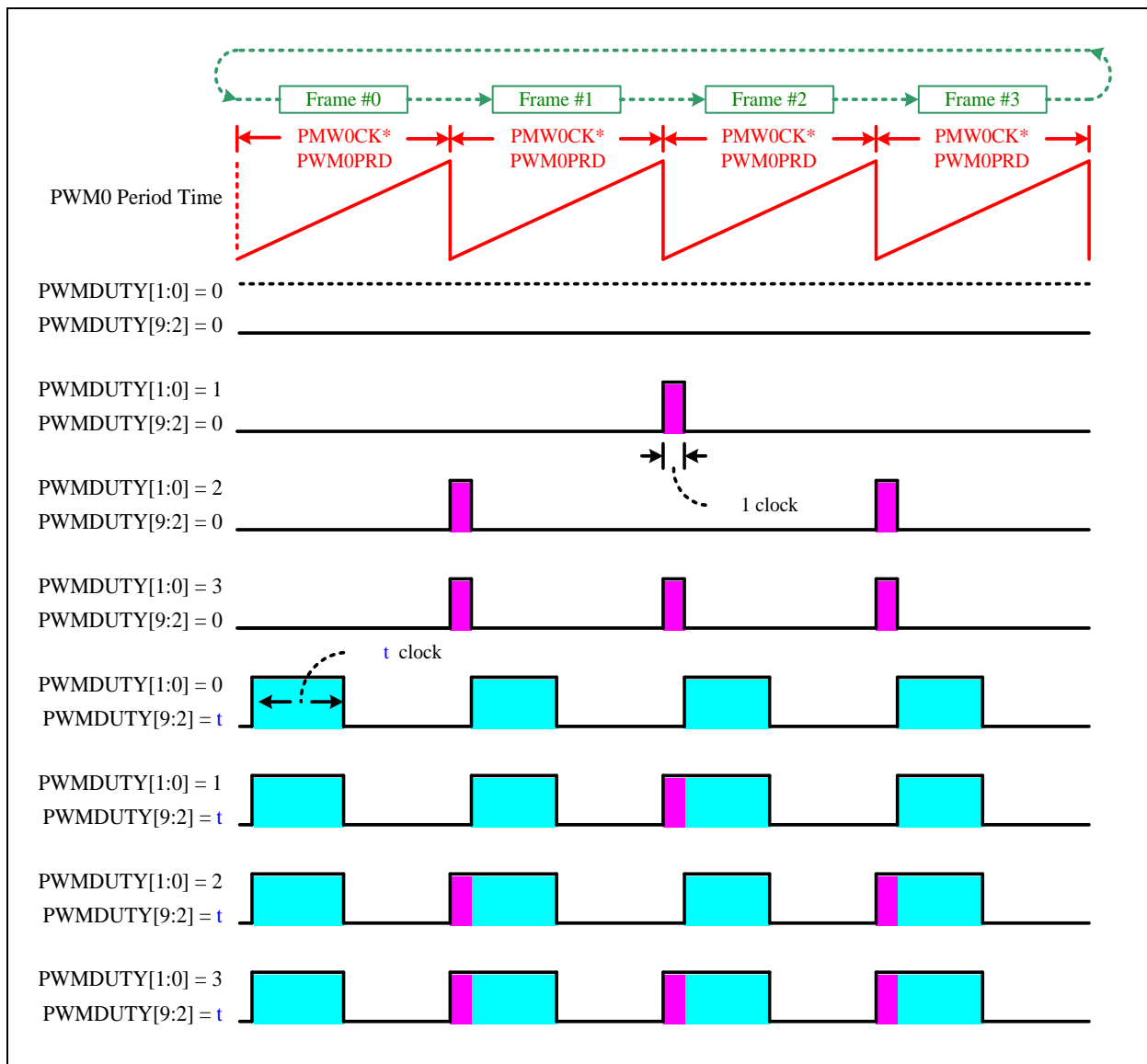
3.5 PWM0: (8+2) bits PWM

The PWM can generate waveform with 1024 duty resolution based on F_{PWM} clock, the F_{PWM} can select Fast-clock or Fast-clock-pre by PWMCKS (R11.2). A spread LSB technique allows PWM to run its frequency at “System Clock divided by 256” instead of “System Clock divided by 1024”, which means the PWM is 4 times faster than normal. The advantage of higher PWM frequency is that the post RC filter can transform the PWM signal to more stable DC voltage level. The PWM output signal reset to low level whenever the 8-bit base counter matches the 8-bit MSB of PWM duty register PWM0DH (F0C.7~0). When the base counter rolls over, the 2-bit LSB of PWM duty register PWM0DL (F0D.7~6) decides whether to set the PWM output signal high immediately or set it high after one clock cycle delay.

The PWM0 period can be set by writing period value to PWM0PRD register (R14). Note that changing the PWM0PRD is immediately changing the PWM0PRD values, which are different from PWM0DH /PWM0DL which has buffer to update the duty at the end of current period. The Programmer must pay attention to the current time to change PWM0PRD by observing the following figure. There is a digital comparator that compares the PWM0 counter and PWM0PRD, if PWM0 counter is larger than PWM0PRD after setting the PWM0PRD, a fault long PWM cycle will be generated because PWM0 counter must count to overflow then keep counting PWM0PRD to finish the cycle.



PWM0 Block Diagram



PWM0 8+2 Timing Diagram

Example:

; Setup PWM0 clock source and prescaler.

```
MOVLW    00000101B    ; R11.5 (PWMDIS)= 0, PWM0/PWM1 clock enable
MOVWR    MR11          ; R11.2 (PWMCKS)= 1, FPWM=Fast-clock-pre(12 MHz)
                                ; R11.1~0 (PWM0PSC) =1,
                                ; PWM clock=FPWM/2=6 MHz

MOVLW    80H
MOVWR    PWM0PRD      ; Set PWM0 period [7:0] =80H.

MOVLW    00H
MOVWF    PWM0DL      ; Set PWM0 duty [1:0] =0

MOVLW    20H
MOVWF    PWM0DH      ; Set PWM0 duty [9:2] =20H
MOVLW    01000000B
MOVWR    MR0B        ; R0B.6 (PWM0OE) =1, Enable PWM0 OUT (PA0)
```

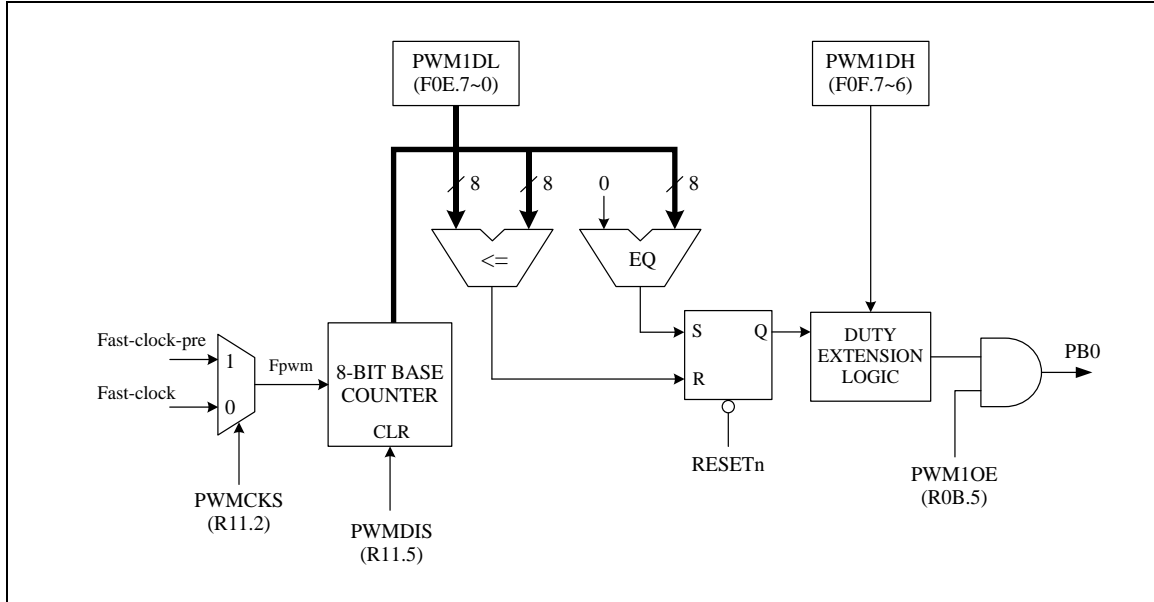
$F_{\text{sys}}=4$ MHz, PWM clock= $F_{\text{PWM}}/2=6$ MHz, PWM0PRD=80H, PWM0DL=00H, PWM0DH =20H

PWM0 output frequency= 6 MHz / (PWM0PRD+1) = 6 MHz/129=46512 KHz

PWM0 output duty= $32 / 128=25\%$.

3.6 PWM1: (8+2) bits PWM

The PWM1 is similar with PWM0. The differences are: PWM1 has no PWM1PRD, and no PWM1PSC adjustable



PWM1 Block Diagram

Example:

[CPU running at FAST mode, Fsys=FIRC 4 MHz]

; Setup PWM1 clock source.

```
MOVLW    0000000B    ; R11.5 (PWMDIS)= 0, PWM0/PWM1 clock enable
MOVWR    MR11        ; R11.2 (PWMCKS)= 0, FPWM=Fast-clock(4 MHz)
```

```
MOVLW    C0H
MOVWF    F0F        ; Set PWM1 duty[1:0] =3
```

```
MOVLW    80H
MOVWF    PWM1DH    ; Set PWM1 duty[9:2] =80H
```

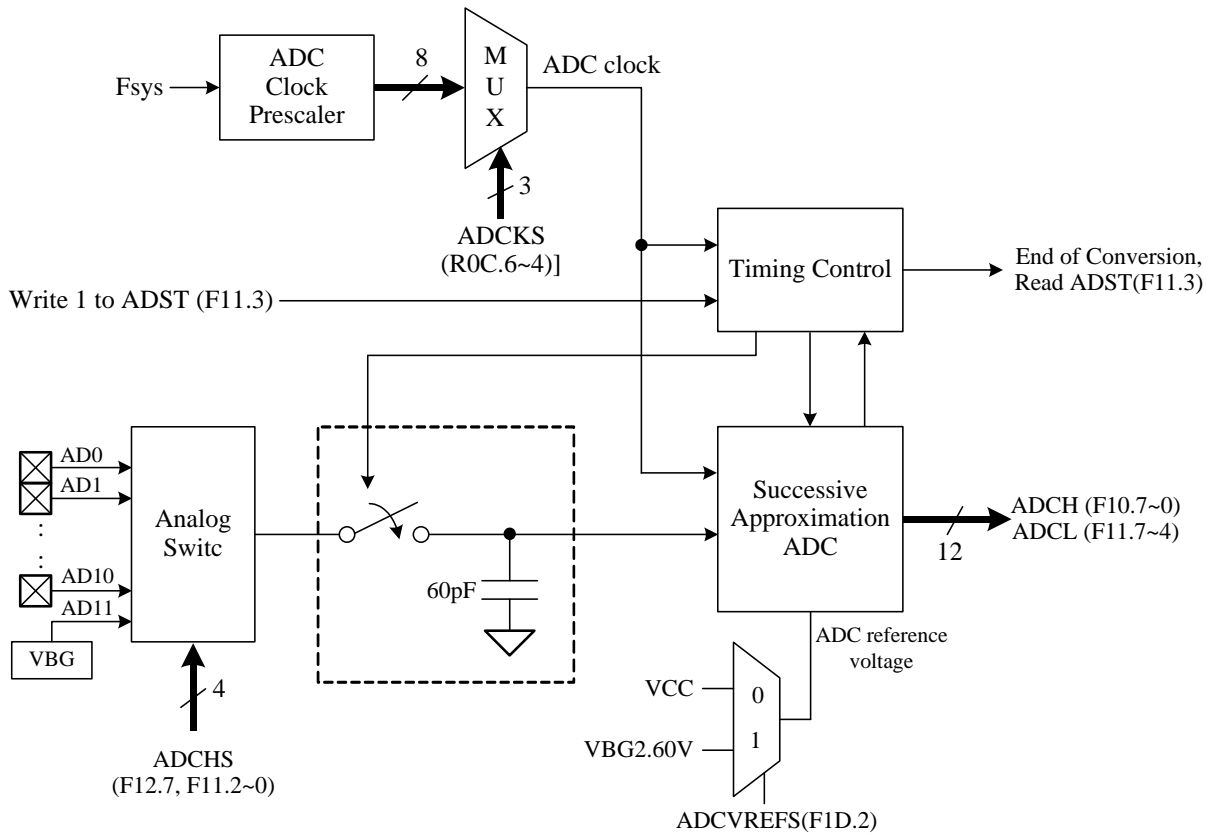
```
MOVLW    00100000B
MOVWR    MR0B      ; R0B.5 (PWM1OE) =1, Enable PWM1 OUT (PB0)
```

Fsys=4 MHz, PWM clock source=Fast-clock = 4 MHz, PWM1DL=3, PWM1DH=80H

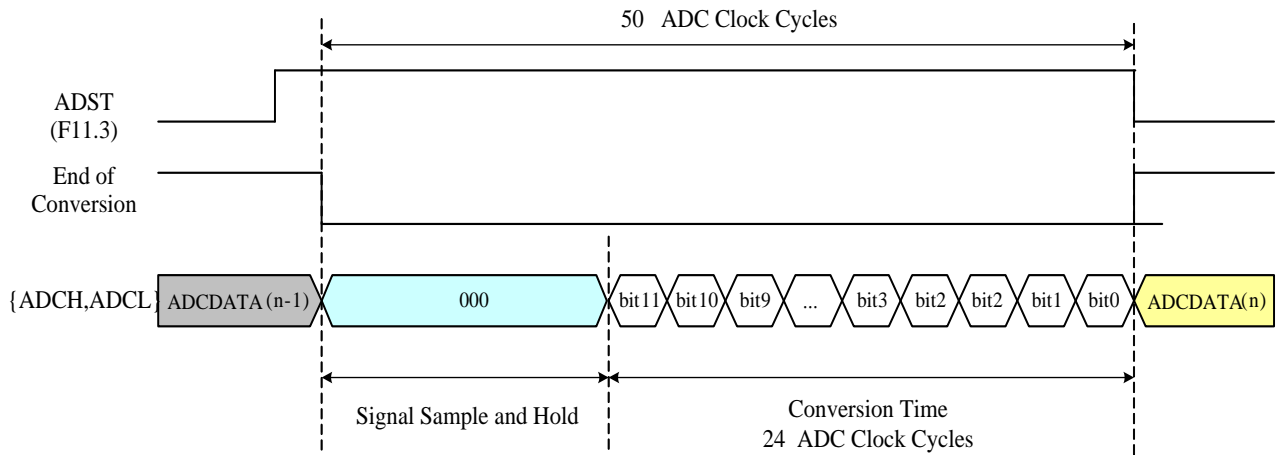
PWM1 output frequency=4 MHz/256=15.625 KHz

PWM1 output duty=128/256=50%.

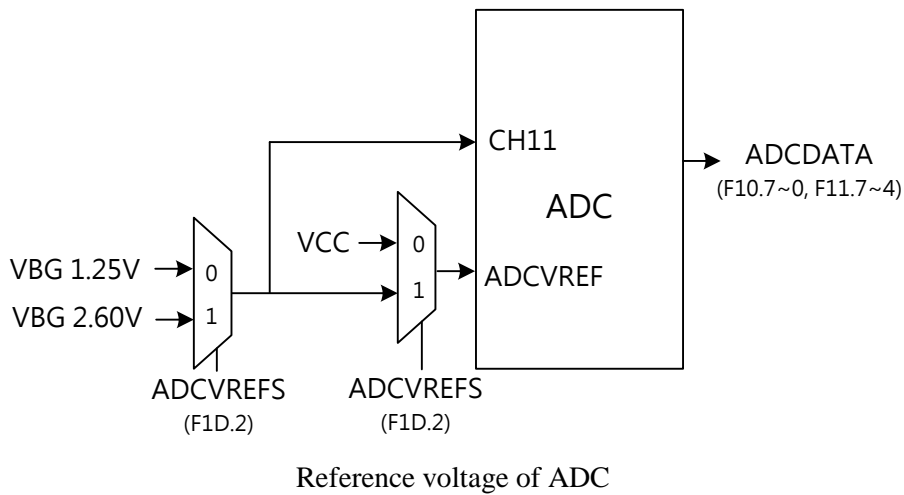
3.7 Analog-to-Digital Converter



The 12-bit ADC (Analog to Digital Converter) consists of an 11-channel analog input multiplexer, control register, clock generator, 12-bit successive approximation register, and output data register. To use the ADC, user needs to set **ADCKS (R0C.6~4)** to choose a proper ADC clock frequency. User then launches the ADC conversion by setting the **ADST (F11.3)** control bit. After end of conversion, H/W automatic clears the **ADST (F11.3)** bit. User can poll this bit to know the conversion status. The **ADPIE8 (R13.2~0)**, **ADPIE (R12.7~0)** control registers are used for ADC pin configuration, user can write the corresponding bit to “0” when the pin is used as an ADC input. The setting can disable the pin logical input path to save power consumption.



As shown in the figure below, the user has two ADC reference voltages to choose from. If the user chooses $ADCVREFS = 0$, the ADC reference voltage source is VCC , and the user can choose to switch the channel to CH11 ($V_{BG1.25V}$) to calculate the current voltage VCC . If the user chooses $ADCVREFS = 1$, the ADC reference voltage source is $V_{BG2.60V}$, and it must operate under the environment of $VCC > 2.8V$ to work normally. Before using the "SLEEP" command, set $ADCVREFS = 0$ to reduce power consumption.



◇ Example:

[CPU running at FAST mode , Fsys=FIRC 4 MHz]

ADC clock frequency=500 KHz, ADC channel=ADC0 (PA6).

```

MOV LW    01010000B    ; R0C.6~4 (ADCKS)
MOV WR    MR0C         ; ADC clock frequency=Fsys/8= 500 KHz

MOV LW    01000000B    ; ADC0 (PA6)
MOV WR    PAPUN        ;R08
MOV LW    11111110B    ; ADC0 (PA6)
MOV WR    ADPIE        ;R12

MOV LW    00000000B
MOV WF    ADCTL        ; F11.2~0 (ADCHS[2:0])= 0, ADC select ADC0 (PA6 pin).
BCF      ADCHS3        ; F12.7 (ADCHS[3]) =0

BSF      ADST          ; F11.3 (ADST), ADC start conversion.

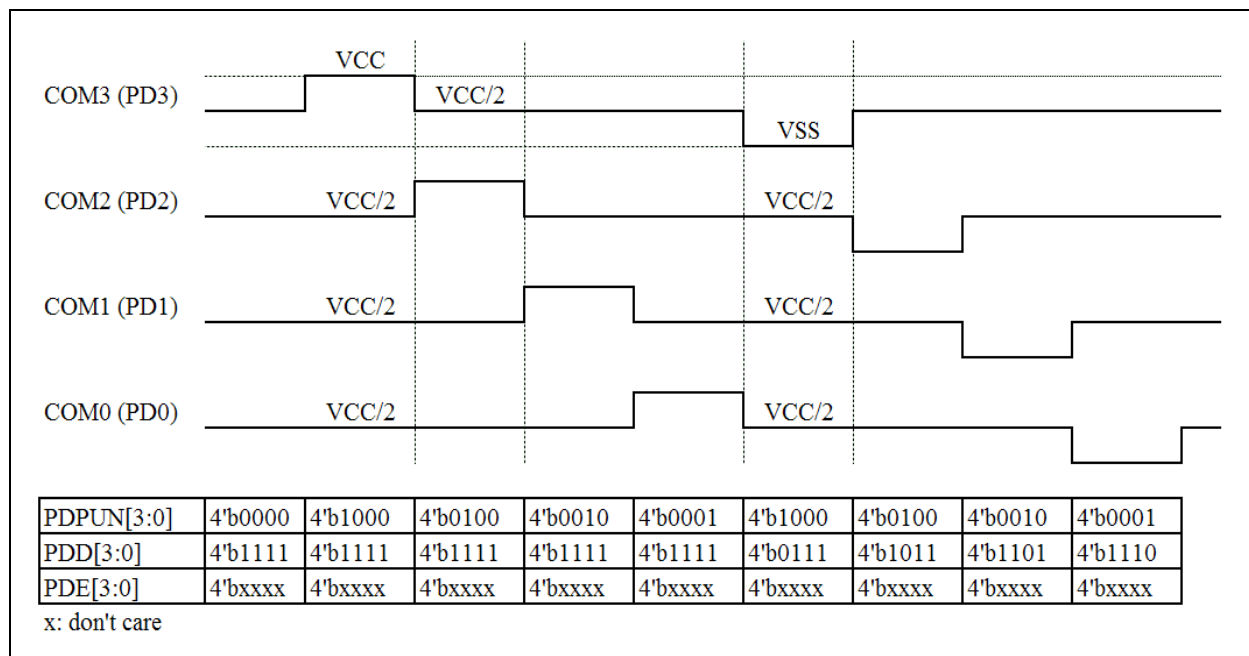
WAIT_ADC:
BTFSC    ADST          ; Wait ADC conversion finish.
GOTO     WAIT_ADC

MOV FW    ADCH         ; F10.7~0, Read ADC result [11:4] into W
MOV FW    ADCTL        ; F11.7~4, Read ADC result [3:0] into W
    
```

3.8 1/2 bias VCC/2 Voltage Generator

By setting SYSCFG (PD3IOE) option to be LCD mode, can enable entire PD[3:0] as LCD COM3~COM0 and will also always disable anyone PD[3:0] I/O function, meanwhile PDE[3:0] (R07.3~0) are invalid. LCD mode can output VCC、VCC/2、VSS three levels voltage to PD[3:0] by setting corresponding PDUN[3:0], PDD[3:0] shown as below pins state table. If enter STOP/IDLE mode, these PD[3:0] will automatically pull to VCC level.

	PD3IOE (SYSCFG[9])	PDPUN[3:0] (R0A.3~0)	PDE[3:0] (R07.3~0)	PDD[3:0] (F07.3~0)	Pins State
I/O mode	1	1/0	1/0	1/0	Normal IO
LCD mode	0	0	x	x	VCC/2
	0	1	x	0	VSS
	0	1	x	1	VCC



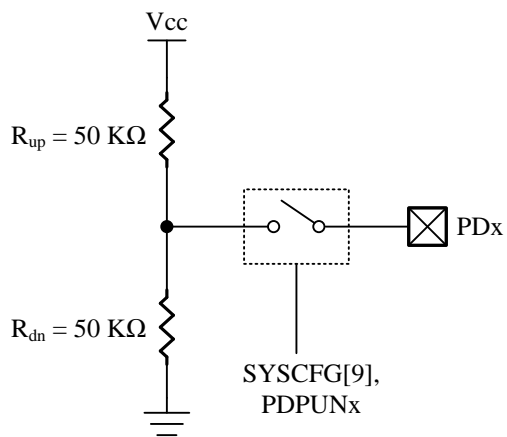
1/2 bias VCC/2 voltage generator by S/W control (PD3IOE=0)

◇ Example:

```

MOVLW    x0000xxxB    ;
MOVWR    ADPIE8      ; PD0~PD3 set to non-digital input mode
MOVLW    xxxx1000B   ;
MOVWR    PDPUN       ; PD2~PD0 output VCC/2, PD3 depend on PDD[3]

MOVLW    xxxx0111B   ;
MOVWF    PDD         ; PD3 output VSS
    
```

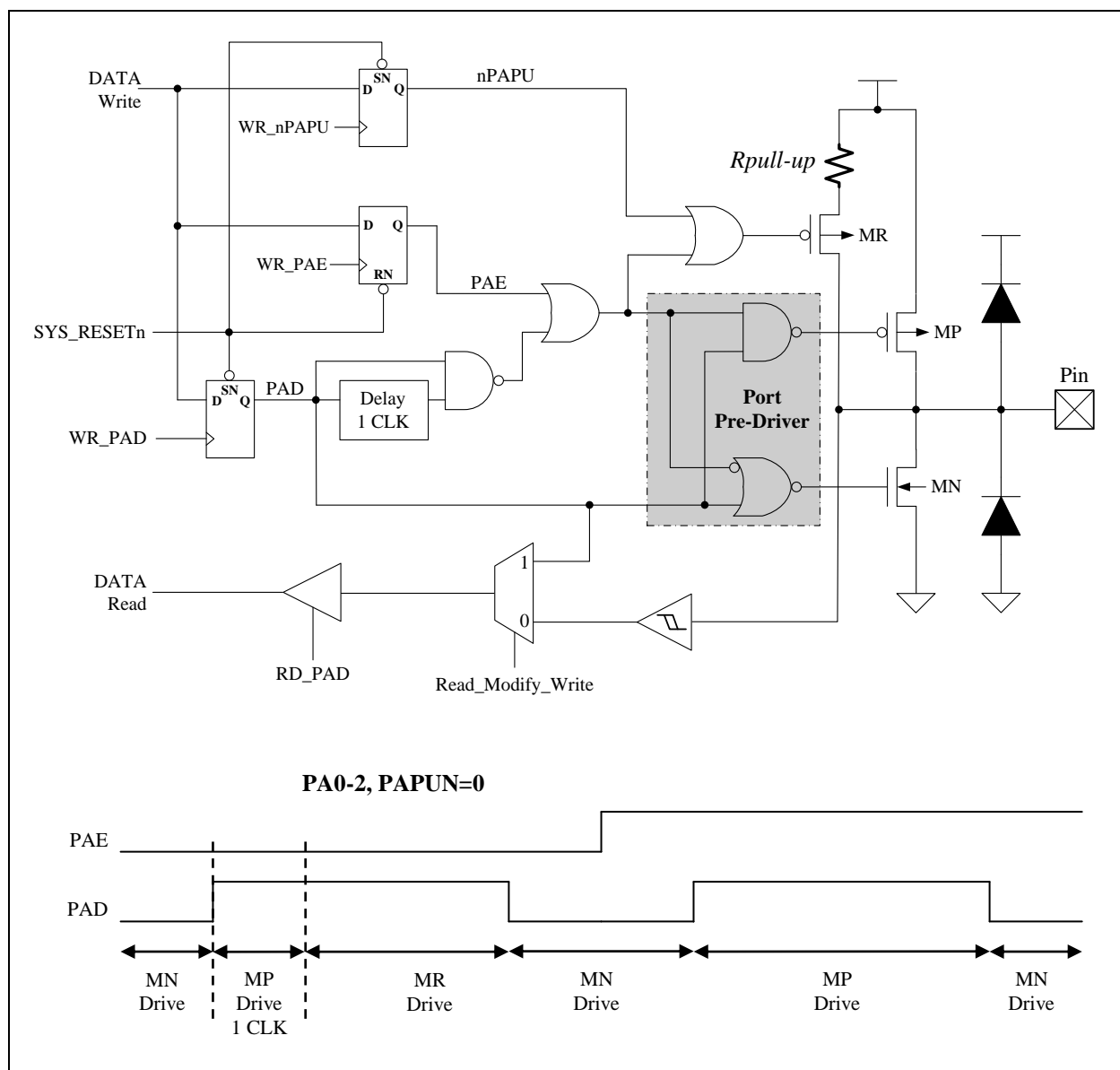


LCD COM3~0 bias circuit

4. I/O Port

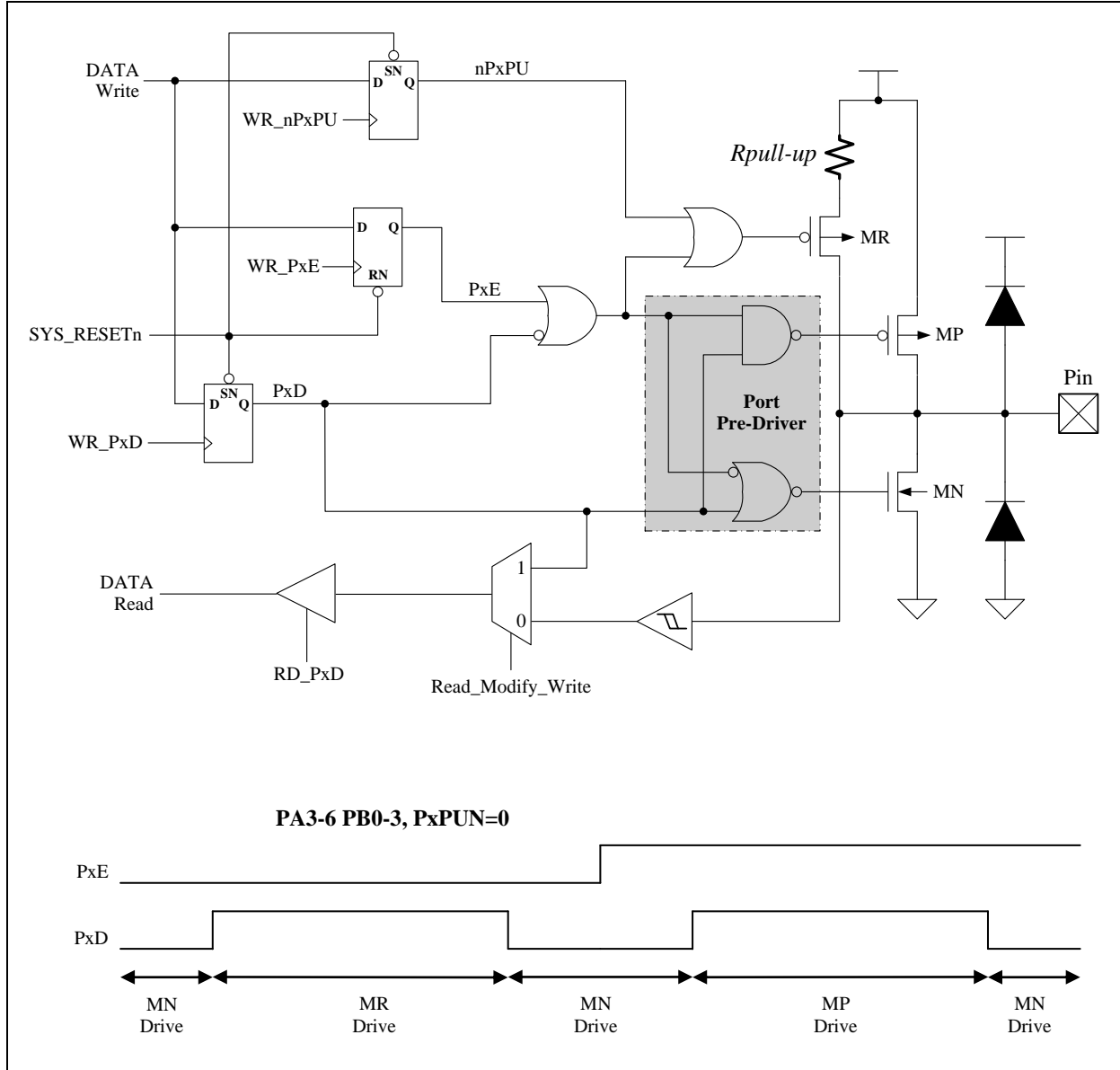
4.1 PA0-2

These pins can be used as Schmitt-trigger input, CMOS push-pull output or “pseudo-open-drain” output. The pull-up resistor is assignable to each pin by S/W setting. To use the pin in Schmitt-trigger input mode, S/W needs to set the PAE=0 and PAD=1. To use the pin in “pseudo-open-drain” mode, S/W sets the PAE=0. The benefit of pseudo-open-drain structure is that the output rise time can be much faster than pure open-drain structure. S/W sets PAE=1 to use the pin in CMOS push-pull output mode. Reading the pin data (PAD) has different meaning. In “Read-Modify-Write” instruction, CPU actually reads the output data register. In the others instructions, CPU reads the pin state. The so-called “Read-Modify-Write” instruction includes BSF, BCF and all instructions using F-Plane as destination. °

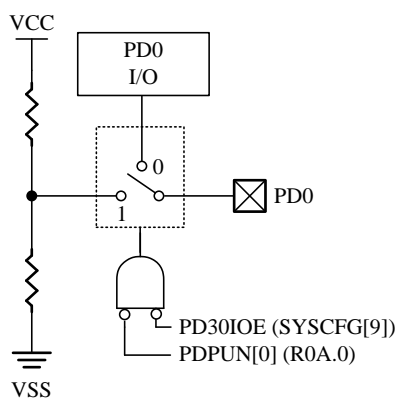


4.2 PA3-6, PB0-1, PD0-7

These pins are almost the same as PA0-2, except they do not support pseudo-open-drain mode. They can be used in pure open-drain mode, instead.



PD0-PD3 pins architecture as below, more controls refer to the section “3.8 1/2 bias VCC/2 Voltage Generator”



◇Example: I/O mode selecting

```
MOVLW    FFH
MOVWF    PDD
MOVLW    00H
MOVWR    PDPUN ; Set PD port pull-high enable
MOVLW    00H
MOVWR    PDE ; Set all ports to be Schmitt-trigger input
```

◇Example: Set PA0-2 is pseudo-open-drain mode

```
MOVLW    xxxxx000B
MOVWR    PAE ; Set PA2-PA0 as pseudo-open-drain mode

MOVLW    xxxxx000B
MOVWF    PAD ; PA2~PA0 output low level.
```

◇Example: Set PA0-2 is CMOS push-pull output mode.

```
MOVLW    xxxxx111B
MOVWR    PAE ; Set PA2-PA0 as CMOS push-pull output mode
```

◇Example: Read data from input port.

```
MOVLW    FFH ; "pseudo-open-drain" I/O structure, port must output High first
MOVWF    PDD ; before read pin
MOVWF    PDD ; Read data from Port D.
```

◇Example: Write data to output port.

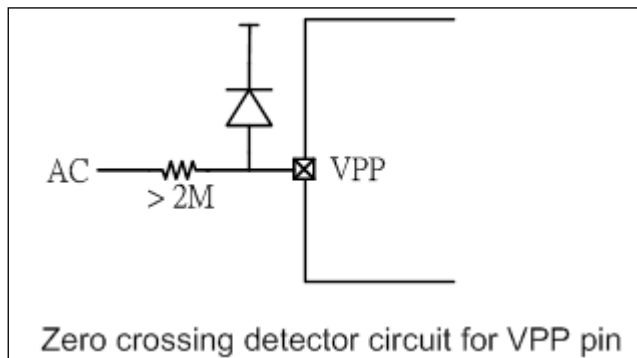
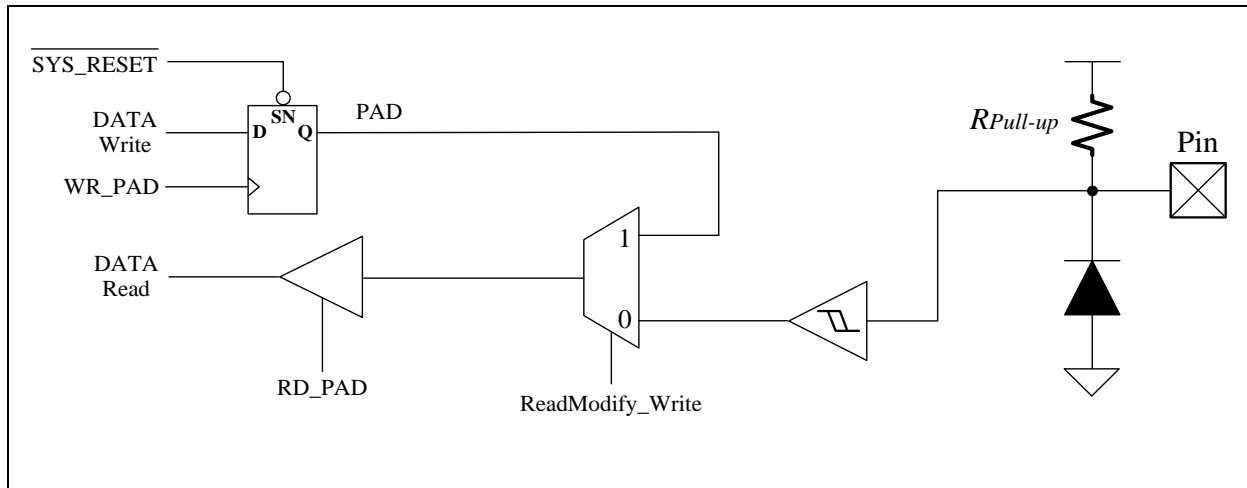
```
MOVLW    55H
MOVWF    PAD ; Write data 55H to Port A.
MOVWF    PBD ; Write data 55H to Port B.
```

◇Example: Write one bit data to output port.

```
BCF PAD, 0
BCF PBD, 1
BCF PDD, 2 ; Set PA0, PB1 and PD2 to be "0".
BSF PAD, 3
BSF PBD, 4
BSF PDD, 7 ; Set PA3, PB4 and PD7 to be "1".
```

4.3 PA7

PA7 can be only used in Schmitt-trigger input mode. The pull-up resistor is always connected to this pin. PA7/VPP has no high voltage protection diode, need an external diode and resistor to achieve AC zero crossing detection



◇Example: Read state from PA7.

Condition: SYSCFG[7] is set to “0”. (If SYSCFG[7] = “1”, then PA7 pin to be external reset pin function.)

```

BTFSS    PAD,7
GOTO     LOOP_A      ; If PA7=0.
GOTO     LOOP_B      ; If PA7=1.
    
```


MEMORY MAP

F-Plane

Name	Address	R/W	Rst	Description
(F00) INDF Function related to: RAM W/R				
INDF	00.7~0	R/W	-	Not a physical register, addressing INDF actually point to the register whose address is contained in the FSR register
(F01) TM0 Function related to: Timer0				
TM0	01.7~0	R/W	0	Timer0 content
(F02) PCL Function related to: PROGRAM COUNT				
PCL	02.7~0	R/W	0	Programming Counter LSB[7~0]
(F03) STATUS Function related to: STATUS				
GB0	03.7	R/W	0	General purpose bit 0
GB1	03.6	R/W	0	General purpose bit 1
RAMBK	03.5	R/W	0	RAM Bank Selection (Fixed to 0)
TO	03.4	R	0	WDT timeout flag, cleared by PWRST, 'SLEEP' or 'CLRWDI' instruction
PD	03.3	R	0	Sleep mode flag, set by 'SLEEP', cleared by 'CLRWDI' instruction
Z	03.2	R/W	0	Zero flag
DC	03.1	R/W	0	Decimal Carry flag
C	03.0	R/W	0	Carry flag
(F04) FSR Function related to: RAM W/R				
GB2	04.7	R/W	0	General purpose bit 2
FSR	04.6~0	R/W	-	File Select Register, indirect address mode pointer
(F05) PAD Function related to: Port A				
PAD7	05.7	R	-	PA7 pin state
PAD	05.6~0	R	-	Port A pin or "data register" state
		W	7F	Port A output data register
(F06) PBD Function related to: Port B				
PBD	06.1~0	R	-	Port B pin or "data register" state
		W	3	Port B output data register
(F07) PDD Function related to: Port D				
PDD	07.7~0	R	-	Port D pin or "data register" state
		W	FF	Port D output data register

Name	Address	R/W	Rst	Description
(F09) INTIF Function related to: Interrupt Flag				
	09.7			Reserved
T2IF	09.6	R	-	T2 interrupt event pending flag, set by H/W while T2 overflows
		W	0	write 0: clear this flag; write 1: no action
TM1IF	09.5	R	-	Timer1 interrupt event pending flag, set by H/W while Timer1 overflows
		W	0	write 0: clear this flag; write 1: no action
TM0IF	09.4	R	-	Timer0 interrupt event pending flag, set by H/W while Timer0 overflows
		W	0	write 0: clear this flag; write 1: no action
WKTIF	09.3	R	-	WKT interrupt event pending flag, set by H/W while WKT time out
		W	0	write 0: clear this flag; write 1: no action
INT2IF	09.2	R	-	INT2(PA7) interrupt event pending flag, set by H/W at INT2 pin's falling edge
		W	0	write 0: clear this flag; write 1: no action
INT1IF	09.1	R	-	INT1(PA1) interrupt event pending flag, set by H/W at INT1 pin's f/r edge
		W	0	write 0: clear this flag; write 1: no action
INT0IF	09.0	R	-	INT0(PA6) interrupt event pending flag, set by H/W at INT0 pin's falling edge
		W	0	write 0: clear this flag; write 1: no action
(F0A) TM1 Function related to: Timer1				
TM1	0a.7~0	R/W	0	Timer1 content
(F0B) CLKS Function related to: CPUCLK				
	0b.7		0	Reserved
SIRCKS	0b.6~5	R/W	3	SIRC clock selection 0:120KHz 1:30KHz 2:7.5KHz 3:1.875KHz
FASTSTP	0b.4	R/W	0	Fast-clock control 0: Fast-clock Enable 1: Fast-clock Disable
CPUCKS	0b.3	R/W	0/1	System clock (Fsys) selection, the reset value depends on SYSCFG[5]. 0: Fast-clock 1: Slow-clock If MODE3V(SYSCFG[5])=1, the reset value is 1, otherwise is 0
SLOWEN	0b.2	R/W	1	If CPUCKS=1, this SLOWEN bit is invalid, Slow-clock keep oscillating. If CPUCKS=0, set 1 to enable Slow-clock oscillate, clear 0 to stop Slow-clock oscillating. Set SLOWEN=0 to save power before enter STOP mode.
	0b.1~0		0	Reserved
(F0C) PWM0DH Function related to: PWM0				
PWM0DH	0c.7~0	R/W	0	PWM0 duty 8-bit MSB
(F0D) PWM0DL Function related to: PWM0				
PWM0DL	0d.7~6	R/W	0	PWM0 duty 2-bit LSB
	0d.5~0			Reserved

Name	Address	R/W	Rst	Description
(F0E) PWM1DH				Function related to: PWM1
PWM1DH	0e.7~0	R/W	0	PWM1 duty 8-bit MSB
(F0F) MF0F				Function related to : PWM1 / Table Read
PWM1DL	0f.7~6	R/W	0	PWM1 duty 2-bit LSB
	0f.5~3			Reserved
DPH	0f.2~0	R/W	0	Table read high address, data rom pointer (DPTR) high byte
(F10) ADCH				Function related to: ADC
ADCH	10.7~0	R	-	ADC output data MSB, ADQ[11:4]
(F11) ADCTL				Function related to: ADC
ADCL	11.7~4	R	-	ADC output data LSB, ADQ[3:0]
ADST	11.3	R/W	0	ADC start bit. 0: H/W clear after end of conversion 1: ADC start conversion,
ADCHS	11.2~0	R/W	0	ADC channel select bit2~bit0. {ADCHS3(F12.7), ADCHS} = 0000: ADC0 (PA6) 0100: ADC4 (PD7) 1000: ADC8 (PA0) 0001: ADC1 (PA1) 0101: ADC5 (PA5) 1001: ADC9 (PD5) 0010: ADC2 (PA2) 0110: ADC6 (PD6) 1010: ADC10 (PD4) 0011: ADC3 (PB1) 0111: ADC7 (PB0) 1011: VBG 1.25v
(F12) MF12				Function related to: ADC/T2/TM1/TM0
ADCHS3	12.7	R/W	0	ADC channel select bit3
	12.6~3			Reserved
T2CLR	12.2	R/W	1	T2 counter clear 0: Release 1: Clear and hold
TM1STP	12.1	R/W	0	Timer1 counter stop 0: Release 1: Stop counting
TM0STP	12.0	R/W	0	Timer0 counter stop 0: Release 1: Stop counting
(F13) DPL				Function related to: Table Read
DPL	13.7~0	R/W	0	Table read low address, data ROM pointer (DPTR) low byte
(F1C) NRSTEN				Function related to: Natural reset
NRSTEN	1c.1~0	R/W	01	Natural Reset Enable. 01 : Disable other : Enable. Natural reset is used to protect ROM against extreme voltage or temperature; this function will be closed automatically by H/W during IDLE/STOP mode.
(F1D) MF1D				Function related to: ADC
	1d.5	R/W	1	Reversed. This bit must fix 1.
	1d.4	R/W	1	Reversed. This bit must fix 1.
	1d.3	R/W	0	Reversed. This bit must fix 0.
ADCVREFS	1d.2	R/W	0	ADC reference voltage select. 0:VCC 1:VBG 2.60V *Before using "SLEEP" instruction, set ADCVREFS=0 to reduce power consumption.
(F1F) IRCF				Function relate to: Trim FIRC
IRCF	1f.6~0	R	-	Read the current FIRC TRIM value
User Data Memory				
SRAM	20~27	R/W	-	RAM common area (8 Bytes)
	28~7F	R/W	-	RAM BANK0 area (RAMBK=0, 88 Bytes)

R-Plane

Name	Address	R/W	Rst	Description
(R02) TM0CTL				Function related to: TCOUT/TM0
TCOPSC	02.7~6	W	0	TCOUT prescaler 0: Fsys/2 1: Fsys/4 2: Fsys/8 3: Fsys/16
TM0EDG	02.5	W	0	Timer0 prescaler counting edge for TM0CKI (PA2) pin 0: rising edge 1: falling edge
TM0CKS	02.4	W	0	Timer0 prescaler clock source 0:Fsys/2 1: TM0CKI (PA2) pin
TM0PSC	02.3~0	W	0	Timer0 prescaler. Timer0 prescaler clock source divided by 0000: Fsys/2 0101: Fsys/64 0001: Fsys/4 0110: Fsys/128 0010: Fsys/8 0111: Fsys/256 0011: Fsys/16 1xxx: Fsys/512 0100: Fsys/32
(R03) PWRDN				Function related to: Power Down
PWRDN	03	W	-	write this register to enter STOP/IDLE Mode (i.e. 'SLEEP' instruction)
(R04) WDTCLR				Function related to: WDT
WDTCLR	04	W	-	write this register to clear WDT timer (i.e. 'CLRWDT' instruction)
(R05) PAE				Function related to: Port A
PAE	05.6~3	W	0	Each bit controls its corresponding pin, if the bit is 0: the pin is open-drain output or Schmitt-trigger input 1: the pin is CMOS push-pull output
	05.2~0	W	0	Each bit controls its corresponding pin, if the bit is 0: the pin is pseudo-open-drain output or Schmitt-trigger input 1: the pin is CMOS push-pull output
(R06) PBE				Function related to: Port B
PBE	06.1~0	W	0	Each bit controls its corresponding pin, if the bit is 0: the pin is open-drain output or Schmitt-trigger input 1: the pin is CMOS push-pull output
(R07) PDE				Function related to: Port D
PDE	07.7~0	W	0	When PD30IOE=1 , each bit controls its corresponding pin, if the bit is 0: the pin is open-drain output or Schmitt-trigger input 1: the pin is CMOS push-pull output When PD30IOE=0 , PDE[3:0] will be invalid.
(R08) PAPUN				Function related to: Port A
PAPUN	08.6~0	W	7F	Each bit controls its corresponding pin, if the bit is 0: the pin pull up resistor is enabled, except a. the pin's output data register (PAD) is 0 b. the pin's CMOS push-pull mode is chosen (PAE=1) c. the pin is working for PWM output 1: the pin pull up resistor is disabled
(R09) PBPUN				Function related to: Port B
PBPUN	09.1~0	W	3	Each bit controls its corresponding pin, if the bit is 0: the pin pull up resistor is enabled, except a. the pin's output data register (PBD) is 0 b. the pin's CMOS push-pull mode is chosen (PBE=1) c. the pin is working for PWM output 1: the pin pull up resistor is disabled

Name	Address	R/W	Rst	Description
(R0A) PDPUN Function related to: Port D				
PDPUN	0a.7~0	W	FF	<p>When PD30IOE=1, each bit controls its corresponding pin, if the bit is 0: the pin pull up resistor is enabled, except</p> <p>a. the pin's output data register (PDD) is 0</p> <p>b. the pin's CMOS push-pull mode is chosen (PDE=1)</p> <p>c. pins are working for TM1OUT/TCOUT output</p> <p>1: the pin pull up resistor is disabled</p> <p>When PD30IOE=0, each PDPUN[3:0] corresponding bit is</p> <p>0: the pin can output VCC/2</p> <p>1: the pin can output VCC or VSS, depend on PDD value</p>
(R0B) MR0B Function related to: PWM0/PWM1/INT1/TCOUT/TM1/WKT				
	0b.7			Reserved
PWM0OE	0b.6	W	0	Enable PWM0 output to PA0 pin
PWM1OE	0b.5	W	0	Enable PWM1 output to PB0 pin
INT1EDG	0b.4	W	0	INT1 pin (PA1) edge interrupt event 0: falling edge to trigger 1: rising edge to trigger
TCOE	0b.3	W	0	0:Disable post-prescaler Instruction Cycle(Fsys/2) output. 1:Enable post-prescaler Instruction Cycle(Fsys/2) output to PD6 pin (TCOUT)
TM1OE	0b.2	W	0	Enable Timer1 overflow toggle output to PD0 pin (TM1OUT)
WKTpsc	0b.1~0	W	3	WKT period 00: 17 ms 01: 34 ms 10: 68 ms 11: 136 ms @VCC=4V
(R0C) MR0C Function related to: ADC/TM1				
	0c.7			Reserved
ADCKS	0c.6~4	W	0	ADC clock frequency selection: 000: Fsys/256 100: Fsys/16 001: Fsys/128 101: Fsys/8 010: Fsys/64 110: Fsys/4 011: Fsys/32 111: Fsys/2
TM1PSC	0c.3~0	W	0	Timer1 prescaler. Timer1 clock source divided by 0000: Fsys/2 0101: Fsys/64 0001: Fsys/4 0110: Fsys/128 0010: Fsys/8 0111: Fsys/256 0011: Fsys/16 1xxx: Fsys/512 0100: Fsys/32
(R0D) TM1RLD Function related to: TM1				
TM1RLD	0d.7~0	W	0	Timer1 reload offset value while it rolls over
(R0E) INTIE Function related to: Interrupt Enable				
	0e.7			Reserved
T2IE	0e.6	W	0	T2 interrupt enable, 1=enable, 0=disable
TM1IE	0e.5	W	0	Timer1 interrupt enable, 1=enable, 0=disable
TM0IE	0e.4	W	0	Timer0 interrupt enable, 1=enable, 0=disable
WKTIE	0e.3	W	0	Wakeup Timer interrupt enable, 1=enable, 0=disable Set 0 to clear & disable WKT timer
INT2IE	0e.2	W	0	INT2 pin(PA7) interrupt enable, 1=enable, 0=disable
INT1IE	0e.1	W	0	INT1 pin(PA1) interrupt enable, 1=enable, 0=disable
INT0IE	0e.0	W	0	INT0 pin(PA6) interrupt enable, 1=enable, 0=disable
(R0F) TEST				
TSTREG	0f.7~0	W	0	Test mode register, user does not write it.

Name	Address	R/W	Rst	Description
(R11) MR11				Function related to: EFT/PWM0/PWM1
	11.7	W	0	Reserved, keep write to 0.
VCCFLT	11.6	W	0	Enable EFT enhance operation mode, 1=enable, 0=disable
PWMDIS	11.5	W	0	PWM0 / PWM1 clock disable(PWMDIS=1) or enable(PWMDIS=0)
	11.4~3			Reserved
PWMCKS	11.2	W	0	PWM0 / PWM1 clock source, $F_{PWM} =$ 0: Fast-clock 1: Fast-clock-pre
PWM0PSC	11.1~0	W	0	PWM0 prescaler, PWM0 clock source divided by 00: F_{PWM} 01: $F_{PWM}/2$ 10: $F_{PWM}/4$ 11: $F_{PWM}/64$
(R12) ADPIE				Function related to: ADC
ADPIE	12.7	W	1	Each bit controls its corresponding port I/O enable pin, if the bit is 0: enable ADC7 channel input 1: enable PB0 I/O digital input
	12.6	W	1	0: enable ADC6 channel input 1: enable PD6 I/O digital input
	12.5	W	1	0: enable ADC5 channel input 1: enable PA5 I/O digital input
	12.4	W	1	0: enable ADC4 channel input 1: enable PD7 I/O digital input
	12.3	W	1	0: enable ADC3 channel input 1: enable PB1 I/O digital input
	12.2	W	1	0: enable ADC2 channel input 1: enable PA2 I/O digital input
	12.1	W	1	0: enable ADC1 channel input 1: enable PA1 I/O digital input
	12.0	W	1	0: enable ADC0 channel input 1: enable PA6 I/O digital input
(R13) ADPIE8				Function related to: ADC
ADPIE8	13.7			Reserved
	13.6	W	1	0: enable non-digital input 1: enable PD0 I/O digital input
	13.5	W	1	0: enable non-digital input 1: enable PD1 I/O digital input
	13.4	W	1	0: enable non-digital input 1: enable PD2 I/O digital input
	13.3	W	1	0: enable non-digital input 1: enable PD3 I/O digital input
	13.2	W	1	0: enable ADC10 channel input 1: enable PD4 I/O digital input
	13.1	W	1	0: enable ADC9 channel input 1: enable PD5 I/O digital input
	13.0	W	1	0: enable ADC8 channel input 1: enable PA0 I/O digital input
(R14) PMW0PRD				Function related to: PWM0
PWM0PRD	14.7~0	W	FF	PWM0 period data
(R15) MR15				Function related to: WDT/T2/CPUCLK
WDTPSC	15.7~6	W	1	WDT period 00:137 ms 01:274 ms 10:1096 ms 11:2192 ms @VCC=4V
WDTSTP	15.5	W	0	WDT disable in IDLE/STOP mode, If WDTE=0, this bit is invalid 1: clear & stop counting 0: always counting
T2CKS	15.4	W	0	“T2 clock source” selection. 1: Fsys/128 0: Slow-clock
FCLKDIV	15.3~2	W	1	Fast-clock divider, Fast-clock is 00: Fast-clock-pre/8 01: Fast-clock-pre/3 10: Fast-clock-pre/2 11: Fast-clock-pre
T2PSC	15.1~0	W	0	T2 prescaler. “T2 clock source” divided by - 00: 32768 01: 16384 10: 8192 11: 128
(R16) LVR20OFF				Function related to: LVR2.0V
LVR20OFF	16.7~0	W	-	Write this register with 0x37 to force LVR2.0V disable

INSTRUCTION SET

Each instruction is a 14-bit word divided into an Op Code, which specifies the instruction type, and one or more operands, which further specify the operation of the instruction. The instructions can be categorized as byte-oriented, bit-oriented and literal operations list in the following table.

For byte-oriented instructions, “f” or “r” represents the address designator and “d” represents the destination designator. The address designator is used to specify which address in Program memory is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If “d” is “0”, the result is placed in the W register. If “d” is “1”, the result is placed in the address specified in the instruction.

For bit-oriented instructions, “b” represents a bit field designator, which selects the number of the bit affected by the operation, while “f” represents the address designator. For literal operations, “k” represents the literal or constant value.

Field / Legend	Description
f	F-Plane Register File Address
r	R-Plane Register File Address
b	Bit address
k	Literal. Constant data or label
d	Destination selection field. 0 : Working register 1 : Register file
TO	WDT Time Out Flag
PD	Power Down Flag
W	Working Register
Z	Zero Flag
C	Carry Flag
DC	Decimal Carry Flag
PC	Program Counter
TOS	Top Of Stack
GIE	Global Interrupt Enable Flag (i-Flag)
[]	Option Field
()	Contents
.	Bit Field
B	Before
A	After
←	Assign direction

Mnemonic		Op Code	Cycle	Flag Affect	Description
Byte-Oriented File Register Instruction					
ADDWF	f,d	00 0111 dfff ffff	1	C, DC, Z	Add W and "f"
ANDWF	f,d	00 0101 dfff ffff	1	Z	AND W with "f"
CLRF	f	00 0001 1fff ffff	1	Z	Clear "f"
CLRW		00 0001 0100 0000	1	Z	Clear W
COMF	f,d	00 1001 dfff ffff	1	Z	Complement "f"
DECf	f,d	00 0011 dfff ffff	1	Z	Decrement "f"
DECFSZ	f,d	00 1011 dfff ffff	1 or 2	-	Decrement "f", skip if zero
INCF	f,d	00 1010 dfff ffff	1	Z	Increment "f"
INCFSZ	f,d	00 1111 dfff ffff	1 or 2	-	Increment "f", skip if zero
IORWF	f,d	00 0100 dfff ffff	1	Z	OR W with "f"
MOVFW	f	00 1000 0fff ffff	1	-	Move "f" to W
MOVWF	f	00 0000 1fff ffff	1	-	Move W to "f"
MOVWR	r	00 0000 00rr rrrr	1	-	Move W to "r"
RLF	f,d	00 1101 dfff ffff	1	C	Rotate left "f" through carry
RRF	f,d	00 1100 dfff ffff	1	C	Rotate right "f" through carry
SUBWF	f,d	00 0010 dfff ffff	1	C, DC, Z	Subtract W from "f"
SWAPF	f,d	00 1110 dfff ffff	1	-	Swap nibbles in "f"
TESTZ	f	00 1000 1fff ffff	1	Z	Test if "f" is zero
XORWF	f,d	00 0110 dfff ffff	1	Z	XOR W with "f"
Bit-Oriented File Register Instruction					
BCF	f,b	01 000b bbff ffff	1	-	Clear "b" bit of "f"
BSF	f,b	01 001b bbff ffff	1	-	Set "b" bit of "f"
BTFSC	f,b	01 010b bbff ffff	1 or 2	-	Test "b" bit of "f", skip if clear
BTFSS	f,b	01 011b bbff ffff	1 or 2	-	Test "b" bit of "f", skip if set
Literal and Control Instruction					
ADDLW	k	01 1100 kkkk kkkk	1	C, DC, Z	Add Literal "k" and W
ANDLW	k	01 1011 kkkk kkkk	1	Z	AND Literal "k" with W
CALL	k	10 kkkk kkkk kkkk	2	-	Call subroutine "k"
CLRWDt		00 0000 0000 0100	1	TO, PD	Clear Watch Dog Timer
GOTO	k	11 kkkk kkkk kkkk	2	-	Jump to branch "k"
IORLW	k	01 1010 kkkk kkkk	1	Z	OR Literal "k" with W
MOVLW	k	01 1001 kkkk kkkk	1	-	Move Literal "k" to W
NOP		00 0000 0000 0000	1	-	No operation
RET		00 0000 0100 0000	2	-	Return from subroutine
RETI		00 0000 0110 0000	2	-	Return from interrupt
RETLW	k	01 1000 kkkk kkkk	2	-	Return with Literal in W
TABRL		00 0000 0101 0000	2	-	Lookup ROM low data to W
TABRH		00 0000 0101 1000	2	-	Lookup ROM high data to W
SLEEP		00 0000 0000 0011	1	TO, PD	Go into Power-down mode, Clock oscillation stops
XORLW	k	01 1111 kkkk kkkk	1	Z	XOR Literal "k" with W

ADDLW	Add Literal "k" and W	
Syntax	ADDLW k	
Operands	k : 00h ~ FFh	
Operation	$(W) \leftarrow (W) + k$	
Status Affected	C, DC, Z	
OP-Code	01 1100 kkkk kkkk	
Description	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.	
Cycle	1	
Example	ADDLW 0x15	B : W = 0x10 A : W = 0x25

ADDWF	Add W and "f"	
Syntax	ADDWF f [,d]	
Operands	f : 00h ~ 7Fh, d : 0, 1	
Operation	$(\text{destination}) \leftarrow (W) + (f)$	
Status Affected	C, DC, Z	
OP-Code	00 0111 dfff ffff	
Description	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.	
Cycle	1	
Example	ADDWF FSR, 0	B : W = 0x17, FSR = 0xC2 A : W = 0xD9, FSR = 0xC2

ANDLW	Logical AND Literal "k" with W	
Syntax	ANDLW k	
Operands	k : 00h ~ FFh	
Operation	$(W) \leftarrow (W) \text{ AND } k$	
Status Affected	Z	
OP-Code	01 1011 kkkk kkkk	
Description	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.	
Cycle	1	
Example	ANDLW 0x5F	B : W = 0xA3 A : W = 0x03

ANDWF	AND W with "f"	
Syntax	ANDWF f [,d]	
Operands	f : 00h ~ 7Fh, d : 0, 1	
Operation	$(\text{destination}) \leftarrow (W) \text{ AND } (f)$	
Status Affected	Z	
OP-Code	00 0101 dfff ffff	
Description	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.	
Cycle	1	
Example	ANDWF FSR, 1	B : W = 0x17, FSR = 0xC2 A : W = 0x17, FSR = 0x02

BCF Clear "b" bit of "f"

Syntax	BCF f [,b]	
Operands	f : 00h ~ 3Fh, b : 0 ~ 7	
Operation	(f.b) ← 0	
Status Affected	-	
OP-Code	01 000b bbff ffff	
Description	Bit 'b' in register 'f' is cleared.	
Cycle	1	
Example	BCF FLAG_REG, 7	B : FLAG_REG = 0xC7 A : FLAG_REG = 0x47

BSF Set "b" bit of "f"

Syntax	BSF f [,b]	
Operands	f : 00h ~ 3Fh, b : 0 ~ 7	
Operation	(f.b) ← 1	
Status Affected	-	
OP-Code	01 001b bbff ffff	
Description	Bit 'b' in register 'f' is set.	
Cycle	1	
Example	BSF FLAG_REG, 7	B : FLAG_REG = 0x0A A : FLAG_REG = 0x8A

BTFSC Test "b" bit of "f", skip if clear(0)

Syntax	BTFSC f [,b]	
Operands	f : 00h ~ 3Fh, b : 0 ~ 7	
Operation	Skip next instruction if (f.b) = 0	
Status Affected	-	
OP-Code	01 010b bbff ffff	
Description	If bit 'b' in register 'f' is 1, then the next instruction is executed. If bit 'b' in register 'f' is 0, then the next instruction is discarded, and a NOP is executed instead, making this a 2nd cycle instruction.	
Cycle	1 or 2	
Example	LABEL1 BTFSC FLAG, 1 TRUE GOTO SUB1 FALSE ...	B : PC = LABEL1 A : if FLAG.1 = 0, PC = FALSE if FLAG.1 = 1, PC = TRUE

BTFSS Test "b" bit of "f", skip if set(1)

Syntax	BTFSS f [,b]	
Operands	f : 00h ~ 3Fh, b : 0 ~ 7	
Operation	Skip next instruction if (f.b) = 1	
Status Affected	-	
OP-Code	01 011b bbff ffff	
Description	If bit 'b' in register 'f' is 0, then the next instruction is executed. If bit 'b' in register 'f' is 1, then the next instruction is discarded, and a NOP is executed instead, making this a 2nd cycle instruction.	
Cycle	1 or 2	
Example	LABEL1 BTFSS FLAG, 1 TRUE GOTO SUB1 FALSE ...	B : PC = LABEL1 A : if FLAG.1 = 0, PC = TRUE if FLAG.1 = 1, PC = FALSE

CALL	Call subroutine "k"
Syntax	CALL k
Operands	k : 000h ~ FFFh
Operation	Operation: TOS \leftarrow (PC) + 1, PC.11~0 \leftarrow k
Status Affected	-
OP-Code	10 kkkk kkkk kkkk
Description	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The 12-bit immediate address is loaded into PC bits <11:0>. CALL is a two-cycle instruction.
Cycle	2
Example	LABEL1 CALL SUB1 B : PC = LABEL1 A : PC = SUB1, TOS = LABEL1 + 1

CLRF	Clear "f"
Syntax	CLRF f
Operands	f : 00h ~ 7Fh
Operation	(f) \leftarrow 00h, Z \leftarrow 1
Status Affected	Z
OP-Code	00 0001 1fff ffff
Description	The contents of register 'f' are cleared and the Z bit is set.
Cycle	1
Example	CLRF FLAG_REG B : FLAG_REG = 0x5A A : FLAG_REG = 0x00, Z = 1

CLRW	Clear W
Syntax	CLRW
Operands	-
Operation	(W) \leftarrow 00h, Z \leftarrow 1
Status Affected	Z
OP-Code	00 0001 0100 0000
Description	W register is cleared and Z bit is set.
Cycle	1
Example	CLRW B : W = 0x5A A : W = 0x00, Z = 1

CLRWD	Clear Watchdog Timer
Syntax	CLRWD
Operands	-
Operation	WDT Timer \leftarrow 00h
Status Affected	TO, PD
OP-Code	00 0000 0000 0100
Description	CLRWD instruction clears the Watchdog Timer
Cycle	1
Example	CLRWD B : WDT counter = ? A : WDT counter = 0x00

COMF	Complement "f"
Syntax	COMF f [,d]
Operands	f : 00h ~ 7Fh, d : 0, 1
Operation	(destination) ← (\bar{f})
Status Affected	Z
OP-Code	00 1001 dfff ffff
Description	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.
Cycle	1
Example	COMF REG1, 0 B : REG1 = 0x13 A : REG1 = 0x13, W = 0xEC

DECF	Decrement "f"
Syntax	DECF f [,d]
Operands	f : 00h ~ 7Fh, d : 0, 1
Operation	(destination) ← (f) - 1
Status Affected	Z
OP-Code	00 0011 dfff ffff
Description	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.
Cycle	1
Example	DECF CNT, 1 B : CNT = 0x01, Z = 0 A : CNT = 0x00, Z = 1

DECFSZ	Decrement "f", Skip if 0
Syntax	DECFSZ f [,d]
Operands	f : 00h ~ 7Fh, d : 0, 1
Operation	(destination) ← (f) - 1, skip next instruction if result is 0
Status Affected	-
OP-Code	00 1011 dfff ffff
Description	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, then a NOP is executed instead, making it a 2 cycle instruction.
Cycle	1 or 2
Example	LABEL1 DECFSZ CNT, 1 GOTO LOOP CONTINUE B : PC = LABEL1 A : CNT = CNT - 1 if CNT = 0, PC = CONTINUE if CNT ≠ 0, PC = LABEL1 + 1

GOTO	Unconditional Branch
Syntax	GOTO k
Operands	k : 000h ~ FFFh
Operation	PC.11~0 ← k
Status Affected	-
OP-Code	11 kkkk kkkk kkkk
Description	GOTO is an unconditional branch. The 12-bit immediate value is loaded into PC bits <11:0>. GOTO is a two-cycle instruction.
Cycle	2
Example	LABEL1 GOTO SUB1 B : PC = LABEL1 A : PC = SUB1

INCF	Increment "f"	
Syntax	INCF f [,d]	
Operands	f : 00h ~ 7Fh	
Operation	(destination) ← (f) + 1	
Status Affected	Z	
OP-Code	00 1010 dfff ffff	
Description	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.	
Cycle	1	
Example	INCF CNT, 1	B : CNT = 0xFF, Z = 0 A : CNT = 0x00, Z = 1

INCFSZ	Increment "f", Skip if 0	
Syntax	INCFSZ f [,d]	
Operands	f : 00h ~ 7Fh, d : 0, 1	
Operation	(destination) ← (f) + 1, skip next instruction if result is 0	
Status Affected	-	
OP-Code	00 1111 dfff ffff	
Description	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead, making it a 2 cycle instruction.	
Cycle	1 or 2	
Example	LABEL1 INCFSZ CNT, 1 GOTO LOOP CONTINUE	B : PC = LABEL1 A : CNT = CNT + 1 if CNT = 0, PC = CONTINUE if CNT ≠ 0, PC = LABEL1 + 1

IORLW	Inclusive OR Literal with W	
Syntax	IORLW k	
Operands	k : 00h ~ FFh	
Operation	(W) ← (W) OR k	
Status Affected	Z	
OP-Code	01 1010 kkkk kkkk	
Description	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.	
Cycle	1	
Example	IORLW 0x35	B : W = 0x9A A : W = 0xBF, Z = 0

IORWF	Inclusive OR W with "f"	
Syntax	IORWF f [,d]	
Operands	f : 00h ~ 7Fh, d : 0, 1	
Operation	(destination) ← (W) OR k	
Status Affected	Z	
OP-Code	00 0100 dfff ffff	
Description	Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.	
Cycle	1	
Example	IORWF RESULT, 0	B : RESULT = 0x13, W = 0x91 A : RESULT = 0x13, W = 0x93, Z = 0

MOVFW Move "f" to W

Syntax	MOVFW f	
Operands	f : 00h ~ 7Fh	
Operation	(W) ← (f)	
Status Affected	-	
OP-Code	00 1000 0fff ffff	
Description	The contents of register 'f' are moved to W register.	
Cycle	1	
Example	MOVFW FSR	B : FSR = 0xC2, W = ? A : FSR = 0xC2, W = 0xC2

MOVLW Move Literal to W

Syntax	MOVLW k	
Operands	k : 00h ~ FFh	
Operation	(W) ← k	
Status Affected	-	
OP-Code	01 1001 kkkk kkkk	
Description	The eight-bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.	
Cycle	1	
Example	MOVLW 0x5A	B : W = ? A : W = 0x5A

MOVWF Move W to "f"

Syntax	MOVWF f	
Operands	f : 00h ~ 7Fh	
Operation	(f) ← (W)	
Status Affected	-	
OP-Code	00 0000 1fff ffff	
Description	Move data from W register to register 'f'.	
Cycle	1	
Example	MOVWF REG1	B : REG1 = 0xFF, W = 0x4F A : REG1 = 0x4F, W = 0x4F

MOVWR Move W to "r"

Syntax	MOVWR r	
Operands	r : 00h ~ 3Fh	
Operation	(r) ← (W)	
Status Affected	-	
OP-Code	00 0000 00rr rrrr	
Description	Move data from W register to register 'r'.	
Cycle	1	
Example	MOVWR REG1	B : REG1 = 0xFF, W = 0x4F A : REG1 = 0x4F, W = 0x4F

NOP No Operation

Syntax	NOP
Operands	-
Operation	No Operation
Status Affected	-
OP-Code	00 0000 0000 0000
Description	No Operation
Cycle	1
Example	NOP

RET Return from Subroutine

Syntax	RET
Operands	-
Operation	PC ← TOS
Status Affected	-
OP-Code	00 0000 0100 0000
Description	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.
Cycle	2
Example	RET A : PC = TOS

RETI Return from Interrupt

Syntax	RETI
Operands	-
Operation	PC ← TOS, GIE ← 1
Status Affected	-
OP-Code	00 0000 0110 0000
Description	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in to the PC. Interrupts are enabled. This is a two-cycle instruction.
Cycle	2
Example	RETI A : PC = TOS, GIE = 1

RETLW Return with Literal in W

Syntax	RETLW k
Operands	k : 00h ~ FFh
Operation	PC ← TOS, (W) ← k
Status Affected	-
OP-Code	01 1000 kkkk kkkk
Description	The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Cycle	2
Example	CALL TABLE B : W = 0x07 : TABLE ADDWF PCL, 1 A : W = value of k8 RETLW k1 RETLW k2 : RETLW kn

TABRL Return DPTR low byte to W

Syntax	TABRL	
Operands	-	
Operation	(W) ← ROM[DPTR] low byte content, Where DPTR={DPH[max:8],DPL[7:0]}	
Status Affected	-	
OP-Code	00 0000 0101 0000	
Description	The W register is loaded with low byte of ROM[DPTR]. This is a two-cycle instruction.	
Cycle	2	
Example	:	
	:	
	MOVLW	(TAB1&0xFF)
	MOVWF	DPL ; Where DPL is F-plane register
	MOVLW	(TAB1>>8)&0xFF
	MOVWF	DPH ; Where DPH is F-plane register
	TABRL	; W=0x89
	TABRH	; W=0x37
		ORG 0234H
	TAB1:	
	.DT	0x3789, 0x2277 ;ROM data 14 bits

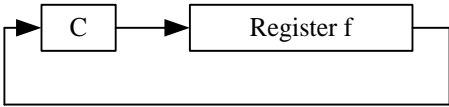
TABRH Return DPTR high byte to W

Syntax	TABRH	
Operands	-	
Operation	(W) ← ROM[DPTR] high byte content, Where DPTR={DPH[max:8],DPL[7:0]}	
Status Affected	-	
OP-Code	00 0000 0101 1000	
Description	The W register is loaded with high byte of ROM[DPTR]. This is a two-cycle instruction.	
Cycle	2	

RLF Rotate Left "f" through Carry

Syntax	RLF f [,d]	
Operands	f : 00h ~ 7Fh, d : 0, 1	
Operation		
Status Affected	C	
OP-Code	00 1101 dfff ffff	
Description	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.	
Cycle	1	
Example	RLF REG1, 0	B : REG1 = 1110 0110, C = 0 A : REG1 = 1110 0110 W = 1100 1100, C = 1

RRF Rotate Right "f" through Carry

Syntax	RRF f [,d]
Operands	f : 00h ~ 7Fh, d : 0, 1
Operation	
Status Affected	C
OP-Code	00 1100 dfff ffff
Description	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.
Cycle	1
Example	RRF REG1, 0 B : REG1 = 1110 0110, C = 0 A : REG1 = 1110 0110 W = 0111 0011, C = 0

SLEEP Go into standby mode, Clock oscillation stops

Syntax	SLEEP
Operands	-
Operation	-
Status Affected	TO, PD
OP-Code	00 0000 0000 0011
Description	Go into STOP mode with the oscillator stops.
Cycle	1
Example	SLEEP -

SUBWF Subtract W from "f"

Syntax	SUBWF f [,d]
Operands	f : 00h ~ 7Fh, d : 0, 1
Operation	(destination) ← (f) - (W)
Status Affected	C, DC, Z
OP-Code	00 0010 dfff ffff
Description	Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.
Cycle	1
Example	SUBWF REG1, 1 B : REG1 = 0x03, W = 0x02, C = ?, Z = ? A : REG1 = 0x01, W = 0x02, C = 1, Z = 0 SUBWF REG1, 1 B : REG1 = 0x02, W = 0x02, C = ?, Z = ? A : REG1 = 0x00, W = 0x02, C = 1, Z = 1 SUBWF REG1, 1 B : REG1 = 0x01, W = 0x02, C = ?, Z = ? A : REG1 = 0xFF, W = 0x02, C = 0, Z = 0

SWAPF

Swap Nibbles in "f"

Syntax	SWAPF f [,d]	
Operands	f : 00h ~ 7Fh, d : 0, 1	
Operation	(destination,7~4) ← (f.3~0), (destination.3~0) ← (f.7~4)	
Status Affected	-	
OP-Code	00 1110 dfff ffff	
Description	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.	
Cycle	1	
Example	SWAPF REG, 0	B : REG1 = 0xA5 A : REG1 = 0xA5, W = 0x5A

TESTZ

Test if "f" is zero

Syntax	TESTZ f	
Operands	f : 00h ~ 7Fh	
Operation	Set Z flag if (f) is 0	
Status Affected	Z	
OP-Code	00 1000 1fff ffff	
Description	If the content of register 'f' is 0, Zero flag is set to 1.	
Cycle	1	
Example	TESTZ REG1	B : REG1 = 0, Z = ? A : REG1 = 0, Z = 1

XORLW

Exclusive OR Literal with W

Syntax	XORLW k	
Operands	k : 00h ~ FFh	
Operation	(W) ← (W) XOR k	
Status Affected	Z	
OP-Code	01 1111 kkkk kkkk	
Description	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.	
Cycle	1	
Example	XORLW 0xAF	B : W = 0xB5 A : W = 0x1A

XORWF

Exclusive OR W with "f"

Syntax	XORWF f [,d]	
Operands	f : 00h ~ 7Fh, d : 0, 1	
Operation	(destination) ← (W) XOR (f)	
Status Affected	Z	
OP-Code	00 0110 dfff ffff	
Description	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.	
Cycle	1	
Example	XORWF REG, 1	B : REG = 0xAF, W = 0xB5 A : REG = 0x1A, W = 0xB5

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$)

Parameter	Rating	Unit
Supply voltage	$V_{SS}-0.3$ to $V_{SS}+6.5$	V
Operating voltage	LVR to $V_{SS}+5.5$	
Input voltage	$V_{SS}-0.3$ to $V_{CC}+0.3$	
Output voltage	$V_{SS}-0.3$ to $V_{CC}+0.3$	
Output current high per all PIN	-80	mA
Output current low per all PIN	+150	
Operating temperature	-40 to +105	$^{\circ}\text{C}$
Storage temperature	-65 to +150	

2. DC Characteristics (T_A=25°C)

Parameter	Sym	Conditions		Min.	Typ.	Max.	Unit
Input High Voltage	V _{IH}	All Input except PA7	V _{CC} =3~5V	0.6V _{CC}		V _{CC}	V
		PA7	V _{CC} =3~5V	0.7V _{CC}		V _{CC}	V
Input Low Voltage	V _{IL}	All Input except PA7	V _{CC} =3~5V	V _{SS}		0.2V _{CC}	V
		PA7	V _{CC} =3~5V	V _{SS}		0.2V _{CC}	V
Output High Current	I _{OH}	All Output	V _{CC} =5V, V _{OH} =4.5V	–	10	–	mA
			V _{CC} =3V, V _{OH} =2.7V	–	4	–	
Output Low Current	I _{OL}	All Output	V _{CC} =5V, V _{OL} =0.5V	–	40	–	mA
			V _{CC} =3V, V _{OL} =0.3V	–	18	–	
Input Leakage Current (pin high)	I _{ILH}	All Input	V _{IN} =V _{CC}	–	–	1	uA
Input Leakage Current (pin low)	I _{ILL}	All Input	V _{IN} =0V	–	–	–1	uA
Pull-up Resistor	R _{UP}	VIN=0 V Ports A/B/D	V _{CC} =5.0V	–	32	–	KΩ
			V _{CC} =3.0V	–	55	–	
		VIN=0 V PA7	V _{CC} =5.0V	–	165	–	
			V _{CC} =3.0V	–	165	–	

Parameter	Sym	Mode	Conditions	V _{CC}	Min.	Typ.	Max.	Unit
*Power Supply Current (No Load)	I _{CC}	FAST	FIRC12MHz	5V	–	4.3	–	mA
				3V	–	2.7	–	
			FIRC6MHz,	5V	–	3.6	–	
				3V	–	2.3	–	
			FIRC4MHz	5V	–	3.3	–	
				3V	–	2.1	–	
		SLOW	SIRC120KHz	5V	–	2	–	
				3V	–	1.4	–	
		IDLE (WKTPSC=3)	LVR2.3V LVR2.9V	5V	–	75	–	uA
				3V	–	45	–	
			LVR2.0V	5V	–	35	–	
				3V	–	15	–	
			All LVR disable	5V	–	22	–	
				3V	–	7	–	
		STOP	LVR2.0V	5V	–	14	–	
				3V	–	8	–	
All LVR disable	5V		–	0.1	1			
	3V		–	0.1	1			

* SYSCFG[5] = 1 (MODE3V=1) will force LVR2.3/LVR2.9 disable. More detail information, see Chapter 2.2.

* R-plane register 16h = 0x37 will force LVR2.0V disable. More detail information, see Chapter 2.2

3. Clock Timing ($T_A=25^\circ\text{C}$)

Parameter	Sym	Conditions	Min	Typ	Max	Unit
FIRC Clock Frequency	F_{FIRC}	$V_{\text{CC}}=5\text{V}$	–	12.0	–	MHz
		$V_{\text{CC}}=3\text{V}$	–	11.9	–	
SIRC Clock Frequency	F_{SIRC}	$V_{\text{CC}}=5\text{V}$	–	130	–	KHz
		$V_{\text{CC}}=3\text{V}$	–	120	–	

4. Reset Timing Characteristics ($T_A= -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Conditions	Min	Typ	Max	Unit
RESET Input Low width	Input $V_{\text{CC}}=5\text{ V} \pm 10\%$	3	–	–	μs
WDT time	$V_{\text{CC}}=3\sim 5\text{ V}$, WDT $\text{PSC}=11$	-30%	2192	+30%	ms
WKT time	$V_{\text{CC}}=3\sim 5\text{ V}$, WKT $\text{PSC}=11$	-30%	136	+30%	ms
CPU start up time	$V_{\text{CC}}=4\text{ V}$	–	15	–	ms

5. LVR Circuit Characteristics ($T_A=25^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
LVR Reference Voltage	LVR_{th}	-10%	2.0	+10%	V
		-3%	2.4	+3%	
		-3%-	3.05	+3%	
LVR Hysteresis Voltage	V_{HYST}	–	± 0.1	–	V
Low Voltage Detection time	t_{LVR}	100	–	–	μs

6. LCD Driver Characteristics ($T_A=25^\circ\text{C}$)

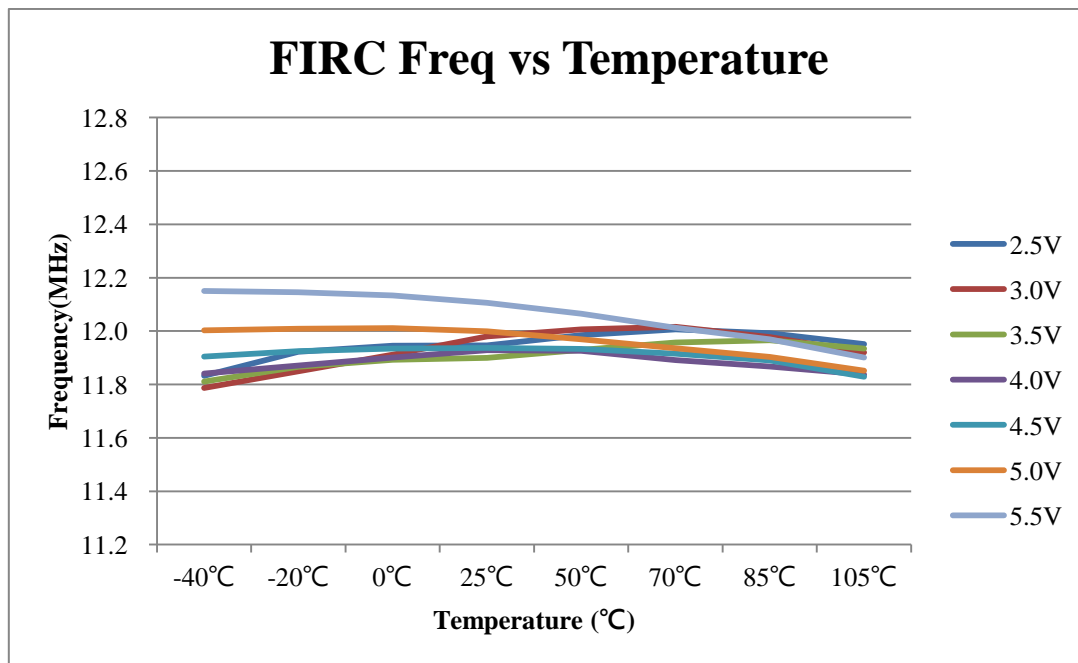
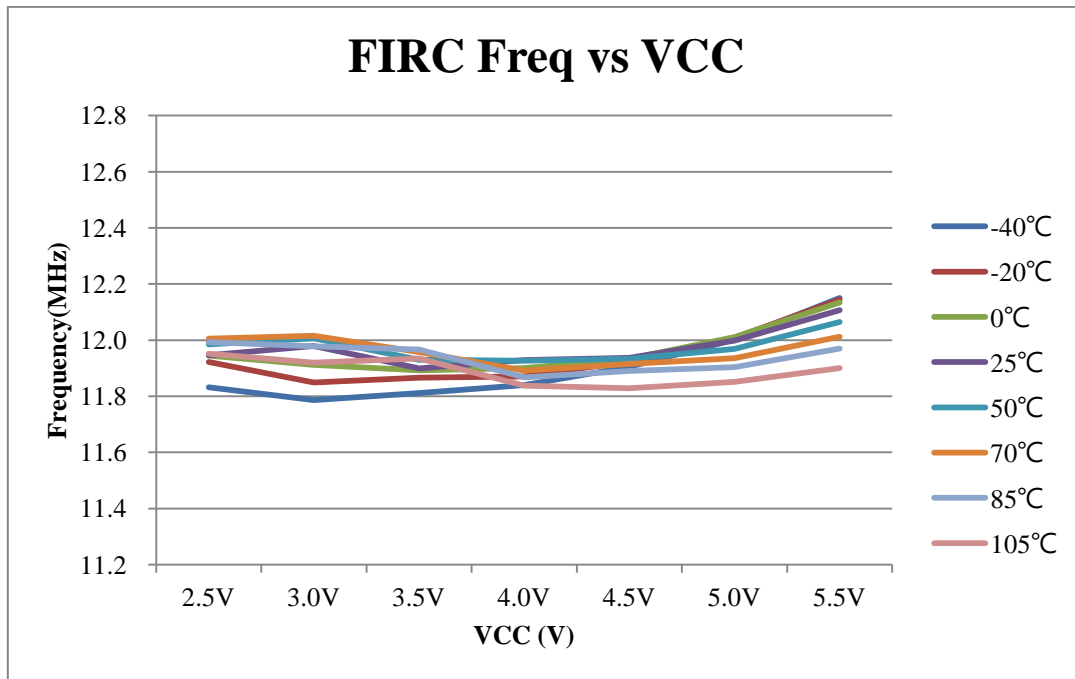
Parameter	Sym	Conditions	Min	Typ	Max	Unit
LCD resistance	R_{up}	$V_{\text{CC}}=3\sim 5\text{ V}$	–	50	–	$\text{K}\Omega$
	R_{dn}	$V_{\text{CC}}=3\sim 5\text{ V}$	–	50	–	$\text{K}\Omega$

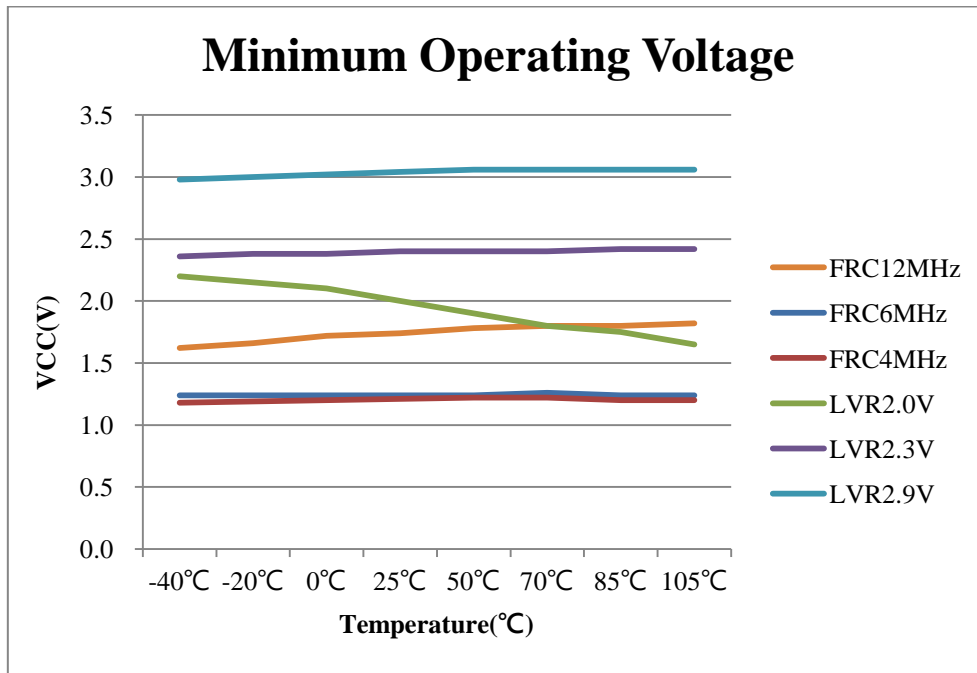
7. ADC Electrical Characteristics (TA=25°C, VCC=2.2V~ 5.5V, VSS=0V)

Parameter	Conditions	Min	Typ	Max	Units
Total Accuracy	V _{CC} =5.12V, V _{SS} =0V	-	±2.5	±4	LSB
Integral Non-Linearity		-	±3.2	±5	
Conversion Time	f _{ADC} =1 MHz	-	50	-	μs
Input Voltage	-	V _{SS}	-	V _{CC}	V
Max ADC Clock freq. (f _{ADC})	Source impedance (Rs < 10K ohm) & ADCVREF=VCC	-	-	2	MHz
	Source impedance (Rs < 20K ohm)	-	-	1	
	Source impedance (Rs < 50K ohm)	-	-	0.5	
	Source is VBG & ADCVREF=VCC	-	-	2	

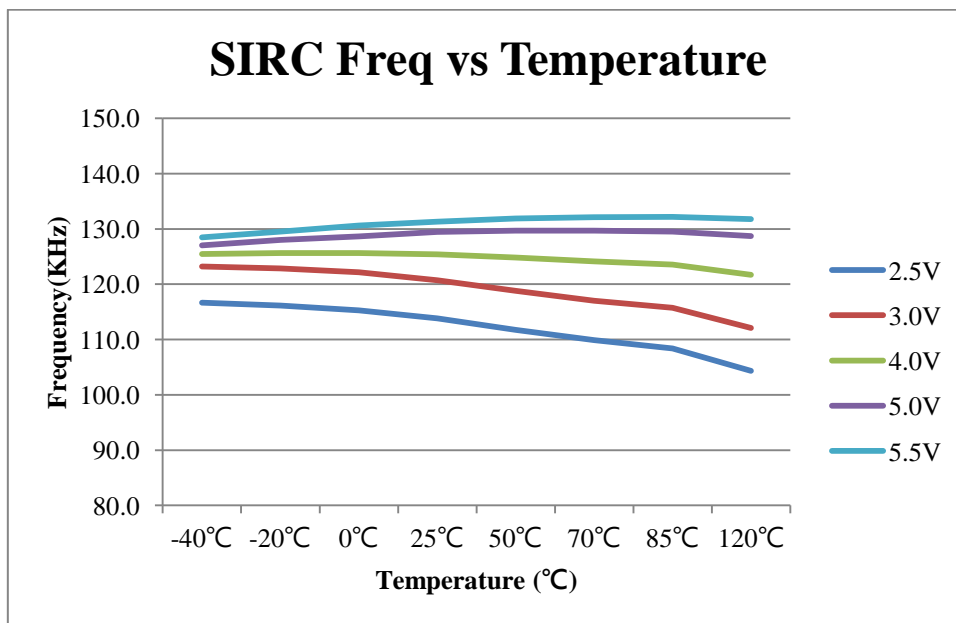
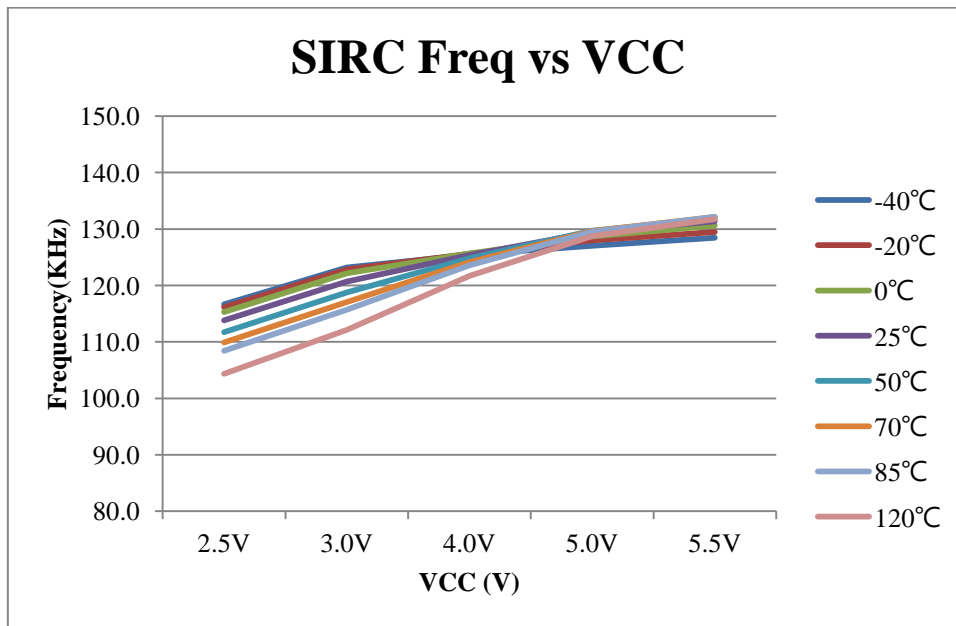
Parameter	Sym	Conditions	Min	Typ	Max	Units
Bandgap Reference Voltage	V _{BG}	VCC=2.5V~5.5V 25°C	-1%	1.25	+1%	V
		VCC=3V~4.5V -0°C~70°C	-1%	1.25	+1%	
		VCC=2.5V~5.0V -20°C~85°C	-2%	1.25	+2%	
		VCC=2.5V~5.5V -40°C~105°C	-3%	1.25	+2%	
ADC Reference Voltage (ADCVREFS=1)	V _{ADC}	VCC=3V~5.5V 25°C	-2.5%	2.60	+2.5%	V
		VCC=3V~4.5V -0°C~70°C	-2.5%	2.60	+2.5%	
		VCC=2.8V~5.0V -20°C~85°C	-3.5%	2.60	+3.5%	
		VCC=2.8V~5.5V -40°C~105°C	-4.5%	2.60	+3.5%	

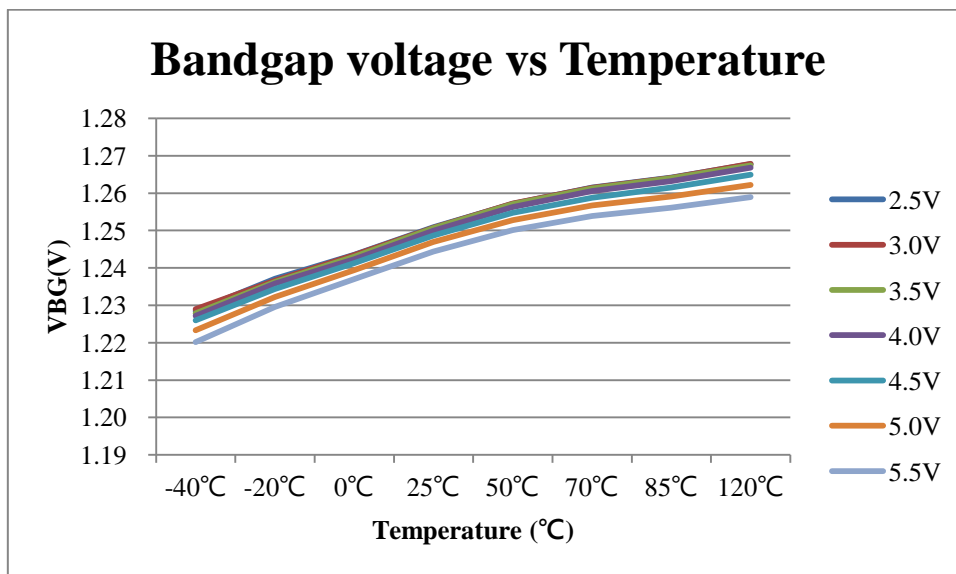
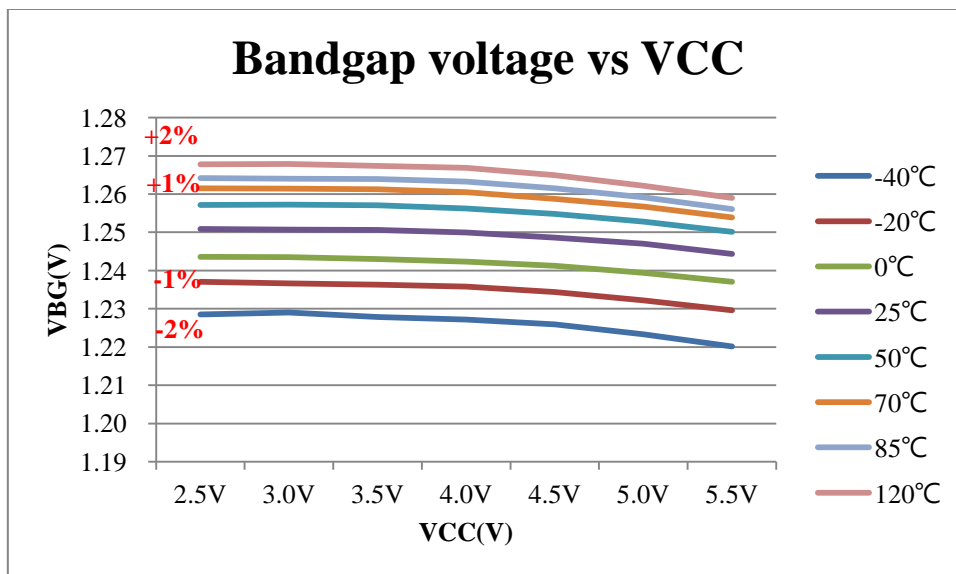
8. Characteristic Graphs





Note: Due to the variation of manufacturing process, this LVR2.0V will slightly vary between different chips.



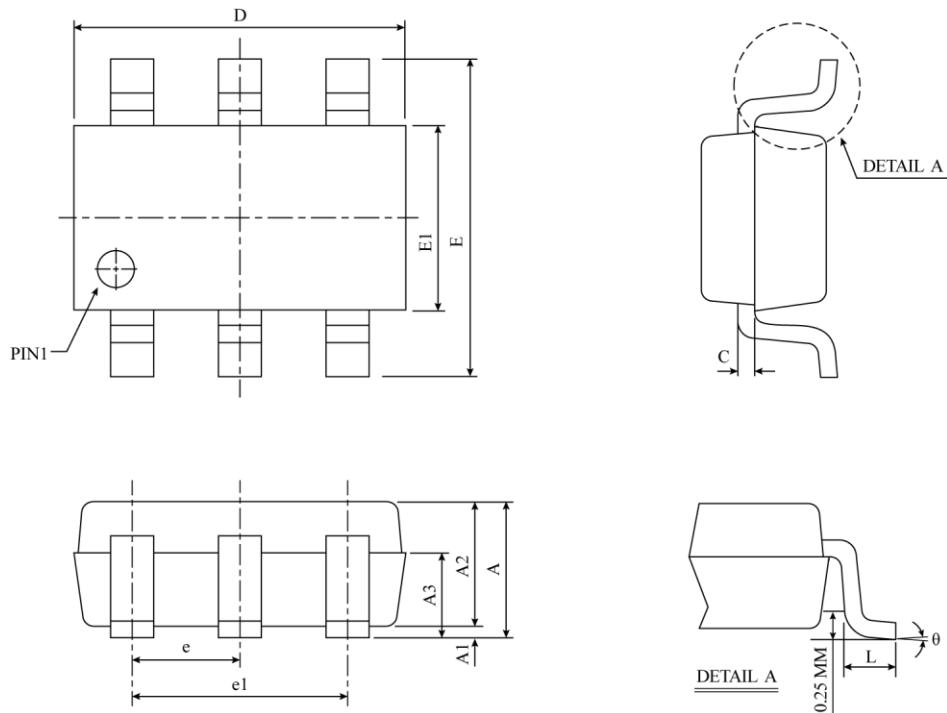


PACKAGING INFORMATION

Please note that the package information provided is for reference only. Since this information is frequently updated, users can contact Sales to consult the latest package information and stocks.

The ordering information:

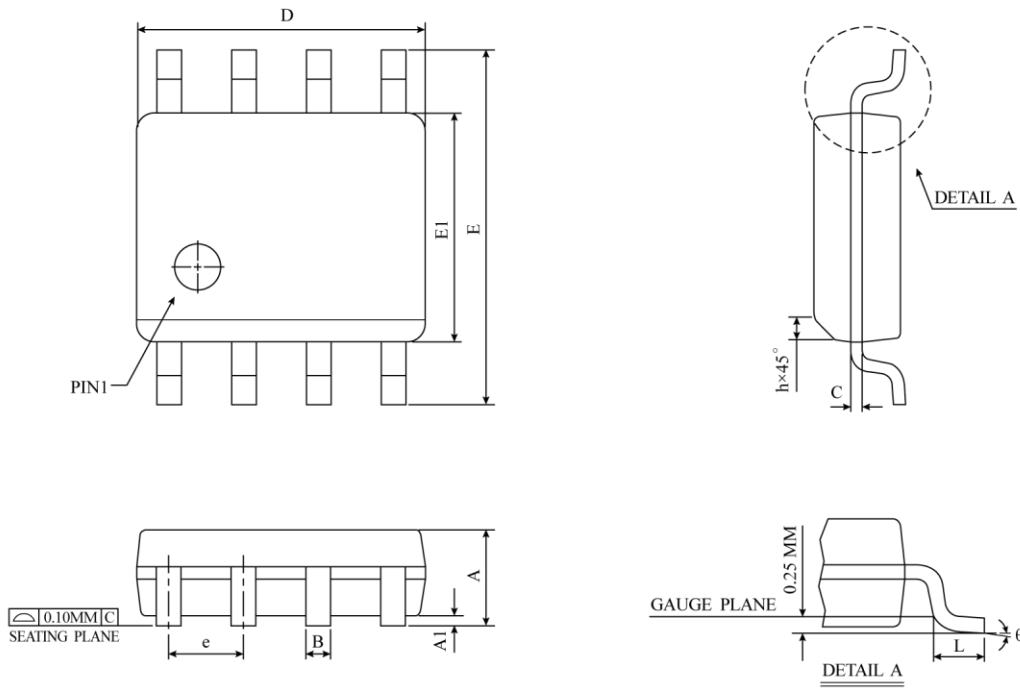
Ordering number	Package
TM57MA29NE-MTP	Wafer/Dice blank chip
TM57MA29NE -COD	Wafer/Dice with code
TM57MA29NE-MTP-A8	SOT23-6
TM57MA29NE-MTP-14	SOP 8-pin (150mil)
TM57MA29NE-MTP-53	MSOP 10-pin (118mil)
TM57MA29NE-MTP-15	SOP 14-pin (150mil)
TM57MA29NE-MTP-03	DIP 16-pin (300 mil)
TM57MA29NE-MTP-16	SOP 16-pin (150 mil)
TM57MA29NE-MTP-26	SSOP 16-pin (150 mil)
TM57MA29NE-MTP-05	DIP 20-pin (300 mil)
TM57MA29NE-MTP-21	SOP 20-pin (300 mil)
TM57MA29NE-MTP-27	SSOP 20-pin (150 mil)
TM57MA29NE-MTP-46	TSSOP 20-pin (173 mil)
TM57MA29NE-MTP-B6	QFN 20-pin (3x3x0.75-0.4mm)

SOT23-6 Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.45	-	-	0.057
A1	0	0.08	0.15	0	0.003	0.006
A2	0.90	1.10	1.30	0.035	0.043	0.051
A3	0.60	0.65	0.70	0.024	0.026	0.028
c	0.12	0.16	0.19	0.005	0.006	0.007
D	2.82	2.92	3.02	0.111	0.115	0.119
E	2.70	2.90	3.10	0.106	0.114	0.122
E1	1.52	1.62	1.72	0.060	0.064	0.068
e	0.85	0.95	1.05	0.033	0.037	0.041
e1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.35	0.48	0.60	0.014	0.019	0.024
θ	0°	4°	8°	0°	4°	8°
JEDEC	M0-178 (AB)					

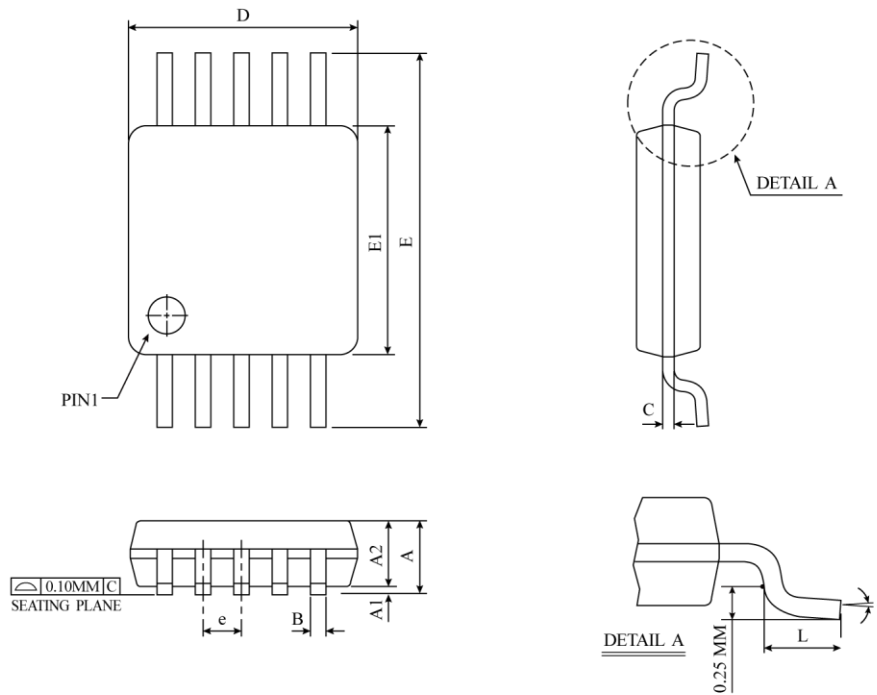
△ *NOTES : ALL DIMENSIONS REFER TO JEDEC STANDARD MO-178 AB
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

SOP-8 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	4.80	4.90	5.00	0.1890	0.1939	0.1988
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AA)					

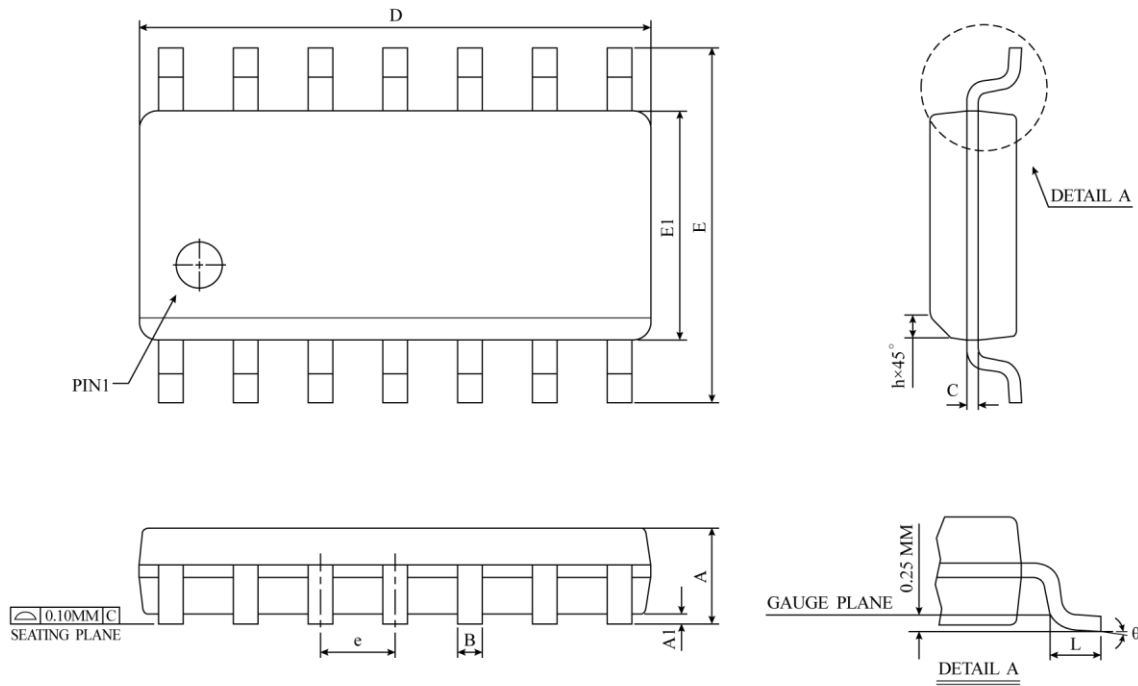
△ *NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

MSOP-10 (118mil) Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.81	0.96	1.10	0.032	0.038	0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.75	0.85	0.95	0.030	0.034	0.037
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	0.50 BSC			0.020 BSC		
L	0.40	0.55	0.70	0.016	0.022	0.028
θ	0°	3°	6°	0°	3°	6°
JEDEC						

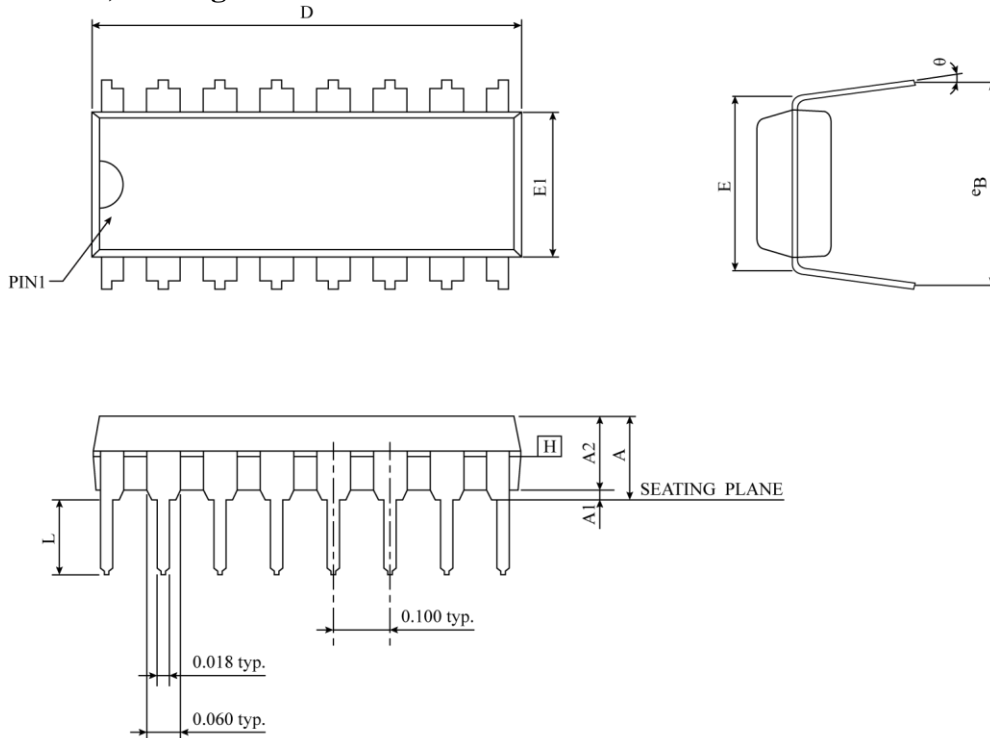
▲ *NOTES : DIMENSION "D" DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.
 MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.12 MM (0.005 INCH) PER SIDE.
 DIMENSION "E1" DOES NOT INCLUDE MOLD PROTRUSIONS
 MOLD PROTRUSIONS SHALL NOT EXCEED 0.25 MM (0.010 INCH) PER SIDE.

SOP-14 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	8.55	8.65	8.75	0.3367	0.3410	0.3444
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AB)					

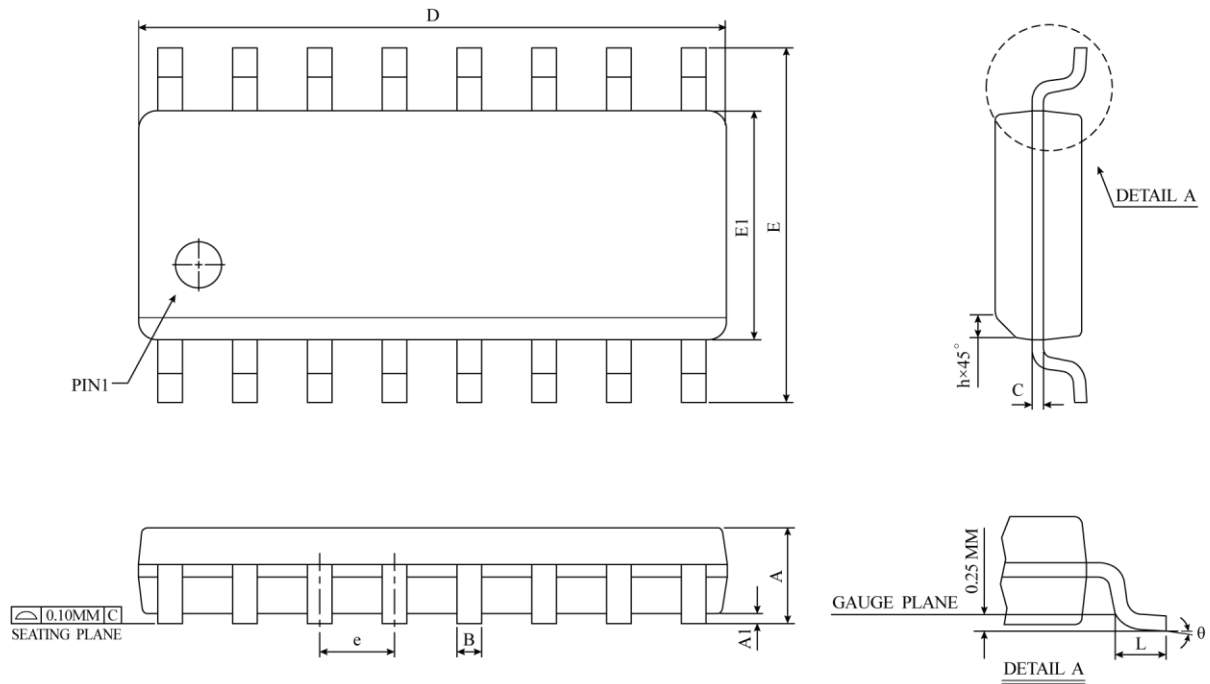
△ * NOTES : DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

DIP-16 (300mil) Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	4.369	-	-	0.172
A1	0.381	0.673	0.965	0.015	0.027	0.038
A2	3.175	3.302	3.429	0.125	0.130	0.135
D	18.669	19.177	19.685	0.735	0.755	0.775
E	7.620 BSC			0.300 BSC		
E1	6.223	6.350	6.477	0.245	0.250	0.255
L	2.921	3.366	3.810	0.115	0.133	0.150
eB	8.509	9.017	9.525	0.335	0.355	0.375
θ	0°	7.5°	15°	0°	7.5°	15°
JEDEC	MS-001 (BB)					

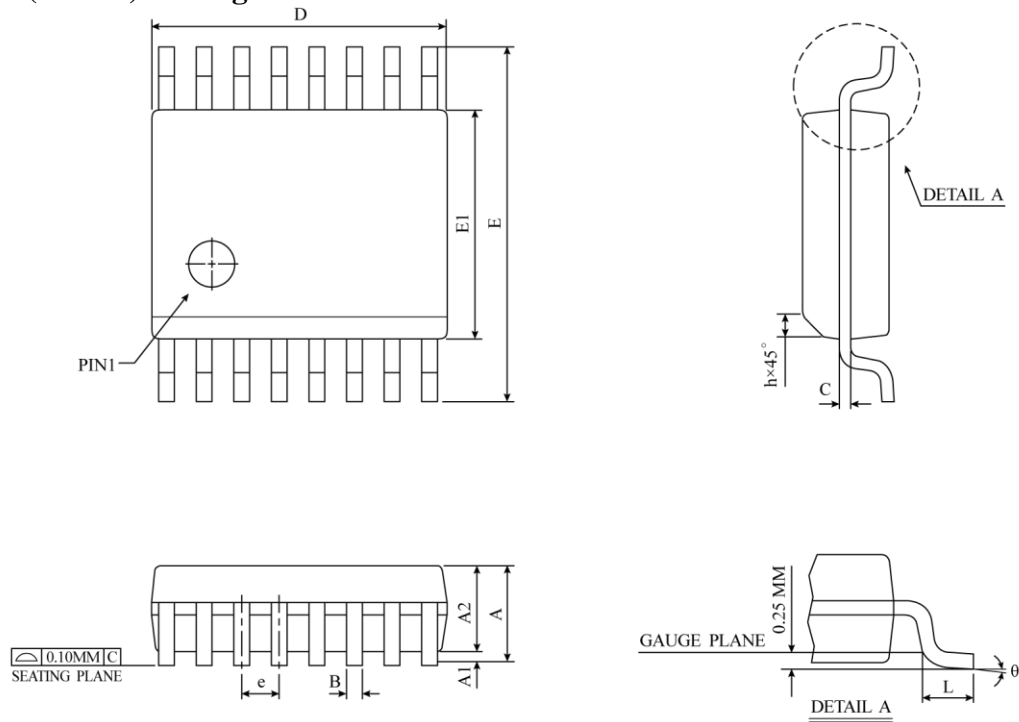
NOTES :

- "D", "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
- eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
- POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
- DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
- DATUM PLANE \square COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

SOP-16 (150 mil) Package Dimension


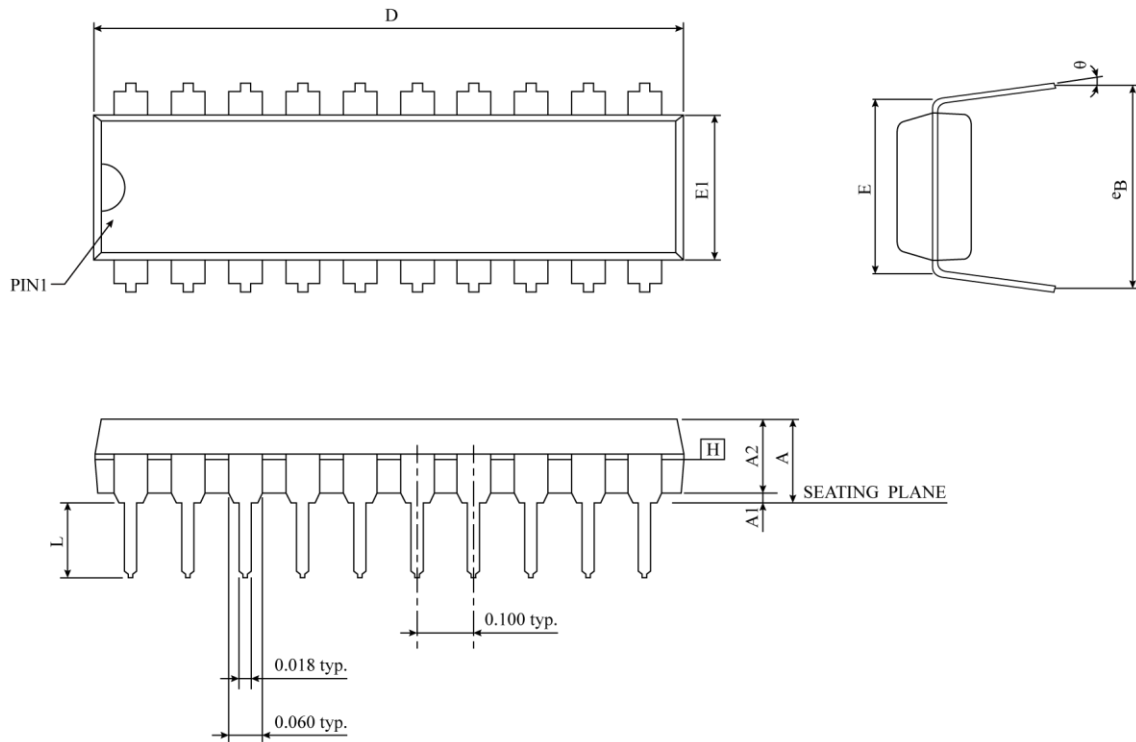
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	9.80	9.90	10.00	0.3859	0.3898	0.3937
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AC)					

△ *NOTES : DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

SSOP-16 (150mil) Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.18	0.25	0.004	0.007	0.010
A2	-	-	1.50	-	-	0.059
B	0.20	0.25	0.30	0.008	0.010	0.012
C	0.18	0.22	0.25	0.007	0.009	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.79	6.00	6.20	0.228	0.236	0.244
E1	3.81	3.90	3.99	0.150	0.154	0.157
e	0.635 BSC			0.025 BSC		
L	0.41	0.84	1.27	0.016	0.033	0.050
θ	0°	4°	8°	0°	4°	8°
JEDEC	M0-137 (AB)					

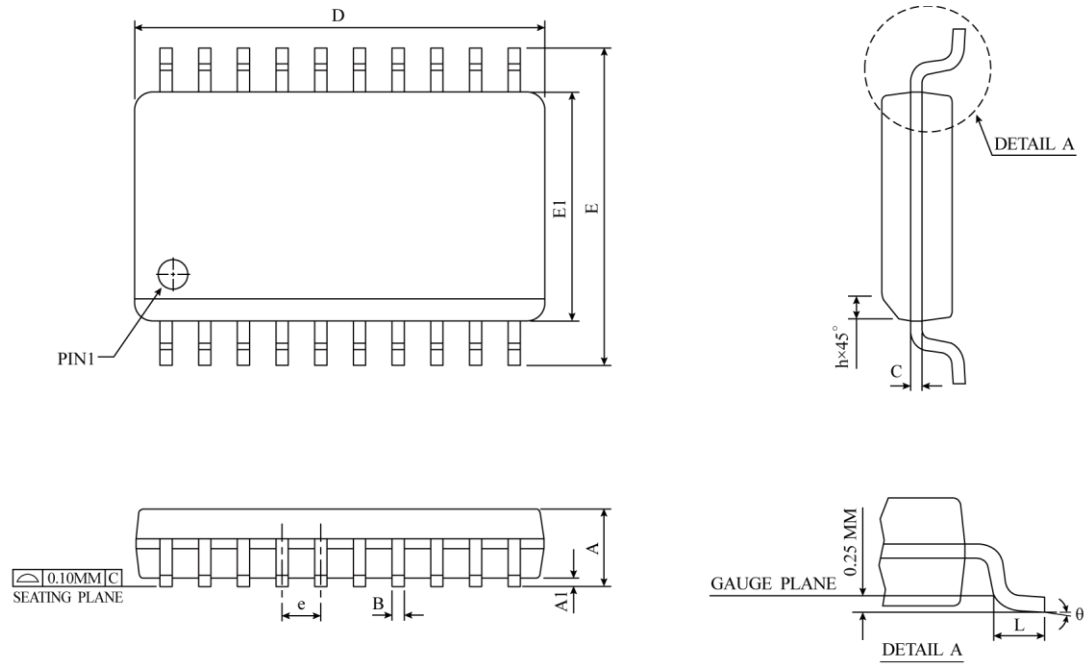
⚠ * NOTES : DIMENSION "D" DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS,
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT
EXCEED 0.15 MM (0.006 INCH) PER SIDE.

DIP-20 (300mil) Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	4.445	-	-	0.175
A1	0.381	-	-	0.015	-	-
A2	3.175	3.302	3.429	0.125	0.130	0.135
D	25.705	26.061	26.416	1.012	1.026	1.040
E	7.620	7.747	7.874	0.300	0.305	0.310
E1	6.223	6.350	6.477	0.245	0.250	0.255
L	3.048	3.302	3.556	0.120	0.130	0.140
eB	8.509	9.017	9.525	0.335	0.355	0.375
θ	0°	7.5°	15°	0°	7.5°	15°
JEDEC	MS-001 (AD)					

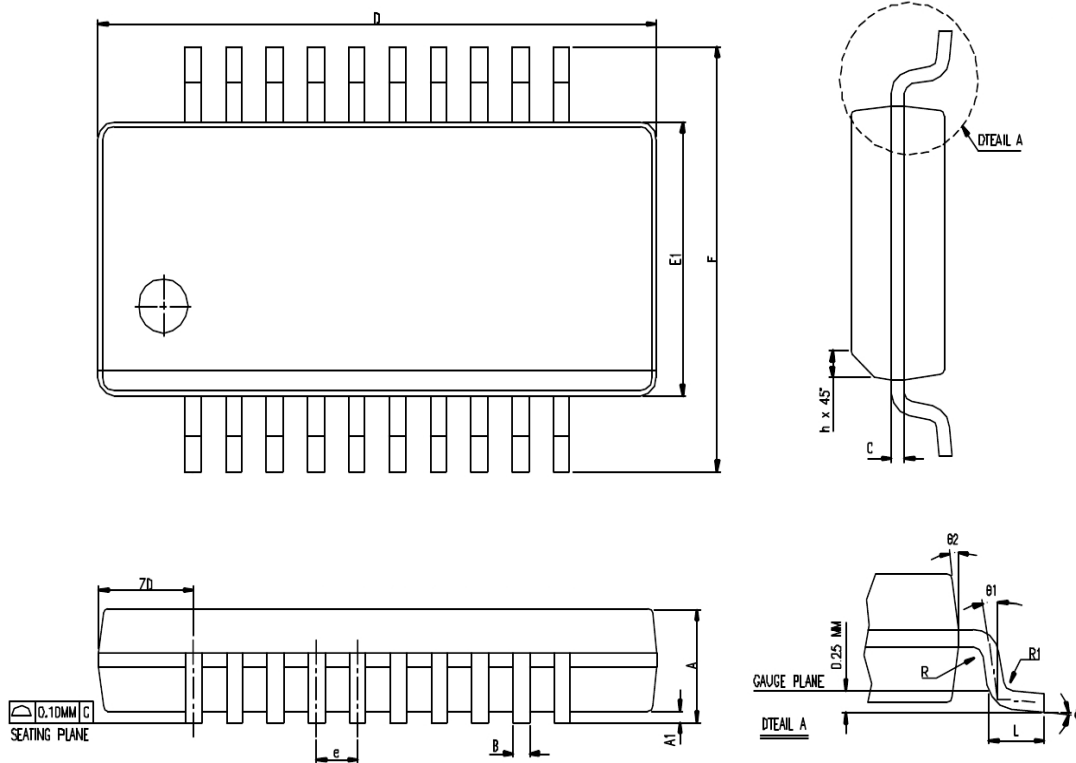
NOTES :

1. "D", "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
2. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
3. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
4. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
5. DATUM PLANE \square COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

SOP20 (300mil) Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	12.60	12.80	13.00	0.4961	0.5040	0.5118
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AC)					

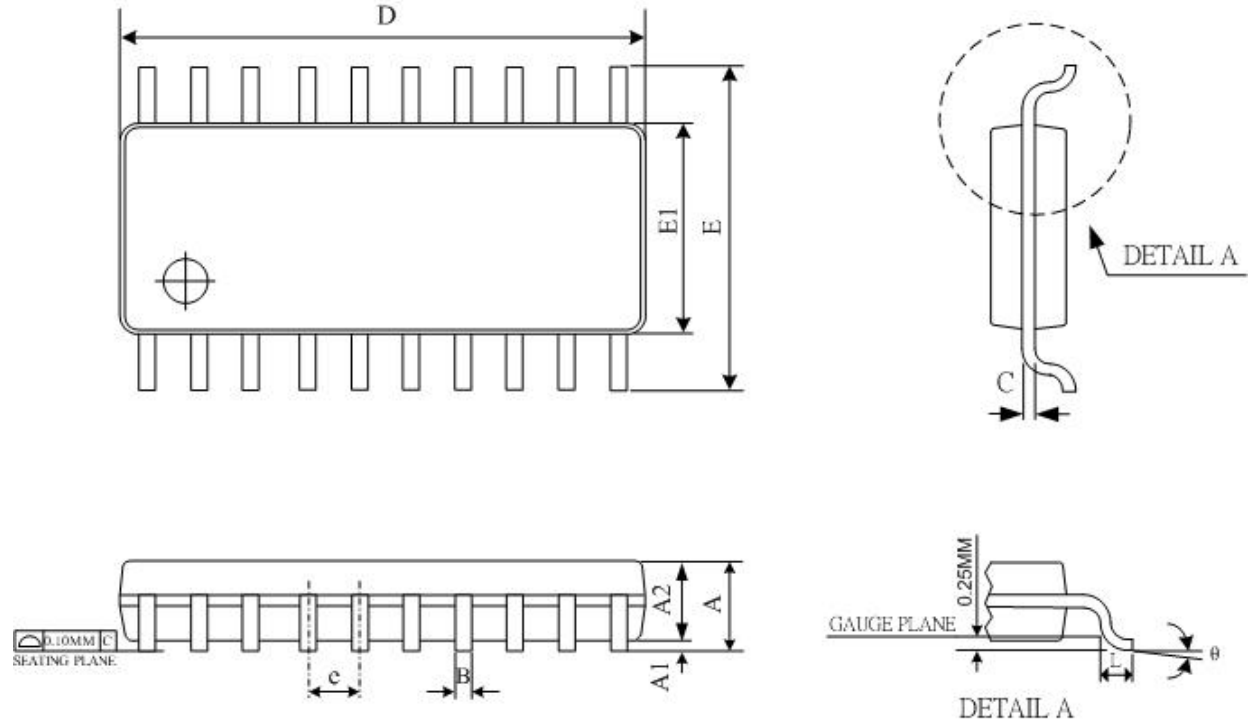
△ *NOTES : DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

SSOP-20 (150mil) Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	-	-	1.50	-	-	0.059
B	0.20	-	0.30	0.008	-	0.012
C	0.18	-	0.25	0.007	-	0.010
e	0.635 BASIC			0.025 BASIC		
D	8.56	8.66	8.74	0.337	0.341	0.344
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25	-	0.50	0.010	-	0.020
ZD	1.4732 REF.			0.058 REF.		
R1	0.20	-	0.33	0.008	-	0.013
R	0.20	-	-	0.008	-	-
θ	0°	-	8°	0°	-	8°
θ1	0°	-	-	0°	-	-
θ2	5°	10°	15°	5°	10°	15°
JEDEC	M0-137(AD)					

Δ *NOTES : DIMENSION “D” DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE.

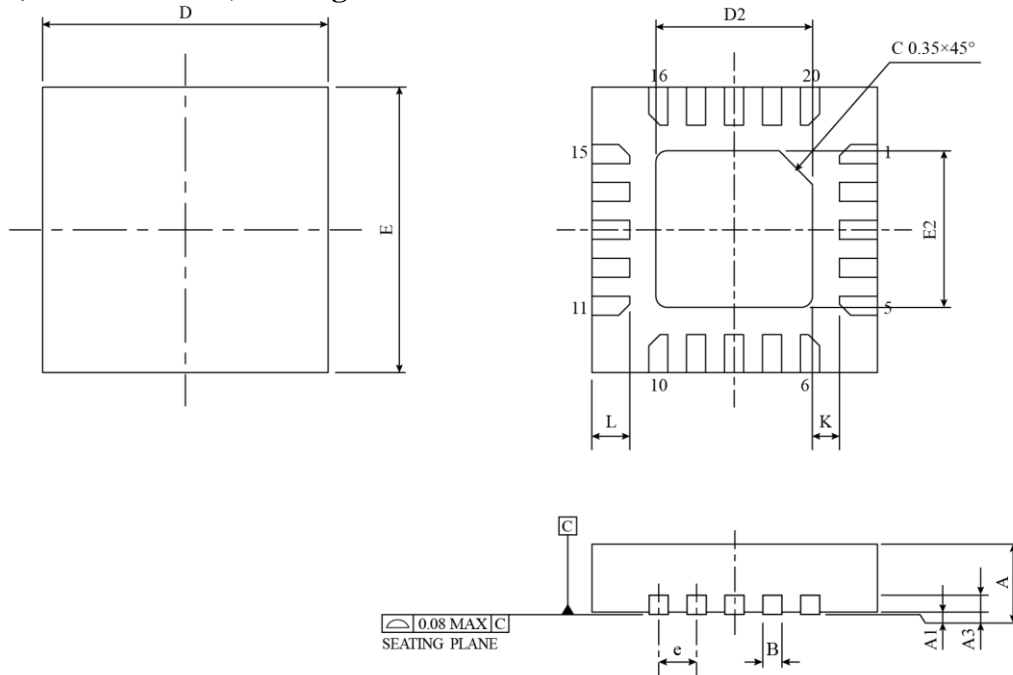
TSSOP-20 (173mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.2	-	-	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.8	0.93	1.05	0.031	0.036	0.041
B	0.19	-	0.3	0.007	-	0.012
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.55	0.246	0.252	0.258
E1	4.3	4.4	4.5	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0 °		8 °	0 °		8 °
JEDEC	MO-153 AC REV.F					

Notes :

- 1.DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
- 2.DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION, INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
- 3.DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08MM TOTAL IN EXCESS OF THE "B" DIMENSION AT MAXIMUM METERIAL CONDITION, DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07MM.

QFN-20 (3x3x0.75-0.4mm) Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF.			0.008 REF.		
B	0.15	0.20	0.25	0.006	0.008	0.010
D	3.00 BSC			0.118 BSC		
E	3.00 BSC			0.118 BSC		
e	0.40 BSC			0.016 BSC		
K	0.20	-	-	0.008	-	-
E2	1.60	1.65	1.70	0.063	0.065	0.067
D2	1.60	1.65	1.70	0.063	0.065	0.067
L	0.30	0.40	0.50	0.012	0.016	0.020
JEDEC						

- △ *NOTES : 1. ALL DIMENSION ARE IN MILLIMETERS.
 2. DIMENSION B APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP.
 IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
 3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.