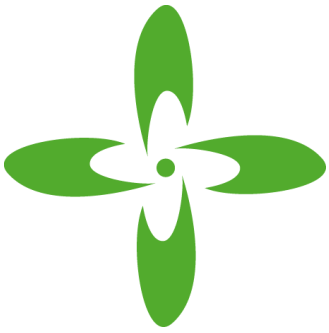

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TM52F4974

DATA SHEET Rev 1.1

(Please read the precautions on the second page before use)

PRECAUTIONS

1. Chip cannot enter Halt/Stop Mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0~2)
2. SFR.LVRCON (E3h) need to be set first when power on.
3. If TKPD=0, F/W must assign TK0 as a TK pin.

AMENDMENT HISTORY

Version	Date	Description
V1.0	Jun, 2024	New Release
V1.1	Aug, 2024	1. Modify the package of ordering number. 2. Added ADC and TK conversion current. 3. Some error correction.

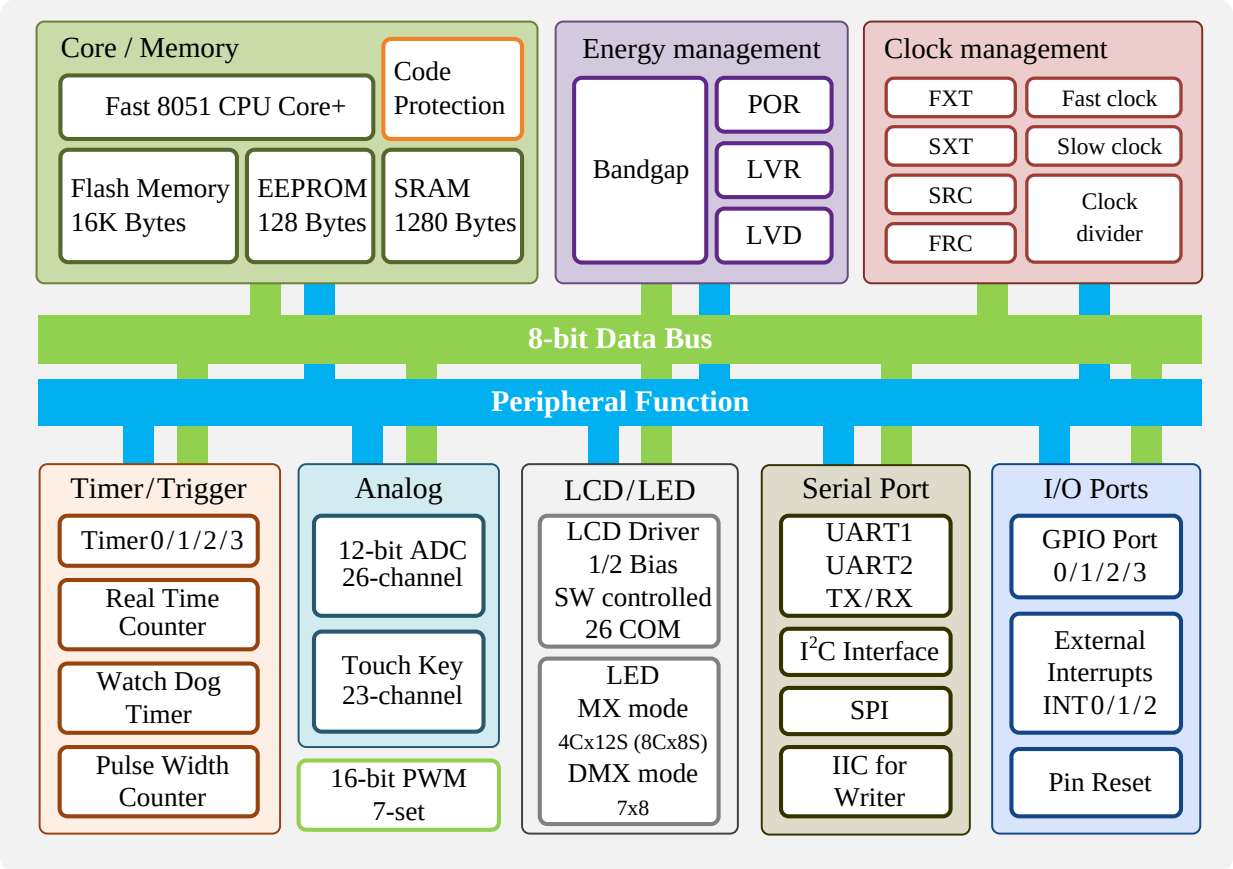
CONTENTS

GENERAL DESCRIPTION

TM52 $_{\text{series}}$ **F4974** are versions of a new, fast 8051 architecture for an 8-bit microcontroller single chip with an instruction set fully compatible with industry standard 8051, and retains most 8051 peripheral's functional block. Typically, the **TM52** executes instructions six times faster than the standard 8051 architecture.

The **TM52-F4974** provides improved performance, lower cost and fast time-to-market by integrating features on the chip, including 16K Bytes Flash program memory, 128 Bytes EEPROM, 1280 Bytes SRAM, Low Voltage Reset (LVR), Low Voltage Detector (LVD), dual clock power saving operation mode, 8051 standard UART and Timer0/1/2, real time clock Timer3, LCD/LED driver, 7 sets 16-bit PWMs, 26 channels 12-bit A/D Convertor, 23 channels Touch Key, I^2C interface, SPI interface and Watch Dog Timer. It's a high reliability and low power consumption feature can be widely applied in consumer and home appliance products.

TM52$_{\text{series}}$ F4974



FEATURES

1. **Standard 8051 Instruction set, fast machine cycle**
   - Executes instructions six times faster than the standard 8051.
2. **Flash Program Memory**
   - 16K Bytes Flash program memory
   - Support “In Circuit Programming” (ICP) or “In System Programming” (ISP) for the Flash code
   - Byte Write “In Application Programming” (IAP) mode is convenient as Data EEPROM access
   - Code Protection Capability
   - 10K erase times at least
   - 10 years data retention at least
3. **128 Bytes EEPROM Memory**
   - 50K erase times at least
   - 10 years data retention at least
4. **Total 1536 Bytes SRAM (IRAM + XRAM)**
   - 256 Bytes IRAM in the 8051 internal data memory area
   - 1280 Bytes XRAM in the 8051 external data memory area (accessed by MOVX Instruction)
5. **Four System Clock type selections**
   - Fast clock from 1~18MHz Crystal (FXT)
   - Fast clock from Internal RC (FRC, 18.432 MHz)
   - Slow clock from 32768Hz Crystal (SXT)
   - Slow clock from Internal RC (SRC, 41 KHz)
   - System Clock can be divided by 1/2/4/16 option
6. **8051 Standard Timer – Timer0/1/2**
   - 16-bit Timer0, also supports T0O clock output for Buzzer application
   - 16-bit Timer1, also supports T1O clock output for Buzzer application
   - 16-bit Timer2, also supports T2O clock output for Buzzer application
7. **24-bit Timer3**
   - Clock source is Slow clock or FRC/512
   - with reload function
   - with clear and hold function
8. **UARTs**
   - UART1, 8051 standard UART
   - UART2, the second UART, supports only Mode1 and Mode3
   - Additional Baud Rate generator option
   - With UART pin select option

9. Seven 16-bit PWMs

【16-bit PWM0 P+N】

- with period-adjustment/buffer-reload/clear and hold function
- Non-overlap durations adjustable
- Half-bridge phase control output
- FRC * 2 (36MHz), FRC (18MHz) or system clock source selectable

【16-bit PWM1~6】

- share period
- with period-adjustment/buffer-reload/clear and hold function
- FRC * 2 (36MHz), FRC (18MHz) or system clock source selectable

10. I^2C interface (Master / Slave)

- with I^2C pin select option

11. SPI interface

- Master or Slave mode selectable
- Programmable transmit bit rate
- Serial clock phase and polarity options
- MSB-first or LSB-first selectable

12. 12-bit ADC with 26 channels External Pin Input and 2 channels Internal Reference Voltage

- Internal Reference Voltage: V_{BG}, $1/4V_{CC}$
- ADC reference voltage: V_{BG} / V_{CC}

13. 23-Channel Touch Key (FTK)

- Internal reference key
- With 4 scanning methods

14. LCD Driver

- Software controlled COM00~07, COM10~17, COM20~21, COM30~37 (Max. 26 pins)
- 1/2 LCD Bias

15. LED Controller/Driver

- COM with Dead Time
- 8-level Brightness selection
- Brightness uniform / enhancement option

【Matrix (MX) mode】

- 4Cx12S ~ 8Cx8S selectable, Max. 16 pins up to 48~64 dots

【Dot matrix (DMX) mode】

- 4Cx4S, 5Cx5S, 6Cx6S, 6Cx7S, 7Cx7S, 7Cx8S, Max. 8 pins up to 56 dots

16. 14 Sources, 4-level priority Interrupt

- Timer0/Timer1/Timer2/Timer3 Interrupt
- INT0/INT1 pin Falling-Edge/Low-Level Interrupt
- INT2 pin Falling-Edge Interrupt
- Port0/1/2/3 Pin Change Interrupt
- UART1 TX/RX Interrupt
- UART2 TX/RX Interrupt
- ADC/Touch Key Interrupt
- I^2C/SPI interrupt
- LVD Interrupt
- PWM0/PWM1 Interrupt

17. Pin Interrupt can Wake up CPU from Halt/Stop mode

- P3.2/P3.3 (INT0/INT1) Interrupt & Wake-up
- P3.7 (INT2) Interrupt & Wake-up
- Each Port0/1/2/3 pin can be defined as Interrupt & Wake-up pin (by pin change)

Note: *Chip cannot enter Halt/Stop mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0~2)*

18. Max. 26 Programmable I/O pins

- CMOS Output
- Pseudo-Open-Drain, or Open-Drain Output
- Schmitt Trigger Input
- Pin Pull-up can be Enabled or Disabled
- All pin with High sink option (80mA@V_{CC}=5V， V_{OL}=0.1V_{CC})

19. Independent RC Oscillating Watch Dog Timer

- 400ms/200ms/100ms/50ms selectable WDT timeout options

20. Five types Reset

- Power on Reset
- Selectable External Pin Reset
- Selectable Watch Dog Reset
- Software Command Reset
- Selectable Low Voltage Reset

21. 16-level Low Voltage Reset (LVR)

- 2.05V/2.19V/2.33V/2.47V/2.61V/2.75V/2.89V/3.03V/ 3.17V/3.31V/3.45V/3.59V/3.73V/3.87V/4.01V/4.15V (step=0.14V)

22. 16-level Low Voltage Detect (LVD)

- 2.05V/2.19V/2.33V/2.47V/2.61V/2.75V/2.89V/3.03V/ 3.17V/3.31V/3.45V/3.59V/3.73V/3.87V/4.01V/4.15V (step=0.14V)
- LVD detect polarity option
- LVD Hysteresis 30mV~80mV

23. Five Power Operation Modes

- Fast/Slow/Idle/Halt/Stop mode

24. Integrated 16-bit Cyclic Redundancy Check function

25. Multiplication and Division

- 8 bits Multiplier & Divider (standard 8051)
- 16 bits Multiplier & Divider
- 32 bits ÷ 16 bits Divider

26. On-chip Debug/ICE interface

- Use P3.0/P3.1 pin or P0.0/P0.1 pin
- Share with ICP programming pin
- Mass production writer only supports P3.0/P3.1

27. Operating Voltage and Current

- V_{CC} = 2.2V ~ 5.5V @F_{SYSCLK}=18.432MHz (-40℃ ~ +105℃)
- I_{CC} = 0.2μA @Stop mode, PWRSAV=1, V_{CC}=3V
- I_{CC} = 2.4μA @Halt mode, PWRSAV=1, V_{CC}=3V
- I_{CC} = 3.6μA @Idle mode, PWRSAV=1, PORPD=1, V_{CC}=3V

28. Operating Temperature Range

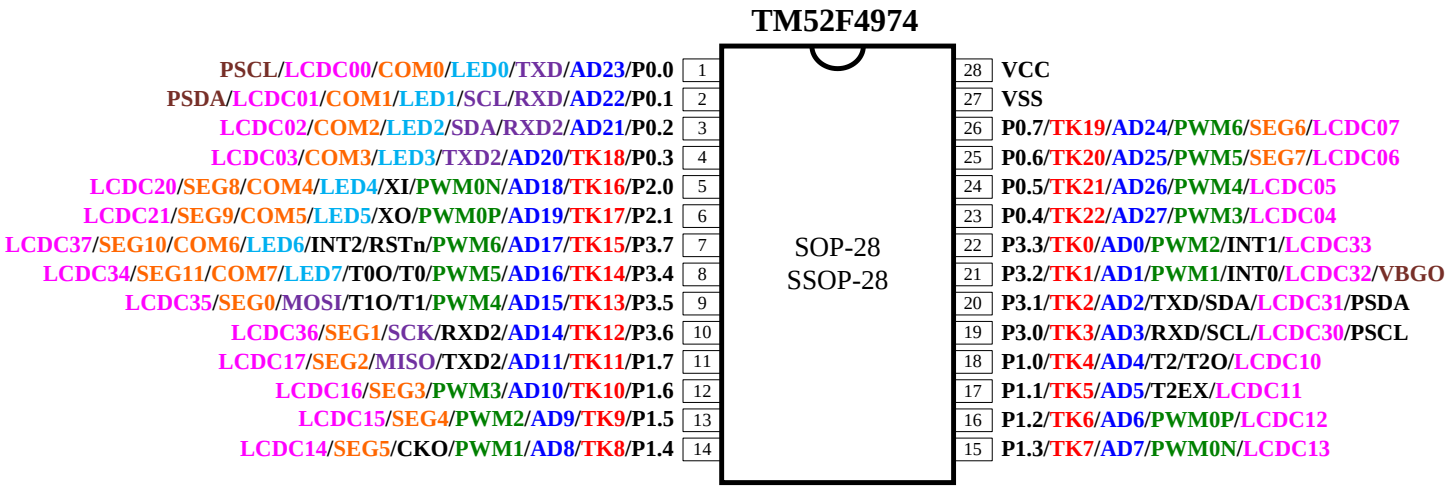
- –40℃ ~ +105℃

29. Package Types

- 28-pin SOP (300 mil)
- 28-pin SSOP (150 mil)
- 20-pin SOP (300 mil)
- 16-pin SOP (150 mil)

PIN ASSIGNMENT

TM52F4974



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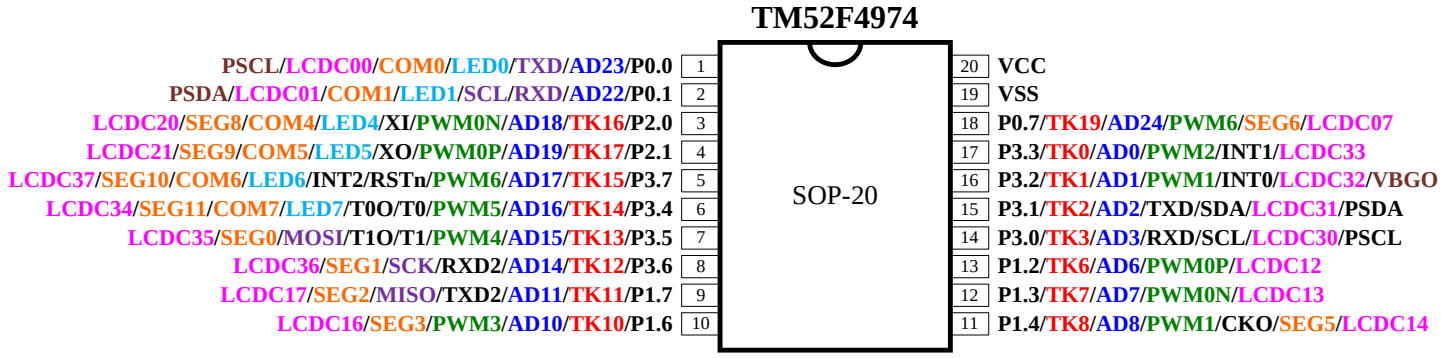

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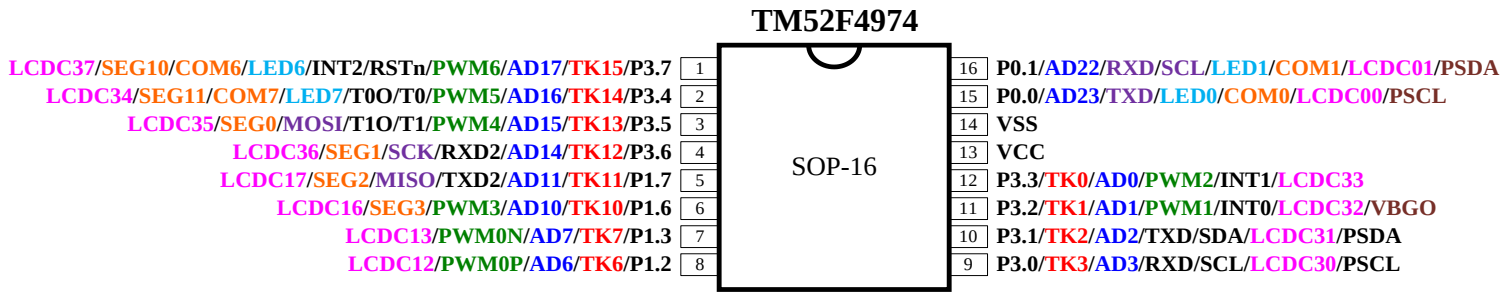


PIN DESCRIPTION

Name	In/Out	Pin Description
P0.0~P0.7 P1.0~P1.7 P2.0~P2.1 P3.3~P3.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software. These pin's level change can interrupt/wake up CPU from Idle/Halt/Stop mode.
P3.0~P3.2	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "**pseudo open drain**" output. Pull-up resistors are assignable by software. These pin's level change can interrupt/wake up CPU from Idle/Halt/Stop mode.
INT0, INT1	I	External low level or falling edge Interrupt input, Idle/Halt/Stop mode wake up input.
INT2	I	External falling edge Interrupt input, Idle/Halt/Stop mode wake up input.
RXD	I/O	UART1 Mode0 transmit & receive data, Mode1/2/3 receive data
RXD2	I/O	UART2 Mode1/3 receive data
TXD	I/O	UART1 Mode0 transmit clock, Mode1/2/3 transmit data.
TXD2	I/O	UART2 Mode1/3 transmit data.
T0, T1, T2	I	Timer0, Timer1, Timer2 event count pin input.
T2EX	I	Timer2 external trigger input.
T0O	O	Timer0 overflow divided by 64 output
T1O	O	Timer1 overflow divided by 2 output
T2O	O	Timer2 overflow divided by 2 output
CKO	O	System Clock divided by 2 output
VBGO	O	Bandgap voltage output
PWM1~PWM6 PWM0P/PWM0N	O	16 bit PWM output
AD0~AD11, AD14~AD27	I	ADC input
TK0~TK22	I	Touch Key input
LCD00~LCD07 LCD10~LCD17 LCD20~LCD21 LCD30~LCD37	O	LCD 1/2 bias output
COM0~COM7	O	LED Matrix mode common output
SEG0~SEG11	O	LED Matrix mode segment output
LED0~LED7	O	LED Dot matrix mode output
SCK	I/O	SPI clock output for master or clock input for slave mode
MISO	I/O	SPI data input for master mode, data output for slave mode
MOSI	I/O	SPI data output for master mode, data input for slave mode
SCL	I/O	I^2C SCL
SDA	I/O	I^2C SDA
PSCL	I/O	I^2C SCL for program
PSDA	I/O	I^2C SDA for program
RSTn	I	External active low reset input, Pull-up resistor is fixed enable.
XI, XO	–	Crystal/Resonator oscillator connection for System clock (FXT or SXT)
VCC, VSS	P	Power input pin and ground

PIN SUMMERY

Pin # SOP-28	Pin Name	Type	Initial State	Input			Output			Alternative Function								MISC
				Pull-up Control	Wake up	Ext. Interrupt	CMOS Push-Pull	Pseudo Open Drain	Open Drain	LCD	LED MX mode	LED DMX mode	ADC	Touch Key	PWM	Timer	I^2C / SPI / UART	
1	PSCL/LCDC00/COM0/LED0/TXD/AD23/P0.0	I/O	Hi-Z	●	●	●	●		●	●	●	●	●				●	PSDL
2	PSDA/LCDC01/COM1/LED1/SCL/RXD/AD22/P0.1	I/O	Hi-Z	●	●	●	●		●	●	●	●	●				●	PSDA
3	LCDC02/COM2/LED2/SDA/RXD2/AD21/P0.2	I/O	Hi-Z	●	●	●	●		●	●	●	●	●				●	
4	LCDC03/COM3/LED3/TXD2/AD20/TK18/P0.3	I/O	Hi-Z	●	●	●	●		●	●	●	●	●	●			●	
5	LCDC20/SEG8/COM4/LED4/XI/PWM0N/AD18/TK16/P2.0	I/O	Hi-Z	●	●	●	●		●	●	●	●	●	●	●			Crystal
6	LCDC21/SEG9/COM5/LED5/XO/PWM0P/AD19/TK17/P2.1	I/O	Hi-Z	●	●	●	●		●	●	●	●	●	●	●			Crystal
7	LCDC37/SEG10/COM6/LED6/INT2/RSTn/PWM6/AD17/TK15/P3.7	I/O	Hi-Z	●	●	●	●		●	●	●	●	●	●	●			Reset
8	LCDC34/SEG11/COM7/LED7/T0O/T0/PWM5/AD16/TK14/P3.4	I/O	Hi-Z	●	●	●	●		●	●	●	●	●	●	●	●		T0O
9	LCDC35/SEG0/MOSI/T1O/T1/PWM4/AD15/TK13/P3.5	I/O	Hi-Z	●	●	●	●		●	●	●		●	●	●	●	●	T1O
10	LCDC36/SEG1/SCK/RXD2/AD14/TK12/P3.6	I/O	Hi-Z	●	●	●	●		●	●	●		●	●			●	
11	LCDC17/SEG2/MISO/TXD2/AD11/TK11/P1.7	I/O	Hi-Z	●	●	●	●		●	●	●		●	●			●	
12	LCDC16/SEG3/PWM3/AD10/TK10/P1.6	I/O	Hi-Z	●	●	●	●		●	●	●		●	●	●			
13	LCDC15/SEG4/PWM2/AD9/TK9/P1.5	I/O	Hi-Z	●	●	●	●		●	●	●		●	●	●			
14	LCDC14/SEG5/CKO/PWM1/AD8/TK8/P1.4	I/O	Hi-Z	●	●	●	●		●	●	●		●	●	●			CKO
15	LCDC13/PWM0N/AD7/TK7/P1.3	I/O	Hi-Z	●	●	●	●		●	●			●	●	●			
16	LCDC12/PWM0P/AD6/TK6/P1.2	I/O	Hi-Z	●	●	●	●		●	●			●	●	●			
17	LCDC11/T2EX/AD5/TK5/P1.1	I/O	Hi-Z	●	●	●	●		●	●			●	●		●		
18	LCDC10/T2O/T2/AD4/TK4/P1.0	I/O	Hi-Z	●	●	●	●		●	●			●	●		●		T2O
19	PSCL/LCDC30/SCL/RXD/AD3/TK3/P3.0	I/O	Hi-Z	●	●	●	●	●	●	●			●	●			●	PSCL
20	PSDA/LCDC31/SDA/TXD/AD2/TK2/P3.1	I/O	Hi-Z	●	●	●	●	●	●	●			●	●			●	PSDA
21	VBGO/LCDC32/INT0/PWM1/AD1/TK1/P3.2	I/O	Hi-Z	●	●	●	●	●	●	●			●	●	●			VBGO
22	LCDC33/INT1/PWM2/AD0/TK0/P3.3	I/O	Hi-Z	●	●	●	●		●	●			●	●	●			
23	LCDC04/PWM3/AD27/TK22/P0.4	I/O	Hi-Z	●	●	●	●		●	●			●	●	●			
24	LCDC05/PWM4/AD26/TK21/P0.5	I/O	Hi-Z	●	●	●	●		●	●			●	●	●			
25	LCDC06/SEG7/PWM5/AD25/TK20/P0.6	I/O	Hi-Z	●	●	●	●		●	●	●		●	●	●			
26	LCDC07/SEG6/PWM6/AD24/TK19/P0.7	I/O	Hi-Z	●	●	●	●		●	●	●		●	●	●			
27	VSS	P																
28	VCC	P																

FUNCTIONAL DESCRIPTION

1. CPU Core

In the 8051 architecture, the C programming language is used as a development platform. The TM52 device features a fast 8051 core in a highly integrated microcontroller, allowing designers to be able to achieve improved performance compared to a classic 8051 device. TM52 series microcontrollers provide a complete binary code with standard 8051 instruction set compatibility, ensuring an easy migration path to accelerate the development speed of system products. The CPU core includes an ALU, a program status word (PSW), an accumulator (ACC), a B register, a stack point (SP), DPTRs, a program counter, an instruction decoder, and core special function registers (SFRs).

1.1 Accumulator (ACC)

This register provides one of the operands for most ALU operations. Accumulators are generally referred to as A or Acc and sometimes referred to as Register A. In this document, the accumulator is represented as “A” or “ACC” including the instruction table. The accumulator, as its name suggests, is used as a general register to accumulate the intermediate results of a large number of instructions. The accumulator is the most important and frequently used register to complete arithmetic and logical operations. It holds the intermediate results of most arithmetic and logic operations and assists in data transportation.

SFR **E0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E0h.7~0 **ACC:** Accumulator

1.2 B Register (B)

The “B” register is very similar to the ACC and may hold a 1 Byte value. This register provides the second operand for multiply or divide instructions. Otherwise, it may be used as a scratch pad register. The B register is only used by two 8051 instructions, MUL and DIV. When A is to be multiplied or divided by another number, the other number is stored in B. For MUL and DIV instructions, it is necessary that the two operands are in A and B.

ex: DIV AB

When this instruction is executed, data inside A and B are divided, and the answer is stored in A.

SFR **F0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0h.7~0 **B:** B register

1.3 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the Stack Pointer.

SFR **81h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP	SP							
R/W	R/W							
Reset	0	0	0	0	0	1	1	1

81h.7~0 **SP:** Stack Point

1.4 Dual Data Pointer (DPTRs)

TM52 device has two DPTRs, which share the same SFR address. Each DPTR is 16 bits in size and consists of two registers: the DPTR high byte (DPH) and the DPTR low byte (DPL). The DPTR is used for 16-bit-address external memory accesses, for offset code byte fetches, and for offset program jumps. Setting the DPSEL control bit allows the program code to switch between the two physical DPTRs.

SFR **82h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

82h.7~0 **DPL:** Data Point low byte

SFR **83h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	DPH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

83h.7~0 **DPH:** Data Point high byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W
Reset	0	0	0	0	1	1	–	0

F8h.0 **DPSEL:** Active DPTR Select

1.5 Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operations. The instructions that affect the PSW are listed below.

Instruction	Flag		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		

Instruction	Flag		
	C	OV	AC
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
ORL C, /bit	X		
MOV C, bit	X		
CJNE	X		

A “0” means the flag is always cleared, a “1” means the flag is always set and an “X” means that the state of the flag depends on the result of the operation.

SFR **D0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D0h.7 **CY:** ALU carry flag

D0h.6 **AC:** ALU auxiliary carry flag

D0h.5 **F0:** General purpose user-definable flag

D0h.4~3 **RS1, RS0:** The contents of (RS1, RS0) enable the working register banks as:
- 00: Bank 0 (00h~07h)
- 01: Bank 1 (08h~0Fh)
- 10: Bank 2 (10h~17h)
- 11: Bank 3 (18h~1Fh)

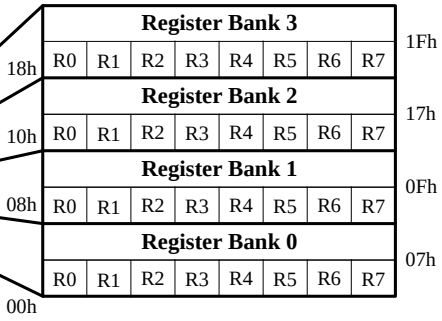
D0h.2 **OV:** ALU overflow flag

D0h.1 **F1:** General purpose user-definable flag

D0h.0 **P:** Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of “one” bits in the accumulator.

PSW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CY	**AC**	**FO**	**RS1**	**RS0**	**OV**	**F1**	**P**

RS1	RS0	Bank
1	1	3
1	0	2
0	1	1
0	0	0



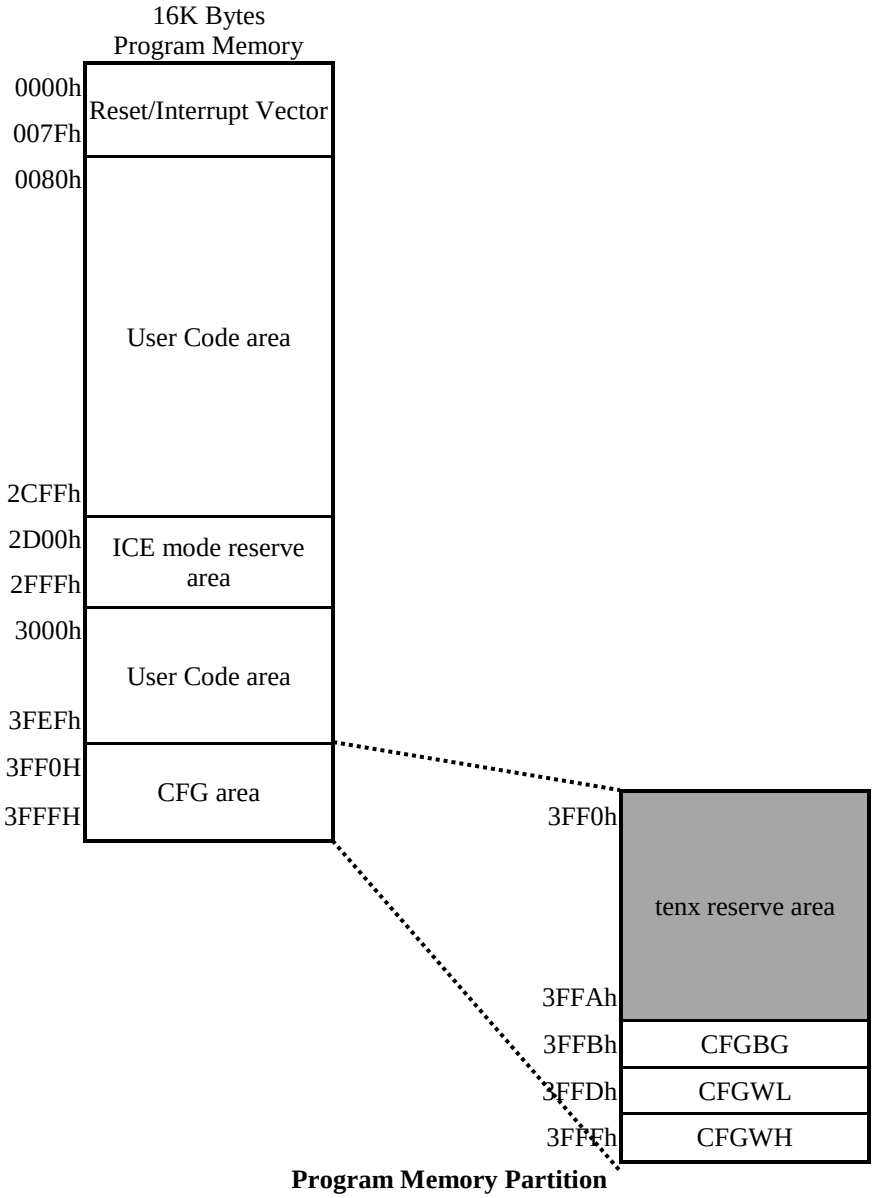
2. Memory

2.1 Program Memory

The Chip has a 16K Bytes Flash program memory which can support In Circuit Programming (ICP), In Application Programming (IAP) and In System Programming (ISP) function modes. The Flash write endurance is at least 10K cycles. The program memory address continuous space (0000h~3FFFh) is partitioned to several sectors for device operation.

2.1.1 Program Memory Functional Partition

The last 16 bytes (3FF0h~3FFFh) of program memory is defined as chip Configuration Word (CFGW), which is loaded into the device control registers upon power on reset (POR). The 0000h~007Fh is occupied by Reset/Interrupt vectors as standard 8051 definition. In the in-circuit emulation (ICE) mode, user also needs to reserve the address space 2D00h~2FFFh for ICE System communication. CRC16H/L is the reserved area of the checksum. Tenx can provide a CRC verification subroutine. The user can calculate the checksum by the CRC verification subroutine to compare with CRC16H/L and check the validity of the ROM code.



Program Memory Partition

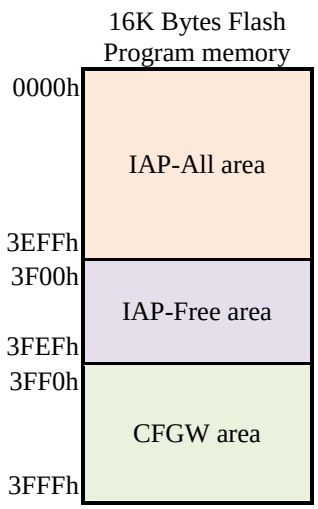
2.1.2 Flash ICP Mode

The Flash memory can be programmed by the tenx proprietary writer **(TWR99/TWR100)**, which needs at least four wires (VCC, VSS, P3.0 and P3.1) to connect to this chip. If user wants to program the Flash memory on the target circuit board (In Circuit Program, ICP), these pins must be reserved sufficient freedom to be connected to the Writer.

Writer wire number	Pin connection
4-Wire	VCC, VSS, P3.0, P3.1

2.1.3 Flash IAP Mode

This chip has "In Application Program" (IAP) capability, which allows software to read/write data from/to the Flash memory during CPU run time as conveniently as data EEPROM access. The IAP function is byte writable, meaning that the chip does not need to erase one Flash page before write. The available IAP data space is 240 Bytes after chip reset, and can be re-defined by the "IAPALL" control register as shown below.



Flash memory	IAPALL	MOVC Accessible	MOVX (IAP) Accessible
0000h~3EFFh	0	Yes	No
	1	Yes	Yes
3F00h~3FEFh	X	Yes	Yes
3FF0h~3FF7h	X	Yes	Yes
3FF8h~3FFEh	0	Yes	No
	1	Yes	Yes
3FFFh	X	Yes	No

In IAP mode, the program Flash memory is separated into three sectors: IAP-All area, IAP-Free area, and CFGW area. These three sectors are regulated differently.

The **IAP-All area** is protected by the IAPALL register to prevent IAP mode from writing application data to the program area, resulting in a program code error that cannot be repaired. The size of this area is 16128 Bytes. Enabling IAPALL requires writing 65h to SFR SWCMD 97h to set the IAPALL control flag. Then, software can use MOVX instructions to write application data to flash memory from 0000h to 3EFFh. If user wants to disable IAPALL function, user can write other values to SFR SWCMD 97h to clear the IAPALL control flag. User must be careful not to overwrite program code which is already resided on the same Flash memory area.

The **IAP-Free area** has no control bit to protect. It can be used to reliably store system application data that needs to be programmed once or periodically during system operation. Other areas of Flash memory can be used to store data, but this area is usually better. The size of this area is 240 Bytes, equivalent to an EEPROM, and Flash memory can provide byte access to read and write commands. The chip has a physical 128 byte EEPROM memory. It has the wider writing voltage range and the better write endurance than Flash memory. It is recommended to use EEPROM memory to store application data first.

The **CFGW area** has 3 data bytes (CFGWH, CFGWL and CFGBG), which is located at the last 16 addresses of Flash memory. The CFGWH is not accessible to IAP, while the CFGWL and CFGBG can be read or written by IAP in case the IAPALL flag is set. CFGWL is copied to the SFR F6h and CFGBG is copied to the SFR F5h after power on reset, software then take over CFGWL's and CFGBG's control capability by modifying the SFR F6h and F5h.

2.1.4 IAP Mode Access Routines

Flash IAP Write is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target Flash address (0000h~3FFEh), and the ACC contains the data being written. The chip accepts IAP write command only when IAPWE=1. Flash IAP writing one byte requires approximately 1 ms @V_{CC}=5.0V. Meanwhile, the CPU stays in a waiting state, but all peripheral modules (Timers, LED, and others) continue running during the writing time. The software must handle the pending interrupts after an IAP write. The chip has a build-in IAP Time-out function for escaping write fail state. Flash IAP writing needs setting the system clock to FRC/2 (or slower) and V_{CC} >4.0V.

Because the Program memory and the IAP data space share the same entity, a **Flash IAP Read** can be performed by the "MOVX A, @DPTR" or "MOVC" instruction as long as the target address points to the 0000h~3FFEh area. A Flash IAP read does not require extra CPU wait time.

```
  ; IAP example code (ASM)
  ; need 4.0V < VCC < 5.5V
MOV     DPTR, #3F00h        ; DPTR=3F00h=target IAP address
MOV     A, #5Ah             ; A=5Ah=target IAP write data
MOV     IAPWE, #47h         ; IAP write enable
MOV     AUX2, #02h          ; IAP Time-Out function enable
MOVX    @DPTR, A            ; Flash[3F00h] =5Ah, after IAP write
                            ; 1ms~2ms H/W writing time, CPU wait
MOV     IAPWE, #00h         ; IAP write disable, immediately after IAP write
CLR     A                   ; A=0
MOVX    A, @DPTR            ; A=5Ah
CLR     A                   ; A=0
MOVC    A, @A+DPTR          ; A=5Ah
```

```
  ; IAP example code (C)
  ; need 4.0V < VCC < 5.5V
unsigned char xdata PROM[4096] _at_ 0x2000    // 0x2000 = start address
unsigned char code CODE[4096] _at_ 0x2000    // 0x2000 = start address

IAPALL = 0x65;
IAPWE = 0x47;
PROM[0x02] = wdata;    // write data into ROM[0x2002]
IAPWE = 0x00;
IAPALL = 0x00;

rdata = CODE[0x105];    // read data from ROM[0x2105]
```

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL/SWRST							
R/W	W							
Reset	–							

97h.7~0 **IAPALL (W):**
Write 65h to set IAPALL flag. Write other value to clear IAPALL flag.

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	–						WDTO	IAPALL
R/W	R						R	R
Reset	0						0	0

97h.0 **IAPALL (R):** Flag indicates Flash can be written by IAP or not
0: Flash IAP disable
1: Flash IAP enable

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPCON	IAPCON							
R/W	W							
Reset	–	–	–	–	–	–	–	–

C9h.7~0 **IAPCON (W):**
Write 47h or 74h to set IAPWE flag; Write 47h can write 1 byte at once, write 74h can write 2 bytes at once. Write other value to clear IAPWE flag. It is recommended to clear it immediately after IAP write.
Write A1h to set INFOWE flag; write other value to clear INFOWE flag. It is recommended to clear it immediately after IAP write.
Write E2h to set EEPWE flag; write other value to clear EEPWE flag. It is recommended to clear it immediately after EEPROM write.

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPCON	IAPWE	IAPTO	EEPWE	INFOWE	–	–	–	–
R/W	R	R	R	R	–	–	–	–
Reset	0	0	0	0	–	–	–	–

C9h.7 **IAPWE (R):** Flag indicates Flash memory can be written by IAP or not
0: IAP Write disable
1: IAP Write enable

C9h.6 **IAPTO (R):** Time-Out flag of IAP write/EEPROM write/INFO write. Set by H/W when IAP or EEPROM write or INFO write Time-out occurs. Cleared this flag by H/W when IAPWE=0 or EEPWE=0 or INFOWE=0.

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.2~1 **IAPTE:** IAP (or EEPROM) write watchdog timer enable
00: Disable
01: wait 3ms trigger watchdog time-out flag, and escape the write fail state
10: wait 6ms trigger watchdog time-out flag, and escape the write fail state
11: wait 25ms trigger watchdog time-out flag, and escape the write fail state

2.1.5 Flash ISP Mode

The “In System Programming” (ISP) usage is similar to IAP, except the purpose is to refresh the Program code. User can use UART/SPI or other method to get new Program code from external host, then writes code as the same way as IAP. ISP operation is complicated; basically it needs to assign a Boot code area to the Flash which does not change during the ISP process.

2.2 EEPROM Memory

This chip contains 128 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 50K write/erase cycles.

EEPROM Memory

EE00h	EEPROM[0]
EE02h	EEPROM[1]
EE04h	. . .
EEFCh	EEPROM[126]
EEFEh	EEPROM[127]

(Only even addresses can be used, odd addresses are invalid)

The EEPROM Write usage is similar to Flash IAP mode. It is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target EEPROM address (EE00h~EEFEh, ADDR=ADDR+2), and the ACC contains the data being written. EEPROM writing requires approximately 2 ms @V_{CC}=3.0V, 1 ms @V_{CC}=5.0V. Meanwhile, the CPU stays in a waiting state, but all peripheral modules (Timers, LED, and others) continue running during the writing time. The software must handle the pending interrupts after an EEPROM write. The chip has a build-in EEPROM Time-out function shared with Flash IAP for escaping write fail state. EEPROM writing needs V_{CC}>3.0V.

The EEPROM Read can be performed by the "MOVX A, @DPTR" instruction as long as the target address points to the EE00h~EEFEh area. The EEPROM read does require approximately 300ns.

```
; EEPROM example code
; need 3.0V < VCC < 5.5V
MOV     DPTR, #0EE00h       ; DPTR=EE00h=target EEPROM[0] address
MOV     A, #0A5h            ; A=A5h=target EEPROM[0] write data
MOV     EEPWE, #0E2h        ; EEPROM write enable
MOV     AUX2, #004h         ; EEPROM Time-Out function enable
MOVX    @DPTR, A            ; EEPROM[0]=A5h, after EEPROM write
                            ; 1ms~2ms H/W writing time, CPU wait
MOV     EEPWE, #000h        ; EEPROM write disable, immediately after EEPROM write
CLR     A                   ; A=0
MOVX    A, @DPTR            ; A=A5h
```

2.3 Precautions for using EEPROM

2.3.1 About the writing characteristics of EEPROM

(1) The writing time of EEPROM is not fixed. It takes different time to write different data.

(2) The writing time is affected by voltage, temperature, and data conversion conditions. Higher voltage makes the writing time shorter. When the temperature is high or there are more data 0, the writing time is longer.

(3) The CPU is in a waiting state during the EEPROM writing process, but all peripheral modules (timers, etc.) continue to run. The software must handle the interrupt generated during the process after the EEPROM data is written.

(4) This chip has a built-in timeout watchdog timer to protect the write timeout, ensuring that the system can execute the program normally.

2.3.2 About the write time of EEPROM

The write time of EEPROM is related to voltage, temperature, and the number of writes.

At least 50,000 erase cycles (F_{SYS}=FRC/2, 3.5V < Write Voltage < 5.5V, -20℃~105℃)

2.3.3 Write verification

Depending on the specific application, it is generally required to read back the value written to the program EEPROM for comparison and verification.

2.3.4 Protection against erroneous writes

When starting the write operation, the following operations can prevent erroneous writes:

(1) Under-voltage detection. When writing EEPROM, the voltage must be >3.5V. The LVD function can be used to monitor the voltage.

(LVD monitoring voltage is recommended to be greater than 3.7V to prevent power failure and leave enough time for writing EEPROM)

(2) Clear the watchdog (WDT) every time a byte is written. Prevent the watchdog from resetting when multiple bytes are written continuously.

(3) When writing data, it is necessary to temporarily disable the interrupt and enable the interrupt after the writing is completed.

(4) In case of software failure, add an EEPROM read-back mechanism to the program to ensure that the data is written correctly.

(5) Timeout protection: Enable the write timeout watchdog (IAPTE) in the program to prevent the system from freezing due to write timeout.

(6) Power glitch: Connecting capacitors in parallel to the VCC and VSS pins according to the waveform can stabilize the system power supply.

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPCON	IAPCON							
R/W	W							
Reset	–	–	–	–	–	–	–	–

C9h.7~0 **IAPCON (W):**

Write 47h or 74h to set IAPWE flag; Write 47h can write 1 byte at once, write 74h can write 2 bytes at once. Write other value to clear IAPWE flag. It is recommended to clear it immediately after IAP write.

Write A1h to set INFOWE flag; write other value to clear INFOWE flag. It is recommended to clear it immediately after IAP write.

Write E2h to set EEPWE flag; write other value to clear EEPWE flag. It is recommended to clear it immediately after EEPROM write.

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPCON	IAPWE	IAPTO	EEPWE	INFOWE	–	–	–	–
R/W	R	R	R	R	–	–	–	–
Reset	0	0	0	0	–	–	–	–

C9h.6 **IAPTO (R):** Time-Out flag of IAP write/EEPROM write/INFO write. Set by H/W when IAP or EEPROM write or INFO write Time-out occurs. Cleared this flag by H/W when IAPWE=0 or EEPWE=0 or INFOWE=0.

C9h.5 **EEPWE (R):** Flag indicates EEPROM memory can be written or not

0: EEPROM Write disable

1: EEPROM Write enable

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.2~1 **IAPTE:** IAP (or EEPROM) write watchdog timer enable

00: Disable

01: wait 3ms trigger watchdog time-out flag, and escape the write fail state

10: wait 6ms trigger watchdog time-out flag, and escape the write fail state

11: wait 25ms trigger watchdog time-out flag, and escape the write fail state

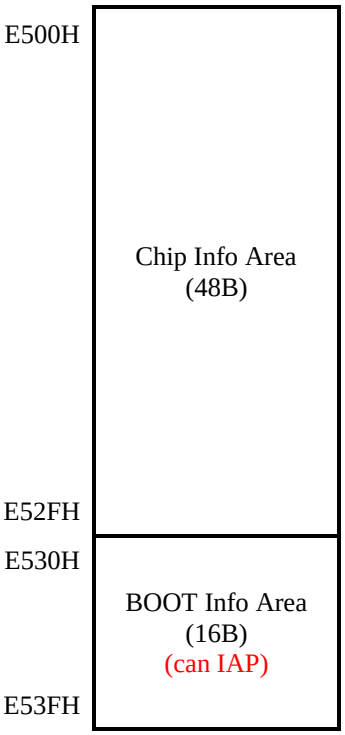
2.4 Information Memory

The Chip has a 64 bytes Information memory. The Information memory address continuous space (E500h~E53Fh) is partitioned to several sectors for device operation.

Chip Info area is tenx reserved defined as production information, such as ID, Special Regulations, Code Num, checksum. BOOT Info area allow IAP write, user can store new checksum code in this area after Flash IAP.

To use IAP function, user need to meet the following conditions:

1. Only BOOT Info Area can be written by IAP.
2. Set INFOWE=1.



Info ROM partition

Info ROM IAP Write is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target Flash address, and the ACC contains the data being written. Flash writing requires approximately 0.6 ms @V_{CC}=4.0V~5.5V, VCC capacitance greater than 220uF. During the period of IAP, the CPU stays in a waiting state, but all peripheral modules continue running during the writing time. The software must handle the pending interrupts after an IAP write. The chip has a build-in write Time-out function selected by IAPTE (F7h.2~1) to escape write fail state.

Info ROM IAP Read only can be performed by the "MOVX" instruction as long as the target address points to the E500h~E53Fh area. An Info ROM IAP read does not require extra CPU wait time.

Info ROM IAP Example:

; need 4.0V < V_{CC} < 5.5V

```
ORL     PWRCON, #80h      ; IVC disable
MOV     DPTR, #E530h      ; DPTR=E530h=target IAP address
MOV     A, #5Ah           ; A=5Ah=target IAP write data
MOV     AUX2,  #04h       ; IAP Time-Out function select
MOV     IAPCON, #A1h      ; Info ROM IAP write enable.
MOVX    @DPTR, A          ; IAP Write Info ROM
                          ; Info ROM[E530h] =5Ah after IAP write
MOV     IAPCON, #00h      ; IAP write disable, immediately after IAP write
ANL     PWRCON, #7Fh      ; IVC Enable
MOVX    A, @DPTR          ; Read Info ROM.  A=5Ah
```

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPCON	IAPCON							
R/W	W							
Reset	–	–	–	–	–	–	–	–

C9h.7~0 **IAPCON (W):**
Write 47h or 74h to set IAPWE flag; Write 47h can write 1 byte at once, write 74h can write 2 bytes at once. Write other value to clear IAPWE flag. It is recommended to clear it immediately after IAP write.
Write A1h to set INFOWE flag; write other value to clear INFOWE flag. It is recommended to clear it immediately after IAP write.
Write E2h to set EEPWE flag; write other value to clear EEPWE flag. It is recommended to clear it immediately after EEPROM write.

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPCON	IAPWE	IAPTO	EEPWE	INFOWE	–	–	–	–
R/W	R	R	R	R	–	–	–	–
Reset	0	0	0	0	–	–	–	–

C9h.6 **IAPTO (R):** Time-Out flag of IAP write/EEPROM write/INFO write. Set by H/W when IAP or EEPROM write or INFO write Time-out occurs. Cleared this flag by H/W when IAPWE=0 or EEPWE=0 or INFOWE=0.

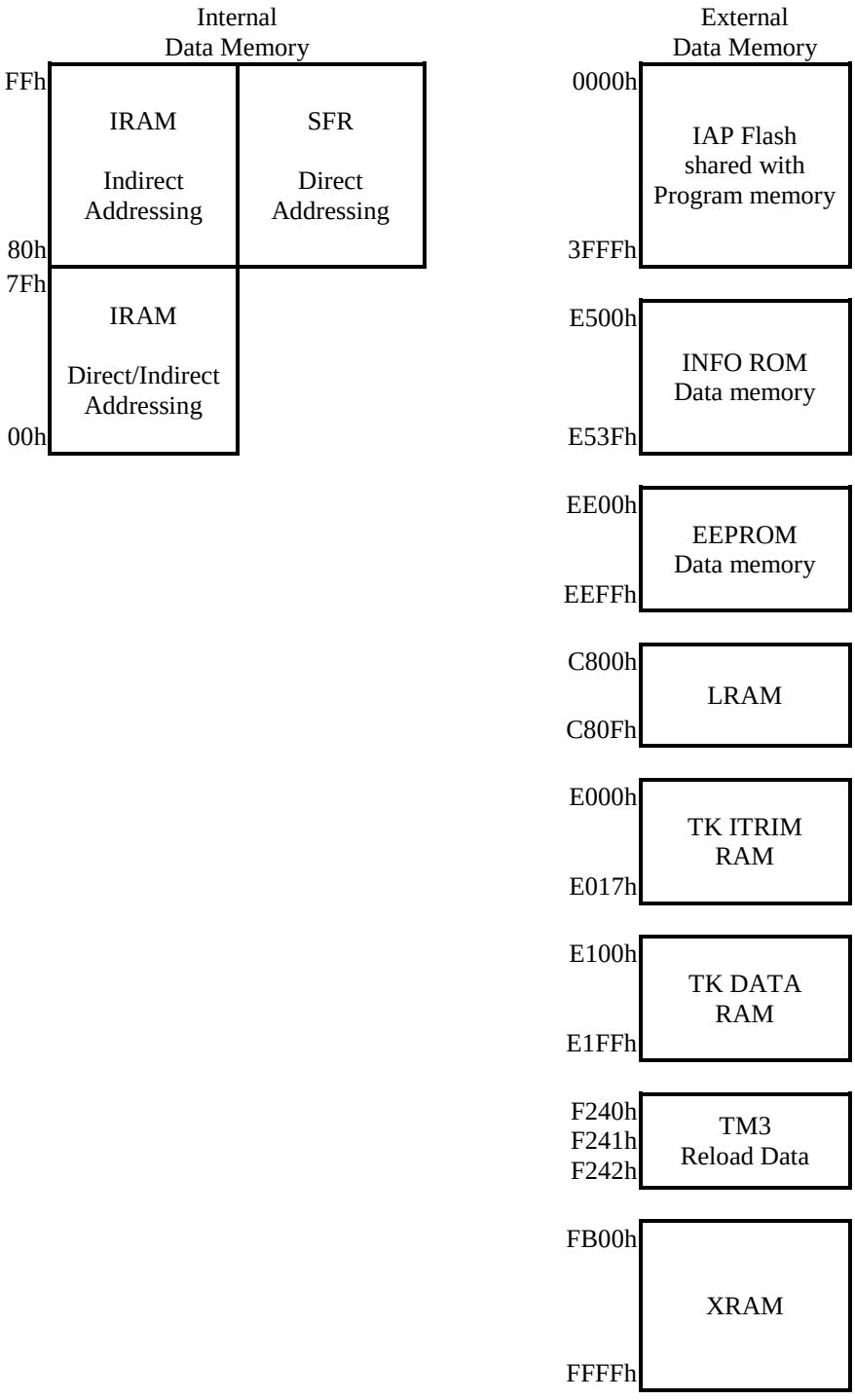
C9h.4 **INFOWE (R):** Flag indicates INFO memory can be written by IAP or not
0: INFO IAP Write disable
1: INFO IAP Write enable

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.2~1 **IAPTE:** IAP write/EEPROM write/INFO write watchdog timer enable
00: Disable
01: wait 3ms trigger watchdog time-out flag, and escape the write fail state
10: wait 6ms trigger watchdog time-out flag, and escape the write fail state
11: wait 25ms trigger watchdog time-out flag, and escape the write fail state

2.5 Data Memory

As the standard 8051, the Chip has both Internal and External Data Memory space. The Internal Data Memory space consists of 256 Bytes IRAM and SFRs, which are accessible through a rich instruction set. The External Data Memory space consists of 1280 Bytes XRAM, 16 Bytes LCD RAM, 3 Bytes TM3 Reload Data, 24 Bytes TK ITRIM RAM, 64 Bytes TK DATA RAM, 128 Bytes EEPROM, 64 Bytes INFO ROM and IAP Flash, which can be only accessed by MOVX instruction.



2.5.1 IRAM

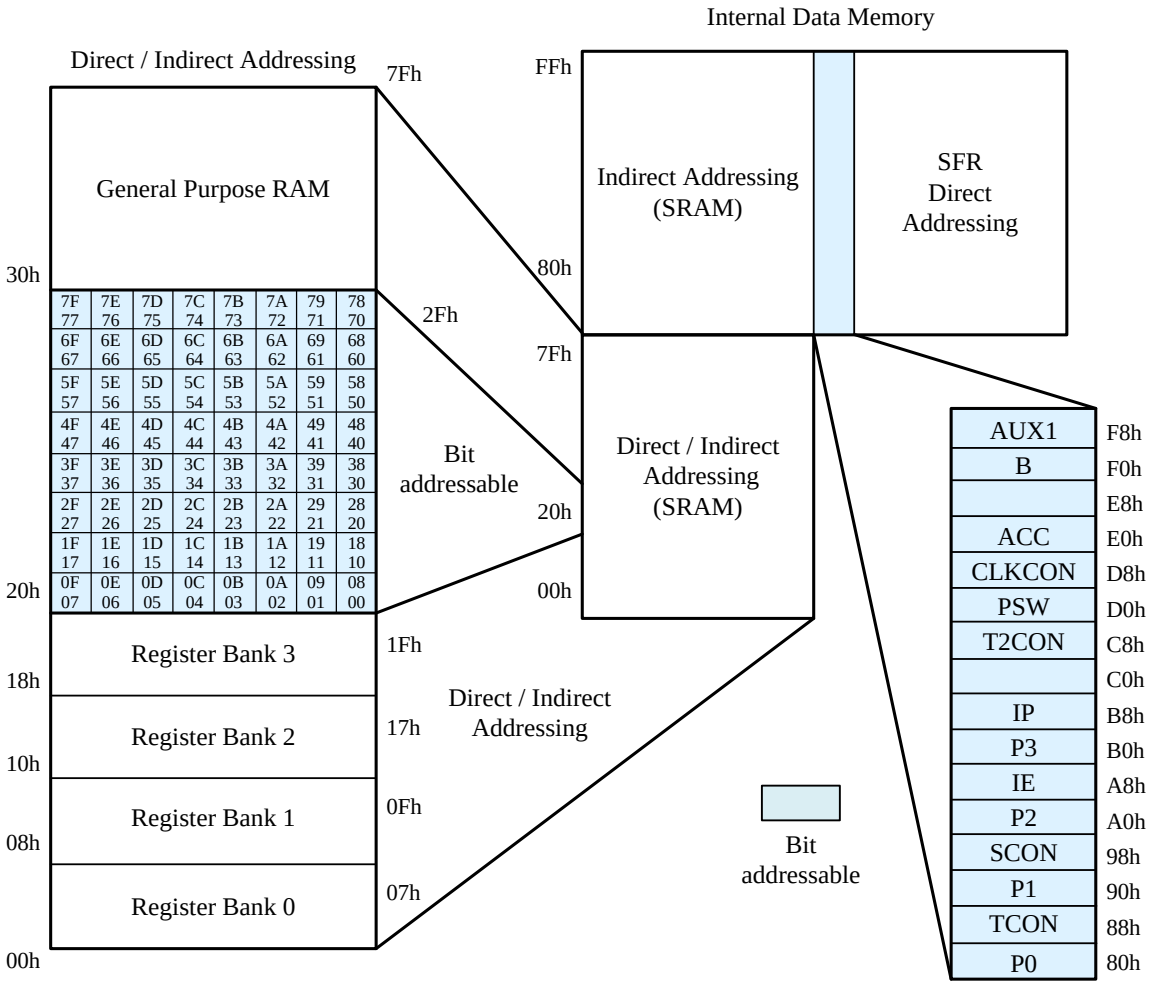
IRAM is located in the 8051 internal data memory space. The whole 256 Bytes IRAM are accessible using indirect addressing but only the lower 128 Bytes are accessible using direct addressing. There are four directly addressable register banks (switching by PSW), which occupy IRAM space from 00h to 1Fh. The address 20h to 2Fh 16 Bytes IRAM space is bit-addressable. IRAM can be used as scratch pad registers or program stack.

2.5.2 XRAM

XRAM is located in the 8051 external data memory space (address from FB00h to FFFFh). The 1280 Bytes XRAM can be only accessed by "MOVX" instruction.

2.5.3 SFRs

All peripheral functional modules such as I/O ports, Timers and UART operations for the chip are accessed via Special Function Registers (SFRs). These registers occupy upper 128 Bytes of direct Data Memory space locations in the range 80h to FFh. There are 14 bit-addressable SFRs (which means that eight individual bits inside a single byte are addressable), such as ACC, B register, PSW, TCON, SCON, and others. The remaining SFRs are only byte addressable. SFRs provide control and data exchange with the resources and peripherals of the Chip. The TM52 series of microcontrollers provides complete binary code with standard 8051 instruction set compatibility. Beside the standard 8051 SFRs, the Chip implements additional SFRs used to configure and access subsystems such as the ADC/TK/LED/LCD…, which are unique to the Chip.



	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
F8h	AUX1							
F0h	B	CRCDL	CRCDH	CRCIN		CFGBG	CFGWL	AUX2
E8h		PWM4DH	PWM4DL	PWM5DH	PWM5DL	PWM6DH	PWM6DL	AUX3
E0h	ACC	MICON	MIDAT	LVRCON	LVDCON	EFTCON	EXA	EXB
D8h	CLKCON	PWM0PRDH	PWM0PRDL	PWM1PRDH	PWM1PRDL	PWM3DH	PWM3DL	UART1CON
D0h	PSW	PWM0DH	PWM0DL	PWM1DH	PWM1DL	PWM2DH	PWM2DL	TKCON3
C8h	T2CON	IAPCON	RCP2L	RCP2H	TL2	TH2	EXA2	EXA3
C0h		SIADR	SICON	SIRCD1	SITXRCD2	ATKCH0	ATKCH1	ATKCH2
B8h	IP	IPH	IP1	IP1H	SPCON	SPSTA	SPDAT	
B0h	P3	LXDCON	LXDCON2	P3LOE	TKTMRL	TKTMRH	PWMOE0	PWMOE1
A8h	IE	INTE1	ADCDL	ADCDH	P1LOE	TKCON	ADCHSEL	PWMCON2
A0h	P2	PWMCON	P1MODL	P1MODH	P3MODL	P3MODH	PINMOD	TKCHS
98h	SCON	SBUF	SCON2	SBUF2	P0WKUP	P2WKUP	P3WKUP	
90h	P1	P0MODL	P0MODH	P2MODL	OPTION	INTFLG	P1WKUP	SWCMD
88h	TCON	TMOD	TL0	TL1	TH0	TH1	P2LOE	UART2CON
80h	P0	SP	DPL	DPH	INTE2	INTFLG2	P0LOE	PCON

SFR table

3. LVR and LVD setting

The Chip provides LVR and Low Voltage Detection (LVD) functions. There are 16-level LVR can be selected by LVRCON and 16-level LVD can be selected by SFR LVDCON. The SFR PWRSAV bits also affect LVR function as tables below.

Operation Mode	SFR			LVR	Function	Note
	LVRPD	PWRSAV	LVRSEL			
Fast Slow	0	X	0000	ON	LV Reset 2.05V	
	0	X	0001	ON	LV Reset 2.19V	
	0	X	0010	ON	LV Reset 2.33V	
	0	X	0011	ON	LV Reset 2.47V	
	0	X	0100	ON	LV Reset 2.61V	
	0	X	0101	ON	LV Reset 2.75V	
	0	X	0110	ON	LV Reset 2.89V	
	0	X	0111	ON	LV Reset 3.03V	
	0	X	1000	ON	LV Reset 3.17V	
	0	X	1001	ON	LV Reset 3.31V	
	0	X	1010	ON	LV Reset 3.45V	
	0	X	1011	ON	LV Reset 3.59V	
	0	X	1100	ON	LV Reset 3.73V	
	0	X	1101	ON	LV Reset 3.87V	
	0	X	1110	ON	LV Reset 4.01V	
	0	X	1111	ON	LV Reset 4.15V	
Idle Stop Halt	0	0	0000	ON	LV Reset 2.05V	Current consumption about 60～80uA
	0	0	0001	ON	LV Reset 2.19V	
	0	0	0010	ON	LV Reset 2.33V	
	0	0	0011	ON	LV Reset 2.47V	
	0	0	0100	ON	LV Reset 2.61V	
	0	0	0101	ON	LV Reset 2.75V	
	0	0	0110	ON	LV Reset 2.89V	
	0	0	0111	ON	LV Reset 3.03V	
	0	0	1000	ON	LV Reset 3.17V	
	0	0	1001	ON	LV Reset 3.31V	
	0	0	1010	ON	LV Reset 3.45V	
	0	0	1011	ON	LV Reset 3.59V	
	0	0	1100	ON	LV Reset 3.73V	
	0	0	1101	ON	LV Reset 3.87V	
	0	0	1110	ON	LV Reset 4.01V	
	0	0	1111	ON	LV Reset 4.15V	
Idle	0	1	XXXX	ON	Disable LVR Enable POR 1.75V	Current consumption about 18uA
Stop Halt	0	1	XXXX	OFF	Disable	*Minimum Current consumption
Idle	1	X	XXXX	ON	Disable LVR Enable POR 1.75V	Current consumption about 18uA
Stop Halt	1	X	XXXX	OFF	Disable	*Minimum Current consumption

Note: *The current consumption of Halt mode is more than Stop mode about 2~7uA, because SRC is enabled.*

SFR **E3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVRCON	–	–	PORPD	LVRPD	LVRSEL			
R/W	–	–	R/W	R/W	R/W			
Reset	–	–	0	0	0	0	0	0

E3h.5 **PORPD:** Power on Reset select
0: POR is enable
1: POR is disable

E3h.4 **LVRPD:** Low Voltage Reset function select
0: LVR is enable
1: LVR is disable

E3h.3~0 **LVRSEL:** Low Voltage Reset select (step=0.14V)

0000: Set LVR at 2.05V	1000: Set LVR at 3.17V
0001: Set LVR at 2.19V	1001: Set LVR at 3.31V
0010: Set LVR at 2.33V	1010: Set LVR at 3.45V
0011: Set LVR at 2.47V	1011: Set LVR at 3.59V
0100: Set LVR at 2.61V	1100: Set LVR at 3.73V
0101: Set LVR at 2.75V	1101: Set LVR at 3.87V
0110: Set LVR at 2.89V	1110: Set LVR at 4.01V
0111: Set LVR at 3.03V	1111: Set LVR at 4.15V

SFR **E4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDCON	LVDM	LVDO	LVDHYS	LVDPD	LVDSEL			
R/W	R/W	R	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0

E4h.7 **LVDM:** Low Voltage Detect function mode
0: $V_{CC} < V_{LVD}$ (LVDIF = 1 while LVDO = 1)
1: $V_{CC} > V_{LVD}$ (LVDIF = 1 while LVDO = 0)

E4h.6 **LVDO:** Low Voltage Detect real time output

E4h.5 **LVDHYS:** LVD Hysteresis Enable
0: LVD Hysteresis disable
1: LVD Hysteresis enable

E4h.4 **LVDPD:** Low Voltage Detect function select (Auto disable in Idle/Halt/Stop mode)
0: enable
1: disable

E4h.3~0 **LVDSEL:** Low Voltage Detect select (step=0.14V)

0000: Set LVD at 2.05V	1000: Set LVD at 3.17V
0001: Set LVD at 2.19V	1001: Set LVD at 3.31V
0010: Set LVD at 2.33V	1010: Set LVD at 3.45V
0011: Set LVD at 2.47V	1011: Set LVD at 3.59V
0100: Set LVD at 2.61V	1100: Set LVD at 3.73V
0101: Set LVD at 2.75V	1101: Set LVD at 3.87V
0110: Set LVD at 2.89V	1110: Set LVD at 4.01V
0111: Set LVD at 3.03V	1111: Set LVD at 4.15V

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W		R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.5 **PWRSAV:** chip power-saving option
Set 1 to reduce the chip's power consumption at Idle/Halt/Stop Mode

4. Reset

The Chip has five types of reset methods. Resets can be caused by Power on Reset (POR), External Pin Reset (XRST), Software Command Reset (SWRST), Watchdog Timer Reset (WDTR), or Low Voltage Reset (LVR). The CFGWH controls the Reset functionality. The SFRs are returned to their default value after Reset.

4.1 Power on Reset (POR)

After power-on reset, the device stays in the reset state and the preheating time of this chip is about 40 ms. A power-on reset requires the voltage on the VCC pin to discharge to near the VSS level before rising above 2.2V. POR is automatically turned off when the chip enters Halt/Stop mode and can be enabled or disabled by PORPD (E3h.5) when the chip enters Halt/Stop mode.

4.2 External Pin Reset (XRST)

External Pin Reset is active low. It needs to keep at least 2 SRC clock cycle long to be seen by the Chip. External Pin Reset can be disabled or enabled by CFGW.

4.3 Software Command Reset (SWRST)

Software Reset is activated by writing data 56h to SWCMD (97h).

4.4 Watchdog Timer Reset (WDTR)

WDT overflow Reset is disabled or enabled by WDTE (F7h.7~6). The WDT uses SRC as its counting time base. It runs in Fast/Slow mode and runs or stops in Idle/Halt/Stop mode. The watchdog timer overflow speed can be defined by WDTPSC (94h.5~4). WDT is cleared by CLRWDT (F8h.7) or reset.

4.5 Low Voltage Reset (LVR)

Low voltage reset (LVR) can select 16 different voltage thresholds through LVRCON (E3h.3~0). When PWRSAV (F7h.5) =1, the LVR will automatically turn off when the chip enters Idle/Halt/Stop mode. It can be enabled or disabled by LVRPD (E3h.4).

Note: *refer to AP-TM52XXXXX_02S for LVR setting information*

Flash **3FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	PORSEL	HVS	–	–	–	–

3FFFh.6 **XRSTE:** External Pin Reset control
0: Disable External Pin Reset
1: Enable External Pin Reset

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	TKBUFS	TM3CKS	WDTPSC		ADCKS		TKOFC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.5~4 **WDTPSC:** Watchdog Timer prescaler time select
00: 400ms WDT overflow rate
01: 200ms WDT overflow rate
10: 100ms WDT overflow rate
11: 50ms WDT overflow rate

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPEN/SWRST							
R/W	W							
Reset	–							

97h.7~0 **SWRST:** Write 56h to generate S/W Reset

SFR **E3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVRCON	–	–	PORPD	LVRPD	LVRSEL			
R/W	–	–	R/W	R/W	R/W			
Reset	–	–	0	0	0	0	0	0

E3h.5 **PORPD:** Power on Reset select
0: POR is enable
1: POR is disable

E3h.4 **LVRPD:** Low Voltage Reset function select
0: LVR is enable
1: LVR is disable

E3h.3~0 **LVRSEL:** Low Voltage Reset select (step=0.14V)
0000: Set LVR at 2.05V
0001: Set LVR at 2.19V
0010: Set LVR at 2.33V
0011: Set LVR at 2.47V
0100: Set LVR at 2.61V
0101: Set LVR at 2.75V
0110: Set LVR at 2.89V
0111: Set LVR at 3.03V
1000: Set LVR at 3.17V
1001: Set LVR at 3.31V
1010: Set LVR at 3.45V
1011: Set LVR at 3.59V
1100: Set LVR at 3.73V
1101: Set LVR at 3.87V
1110: Set LVR at 4.01V
1111: Set LVR at 4.15V

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W		R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.7~6 **WDTE:** Watchdog Timer Reset control
0x: Watchdog Timer Reset disable
10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Halt/Stop mode
11: Watchdog Timer Reset always enable

F7h.5 **PWRSAV:** chip power-saving option
Set 1 to reduce the chip's power consumption at Idle/Halt/Stop Mode

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W
Reset	0	0	0	0	1	1	–	0

F8h.7 **CLRWDT:** Set to clear WDT, H/W auto clear it at next clock cycle

SFR **E4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDCON	LVDM	LVDO	LVDHYS	LVDPD	LVDSEL			
R/W	R/W	R	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0

E4h.7 **LVDM:** Low Voltage Detect function mode
0: $V_{CC} < V_{LVD}$ (LVDIF = 1 while LVDO = 1)
1: $V_{CC} > V_{LVD}$ (LVDIF = 1 while LVDO = 0)

E4h.6 **LVDO:** Low Voltage Detect real time output

E4h.5 **LVDHYS:** LVD Hysteresis Enable
0: LVD Hysteresis disable
1: LVD Hysteresis enable

E4h.4 **LVDPD:** Low Voltage Detect function select (Auto disable in Idle/Halt/Stop mode)
0: enable
1: disable

E4h.3~0 **LVDSEL:** Low Voltage Detect select (step=0.14V)
0000: Set LVD at 2.05V
0001: Set LVD at 2.19V
0010: Set LVD at 2.33V
0011: Set LVD at 2.47V
0100: Set LVD at 2.61V
0101: Set LVD at 2.75V
0110: Set LVD at 2.89V
0111: Set LVD at 3.03V
1000: Set LVD at 3.17V
1001: Set LVD at 3.31V
1010: Set LVD at 3.45V
1011: Set LVD at 3.59V
1100: Set LVD at 3.73V
1101: Set LVD at 3.87V
1110: Set LVD at 4.01V
1111: Set LVD at 4.15V

5. Clock Circuitry & Operation Mode

5.1 System Clock

The Chip is designed with dual-clock system. During runtime, user can directly switch the System clock from fast to slow or from slow to fast. It also can directly select a clock divider of 1, 2, 4 or 16. The Fast clock can be selected as FXT (Fast Crystal, 1~18 MHz) or FRC (Fast Internal RC, 18.432 MHz). The Slow clock can be selected as SXT (Slow Crystal, 32 KHz) or SRC (Slow Internal RC, 41 KHz). Fast mode and Slow mode are defined as the CPU running at Fast and Slow clock speeds.

After Reset, the device is running at Slow mode with 41 KHz SRC. S/W should select the proper clock rate for chip operation safety. The higher V_{CC} allows the chip to run at a higher System clock frequency. In a typical condition, a 18 MHz System clock rate requires V_{CC}> 2.2V.

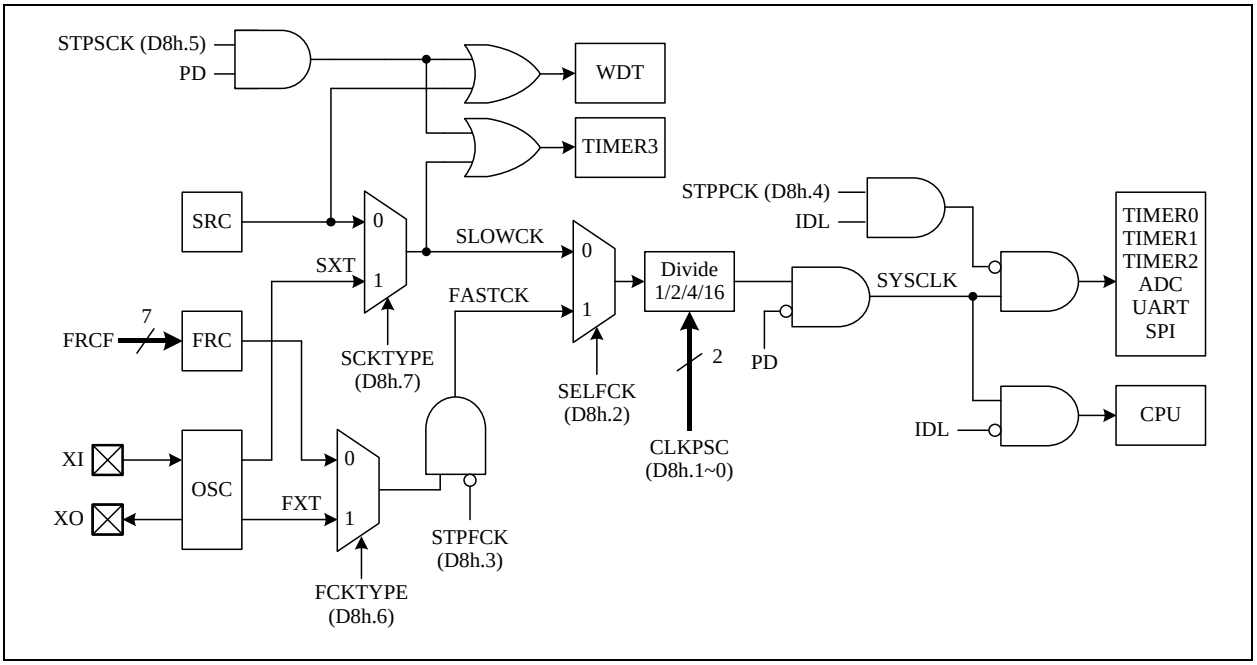
The Chip has an external oscillators connected to the XI/XO pins. It relies on external circuitry for the clock signal and frequency stabilization, such as a stand-alone oscillator, quartz crystal, or ceramic resonator. In Fast mode, the fast oscillator can be used in the range from 1~18 MHz. In Slow mode, the slow oscillator can only use a clock frequency of 32.768 KHz.

The **CLKCON** SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow clock type in Fast mode and change the Fast clock type in Slow mode. Never to write both STPFCK=1 & SELFCK=1. It is recommended to write this SFR bit by bit.

If user wants to switch F_{SYSCLK} from Slow clock to FXT, user should be following the step below

1. Set FCKTYPE (D8h.6)
2. Wait 2ms until FXT oscillation stable
3. Set SELFCK (D8h.2)

The chip can also output the "System clock divided by 2" signal (CKO) to P1.4 pin. CKO pin's output setting is controlled by PINMOD SFR (***see Chapter 7***).



Clock Structure

Note: *Because of the CLKPSC delay, it needs to wait for 16 clock cycles (max.) before switching Slow clock to Fast clock. Also refer to AP-TM52XXXXX_01S and AP-TM52XXXXX_02S about System Clock Application Note.*

SYSCLK	CLKCON (D8h)			
	bit7 SCKTYPE	bit6 FCKTYPE	bit3 STPFCK	bit2 SELFCK
Fast FXT	0/1	1	0	1
Fast FRC	0/1	0	0	1
Slow SXT	1	0/1	0/1	0
Slow SRC	0	0/1	0/1	0
Fast type change	0/1	0 ← → 1	0/1	0
Slow type change	0 ← → 1	0/1	0	1
Stop FRC/FXT	0/1	0/1	0 → 1	0
Switch to FRC/FXT	0/1	0/1	0	0 → 1
Switch to SRC/SXT	0/1	0/1	0	1 → 0

Flash **3FFDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	–	FRCF						

3FFDh.6~0 **FRCF:** FRC frequency adjustment.
FRC is trimmed to 18.432 MHz in chip manufacturing. FRCF records the adjustment data.

SFR **F6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	–	FRCF						
R/W	–	R/W						
Reset	–	–	–	–	–	–	–	–

F6h.6~0 **FRCF:** FRC frequency adjustment
00h= lowest frequency, 7Fh=highest frequency.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	1	0	0	0	1	1

D8h.7 **SCKTYPE:** Slow clock type. This bit can be changed only in Fast mode (SELFCK=1).
0: SRC
1: SXT, P2.0 and P2.1 are crystal pins

D8h.6 **FCKTYPE:** Fast clock type. This bit can be changed only in Slow mode (SELFCK=0).
0: FRC
1: FXT, P2.0 and P2.1 are crystal pins, oscillator gain is high for FXT

D8h.5 **STPSCK:** Set 1 to stop Slow clock in PDOWN mode

D8h.4 **STPPCK:** Set 1 to stop UARTs/Timer0/Timer1/Timer2/ADC clock in Idle mode for current reducing. If set, only Timer3 and pin interrupts are alive in Idle Mode.

D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.

D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock

D8h.1~0 **CLKPSC:** System clock prescaler. Effective after 16 clock cycles (Max.) delay.
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

5.2 Operation Modes

There are five operation modes for this device. **Fast Mode** is defined as the CPU running at Fast clock speed. **Slow Mode** is defined as the CPU running at Slow clock speed. When the System clock speed is lower, the power consumption is lower.

Idle Mode is entered by setting the IDL bit in PCON SFR. Both Fast and Slow clock can be set as the System clock source in Idle Mode, but Slow clock is better for power saving. In Idle mode, the CPU puts itself to sleep while the on-chip peripherals stay active. The "STPPCK" bit in CLKCON SFR can be set to furthermore reduce Idle mode current. If STPPCK is set, only Timer3 and pin interrupts are alive in Idle Mode, others peripherals such as Timer0/1/2, UARTs and ADC are stop. The slower System clock rate also helps current saving. It can be achieved by setup the CLKPSC SFR to divide System clock frequency. Idle mode is terminated by Reset or enabled Interrupts wake up.

Stop Mode is entered by setting the PD bit in PCON SFR and STPSCK is set. This mode is the so-called "Power Down" mode in standard 8051. In Stop mode, all clocks stop except the WDT could be alive if it is enabled. Stop Mode is terminated by Reset or pin wake up.

Halt Mode is entered by setting the PD bit in PCON SFR and STPSCK is cleared. In Halt mode, all clocks stop except the Timer3 and WDT could be alive if they are enabled. Halt Mode is terminated by Reset, pin wake up or Timer3 interrupt. In this mode, Timer3 clock source can only choose Slow clock, not FRC/512.

Note: *Chip cannot enter Halt/Stop Mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0~2)*

Note: *FW must turn off Bandgap to obtain Tiny Current (VBGOUT=0)*

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter Halt/Stop mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter Idle mode.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	1	0	0	0	1	1

D8h.7 **SCKTYPE:** Slow clock type. This bit can be changed only in Fast mode (SELFCK=1).
0: SRC 1: SXT, P2.0 and P2.1 are crystal pins

D8h.6 **FCKTYPE:** Fast clock type. This bit can be changed only in Slow mode (SELFCK=0).
0: FRC 1: FXT, P2.0 and P2.1 are crystal pins, oscillator gain is high for FXT

D8h.5 **STPSCK:** Set 1 to stop Slow clock in PDOWN mode

D8h.4 **STPPCK:** Set 1 to stop UART/Timer0/Timer1/Timer2/ADC clock in Idle mode for current reducing. If set, only Timer3 and pin interrupts are alive in Idle Mode.

D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.

D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock

D8h.1~0 **CLKPSC:** System clock prescaler. Effective after 16 clock cycles (Max.) delay.
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	TKBUFS	TM3CKS	WDTPSC		ADCKS		TKOFC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.6 **TM3CKS:** Timer3 cock source select
0: Slow clock (SXT/SRC)
1: FRC/512

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W		R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.4 **VBGOUT:** V_{BG} voltage output to P3.2
0: Disable
1: Enable

6. Interrupt & Wake-up

This Chip has a 14-source four-level priority interrupt structure. Only the Pin Interrupts can wake up CPU from Halt/Stop mode. Each interrupt source has its own enable control bit. An interrupt event will set its individual Interrupt Flag, no matter whether its interrupt enable control bit is 0 or 1. The Interrupt vectors and flags are list below.

Vector	Flag	Description
0003	IE0	INT0 external pin Interrupt (can wake up Halt/Stop mode)
000B	TF0	Timer0 Interrupt
0013	IE1	INT1 external pin Interrupt (can wake up Halt/Stop mode)
001B	TF1	Timer1 Interrupt
0023	RI+TI	Serial Port (UART1) Interrupt
002B	TF2+EXF2	Timer2 Interrupt
0033	–	Reserved for ICE mode use
003B	TF3	Timer3 Interrupt
0043	PCIF	Port0~Port3 external pin change Interrupt (can wake up Halt/Stop mode)
004B	IE2	INT2 external pin Interrupt (can wake up Halt/Stop mode)
0053	ADIF/TKIF	ADC/TK Interrupt
005B	SPIF MIIF TXDF/RCD2F/RCD1F	SPI/I^2C interrupt
0063	LVDIF	LVD Interrupt
006B	RI2+TI2	Serial Port (UART2) Interrupt
0073	PWM0IF PWM1IF	PWM0~ PWM1 Interrupt

Interrupt Vector & Flag

Vector	Item	Interrupt enable	Sub-interrupt enable	Interrupt flag
0003	IE0	IE A8.0		TCON 88.1
000B	TF0	IE A8.1		TCON 88.5
0013	IE1	IE A8.2		TCON 88.3
001B	TF1	IE A8.3		TCON 88.7
0023	RI+TI	IE A8.4		SCON 98.1~0
002B	TF2+EXF2	IE A8.5		T2CON C8.7~6
0033	–			
003B	TF3	INTE1 A9.0		INTFLG 95.0
0043	PCIF	INTE1 A9.1		INTFLG 95.1
004B	IE2	INTE1 A9.2		INTFLG 95.2
0053	ADIF/TKIF	INTE1 A9.3	INTE2 84.1 INTE2 84.0	INTFLG 95.4 INTFLG 95.5
005B	SPIF MIIF TXDF/RCD2F/RCD1F	INTE1 A9.4	SICON C2.7 SICON C2.6~4	SPSTA BD.7 MICON E1.5 SICON C2.2~0
0063	LVDIF	INTE1 A9.5		INTFLG 95.7
006B	RI2+TI2	INTE1 A9.6		SCON2 9A.1~0
0073	PWM0IF PWM1IF	INTE1 A9.7	INTE2 84.6 INTE2 84.5	INTFLG2 85.6 INTFLG2 85.5

Interrupt related SFRs

6.1 Interrupt Enable and Priority Control

The IE and INTE1 SFRs decide whether the pending interrupt is serviced by CPU. The P0WKUP, P1WKUP, P2WKUP and P3WKUP SFR controls the individual Port0~3 pin's wake-up and interrupt capability. The IP, IPH, IP1 and IP1H SFRs decide the interrupt priority. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

6.2 Suggestions on interrupting subroutines

When entering the interrupt program, in addition to the traditionally known SFR A or PSW that should be PUSH, POP, some SFRs used for indexing should also be added to the ranks of PUSH POP. To avoid writing and reading these SFRs before and after the interruption may cause inconsistencies. In addition, PWMDH, PWMDL, PWMPRDH or PWMPRDL is a 16-bit operation, and the program should avoid interrupts when writing and reading the high byte and low byte. If you are reading and writing these 16-bit SFRs in the meantime an interrupt occurs. And these SFRs are read and written in the interrupt. It is easy to cause read and write errors. For the 16-bit PWM period and duty to read and write, it is recommended to update the data only in the main program, or update the data only in the interrupt to avoid possible errors.

SFR **A8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A8h.7 **EA:** Global interrupt enable control.
0: Disable all Interrupts.
1: Each interrupt is enabled or disabled by its individual interrupt control bit

A8h.5 **ET2:** Timer2 interrupt enable
0: Disable Timer2 interrupt
1: Enable Timer2 interrupt

A8h.4 **ES:** Serial Port (UART1) interrupt enable
0: Disable Serial Port (UART1) interrupt
1: Enable Serial Port (UART1) interrupt

A8h.3 **ET1:** Timer1 interrupt enable
0: Disable Timer1 interrupt
1: Enable Timer1 interrupt

A8h.2 **EX1:** External INT1 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT1 pin Interrupt and Halt/Stop mode wake up
1: Enable INT1 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

A8h.1 **ET0:** Timer0 interrupt enable
0: Disable Timer0 interrupt
1: Enable Timer0 interrupt

A8h.0 **EX0:** External INT0 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT0 pin Interrupt and Halt/Stop mode wake up
1: Enable INT0 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	ES2	LVDIE	SPI2CE	ADTKIE	EX2	PCIE	TM3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.7 **PWMIE:** PWM0~PWM1 interrupt enable
0: Disable PWM0~PWM1 interrupt
1: Enable PWM0~PWM1 interrupt

A9h.6 **ES2:** Serial Port (UART2) interrupt enable
0: Disable Serial Port (UART2) interrupt
1: Enable Serial Port (UART2) interrupt

A9h.5 **LVDIE:** LVD interrupt enable
0: Disable LVD interrupt
1: Enable LVD interrupt.

A9h.4 **SPI2CE:** SPI/I^2C interrupt enable
0: Disable SPI/I^2C interrupt
1: Enable SPI/I^2C interrupt

A9h.3 **ADTKIE:** ADC/TK interrupt enable
0: Disable ADCTK interrupt
1: Enable ADC/TK interrupt

A9h.2 **EX2:** External INT2 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT2 pin Interrupt and Halt/Stop mode wake up
1: Enable INT2 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

A9h.1 **PCIE:** Port0~Port3 pin change interrupt enable. This bit does not affect Halt/Stop mode wake up capability.
0: Disable Port0~Port3 pin change interrupt
1: Enable Port0~Port3 pin change interrupt

A9h.0 **TM3IE:** Timer3 interrupt enable
0: Disable Timer3 interrupt
1: Enable Timer3 interrupt

SFR 84**h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE2	–	PWM1IE	PWM0IE	–	–	–	–	–
R/W	–	R/W	R/W	–	–	–	–	–
Reset	–	0	0	–	–	–	–	–

84h.6 **PWM1IE:** PWM1 Interrupt Enable
0: disable
1: enable (note: PWMIE must be 1 at the same time to generate PWM interrupt)

84h.5 **PWM0IE:** PWM0 Interrupt Enable
0: disable
1: enable (note: PWMIE must be 1 at the same time to generate PWM interrupt)

SFR **B9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPH	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

SFR **B8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

B9h.5, B8h.5 **PT2H, PT2:** Timer2 Interrupt Priority control. (PT2H, PT2) =
11: Level 3 (highest priority)
10: Level 2
01: Level 1
00: Level 0 (lowest priority)

B9h.4, B8h.4 **PSH, PS:** Serial Port (UART1) Interrupt Priority control. Definition as above.

B9h.3, B8h.3 **PT1H, PT1:** Timer1 Interrupt Priority control. Definition as above.

B9h.2, B8h.2 **PX1H, PX1:** External INT1 pin Interrupt Priority control. Definition as above.

B9h.1, B8h.1 **PT0H, PT0:** Timer0 Interrupt Priority control. Definition as above.

B9h.0, B8h.0 **PX0H, PX0:** External INT0 pin Interrupt Priority control. Definition as above.

SFR **BBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1H	PPWMH	PS2H	PLVDH	PSPI2CH	PADTKIH	PLVDH	PPCH	PT3H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR **BAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1	PPWM	PS2	PLVD	PSPI2C	PADTKI	PLVD	PPC	PT3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

BBh.7, BAh.7 **PPWMH, PPWM:** PWM0~PWM1 Interrupt Priority control. Definition as above.

BBh.6, BAh.6 **PS2H, PS2:** Serial Port (UART2) Interrupt Priority control. Definition as above.

BBh.5, BAh.5 **PLVDH, PLVD:** LVD Interrupt Priority control. Definition as above.

BBh.6, BAh.6 **PSPI2CH, PSPI2C:** SPI/I^2C Interrupt Priority control. Definition as above.

BBh.3, BAh.3 **PADTKIH, PADTKI:** ADC/TK Interrupt Priority control. Definition as above.

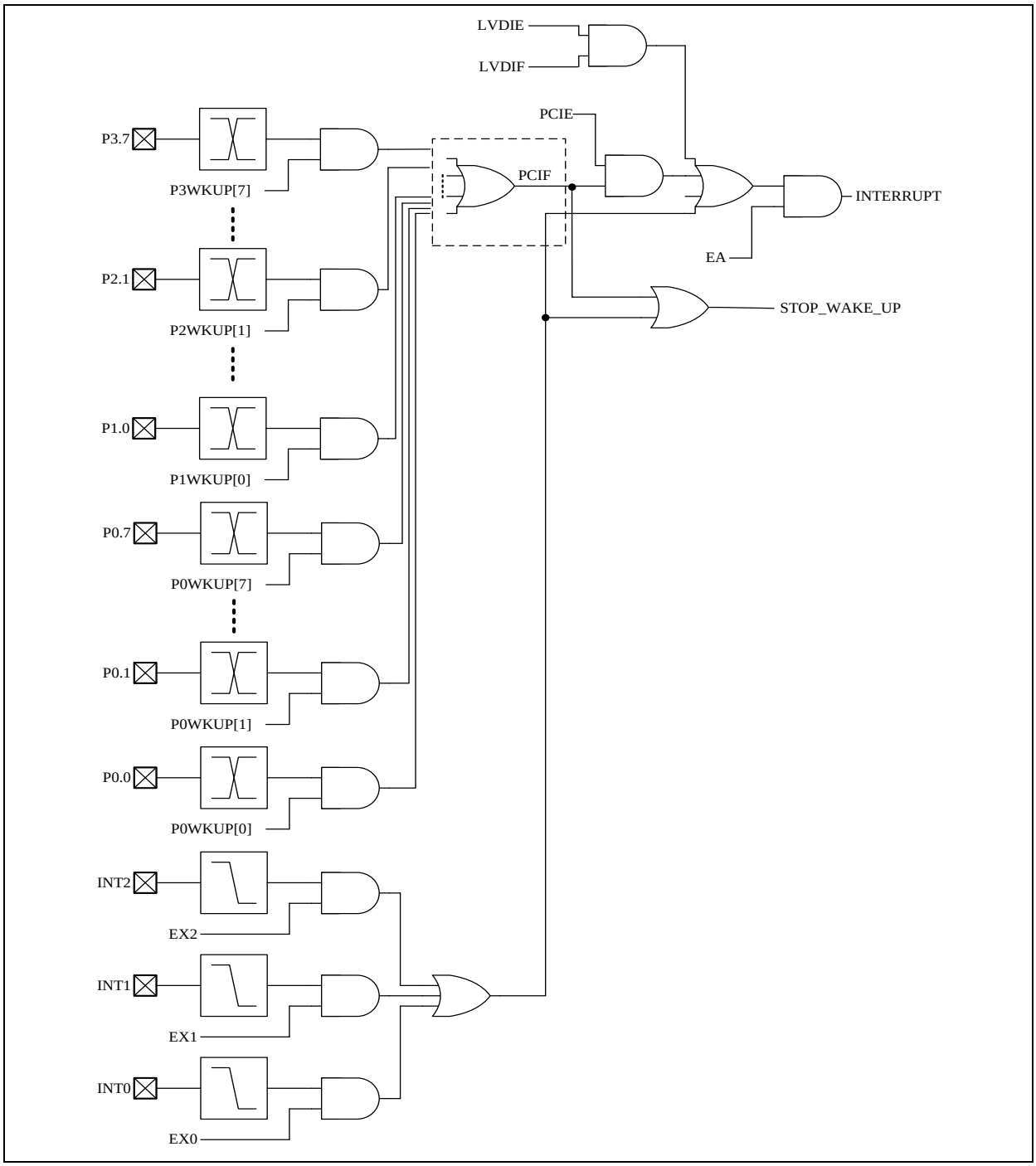
BBh.1, BAh.1 **PPCH, PPC:** Port0~ Port 3 Pin Change Interrupt Priority control. Definition as above.

BBh.0, BAh.0 **PT3H, PT3:** Timer3 Interrupt Priority control. Definition as above.

6.3 Pin Interrupt and LVD interrupt

Pin Interrupts include INT0 (P3.2), INT1 (P3.3), INT2 (P3.7) and Port0~Port3 pin change interrupt. These pins also have the Halt/Stop mode wake up capability. INT0 and INT1 are falling edge or low level triggered as the 8051 standard. INT2 is falling edge triggered and Port0~Port3 Pin Change Interrupt is triggered by I/O state change. For details, see Chapter 7. Pin Mode and pin change enable settings. LVD interrupt can be used to detect the V_{CC} voltage level and generate an interrupt.

Note: *Port0~Port3 pin change wake up or interrupt can only be used in Halt/Stop mode, and not allowed in Fast/Slow/Idle mode.*



Pin interrupt/Wake up & LVD interrupt

Note: *Chip cannot enter Halt/Stop Mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0~2)*

SFR **9Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0WKUP	P0WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

9Ch.7~0 **P0WKUP:** P0.7~P0.0 pin individual Wake-up / Interrupt enable control
0: Disable
1: Enable

SFR **96h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1WKUP	P1WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

96h.7~0 **P1WKUP:** P1.7~P1.0 pin individual Wake-up / Interrupt enable control
0: Disable
1: Enable

SFR **9Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2WKUP	–	–	–	–	–	–	P2WKUP	
R/W	–	–	–	–	–	–	R/W	
Reset	–	–	–	–	–	–	0	0

9Dh.7~0 **P2WKUP:** P2.1~P2.0 pin individual Wake-up / Interrupt enable control
0: Disable
1: Enable

SFR **9Eh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3WKUP	P3WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

9Eh.7~0 **P3WKUP:** P3.7~P3.0 pin individual Wake-up / Interrupt enable control
0: Disable
1: Enable

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVDIF	–	TKIF	ADIF	–	IE2	PCIF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.7 **LVDIF:** Low Voltage Detect interrupt flag
Set by H/W. S/W writes 7Fh to INTFLG to clear this flag.

95h.2 **IE2:** External Interrupt 2 (INT2 pin) edge flag.
Set by H/W when an INT2 pin falling edge is detected, no matter the EX2 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

95h.1 **PCIF:** Port0~Port3 Pin change interrupt flag
Set by H/W when Port0~Port3 pin state change is detected and its interrupt enable bit is set.
S/W can write 0 to clear all pin change interrupt flags (Port0~Port3).

Note: *S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.*

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.3 **IE1:** External Interrupt 1 (INT1 pin) edge flag.
Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.2 **IT1:** External Interrupt 1 control bit
0: Low level active (level triggered) for INT1 pin
1: Falling edge active (edge triggered) for INT1 pin

88h.1 **IE0:** External Interrupt 0 (INT0 pin) edge flag
Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.0 **IT0:** External Interrupt 0 control bit
0: Low level active (level triggered) for INT0 pin
1: Falling edge active (edge triggered) for INT0 pin

SFR **A8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A8h.7 **EA:** Global interrupt enable control.
0: Disable all Interrupts.
1: Each interrupt is enabled or disabled by its individual interrupt control bit

A8h.2 **EX1:** External INT1 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT1 pin Interrupt and Halt/Stop mode wake up
1: Enable INT1 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

A8h.0 **EX0:** External INT0 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT0 pin Interrupt and Halt/Stop mode wake up
1: Enable INT0 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	ES2	LVDIE	SPI2CE	ADTKIE	EX2	PCIE	TM3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.5 **LVDIE:** LVD interrupt enable
0: Disable LVD interrupt
1: Enable LVD interrupt.

A9h.2 **EX2:** External INT2 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT2 pin Interrupt and Halt/Stop mode wake up
1: Enable INT2 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

A9h.1 **PCIE:** Port0~Port3 pin change interrupt enable. This bit does not affect Halt/Stop mode wake up capability.
0: Disable Port0~Port3 pin change interrupt
1: Enable Port0~Port3 pin change interrupt

SFR **E4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDCON	LVDM	LVDO	LVDHYS	LVDPD	LVDSEL			
R/W	R/W	R	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0

E4h.7 **LVDM:** Low Voltage Detect function mode
0: $V_{CC} < V_{LVD}$ (LVDIF = 1 while LVDO = 1)
1: $V_{CC} > V_{LVD}$ (LVDIF = 1 while LVDO = 0)

E4h.6 **LVDO:** Low Voltage Detect real time output

E4h.5 **LVDHYS:** LVD Hysteresis Enable
0: LVD Hysteresis disable
1: LVD Hysteresis enable

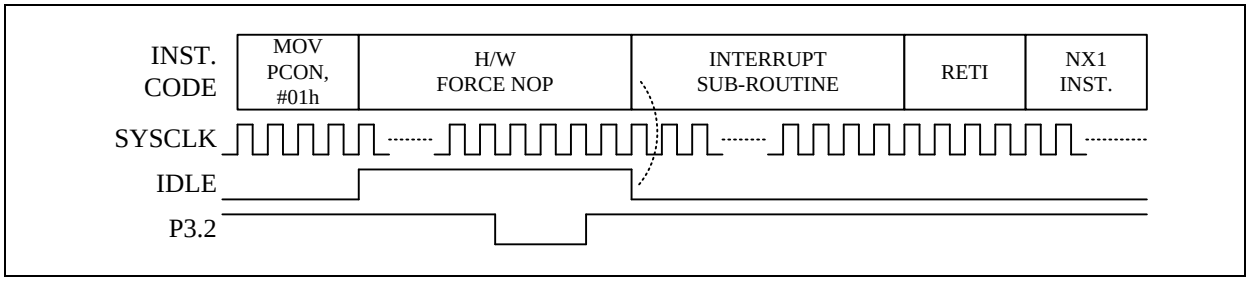
E4h.4 **LVDPD:** Low Voltage Detect function select (Auto disable in Idle/Halt/Stop mode)
0: enable
1: disable

E4h.3~0 **LVDSEL:** Low Voltage Detect select (step=0.14V)
0000: Set LVD at 2.05V
0001: Set LVD at 2.19V
0010: Set LVD at 2.33V
0011: Set LVD at 2.47V
0100: Set LVD at 2.61V
0101: Set LVD at 2.75V
0110: Set LVD at 2.89V
0111: Set LVD at 3.03V
1000: Set LVD at 3.17V
1001: Set LVD at 3.31V
1010: Set LVD at 3.45V
1011: Set LVD at 3.59V
1100: Set LVD at 3.73V
1101: Set LVD at 3.87V
1110: Set LVD at 4.01V
1111: Set LVD at 4.15V

6.4 Idle mode Wake up and Interrupt

Idle mode is waked up by enabled Interrupts, which means individual interrupt enable bit (ex: EX0) and EA bit must be both set to 1 to establish Idle mode wake up capability. All enabled Interrupts change (INT0~INT2, Timers, PWM, ADC, and UARTs) can wake up CPU from Idle mode. Upon Idle wake-up, Interrupt service routine is entered immediately. “The first instruction behind IDL (PCON.0) setting” is executed after interrupt service routine return.

For all pin interrupts to be triggered, each interrupt enable bit (e.g. EX0) and the EA bit must be set to 1 and the pin trigger state must stay long enough (greater than 1 system clock) to be sampled by the system clock. When the EA is not set to 1 or the pin trigger state does not stay long enough, it will not wake up and will not generate an interrupt subroutine.



EA=EX0=1, Idle mode wake-up and Interrupt by P3.2 (INT0)

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter Halt/Stop mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter Idle mode.

6.5 Halt/Stop mode Wake up and Interrupt

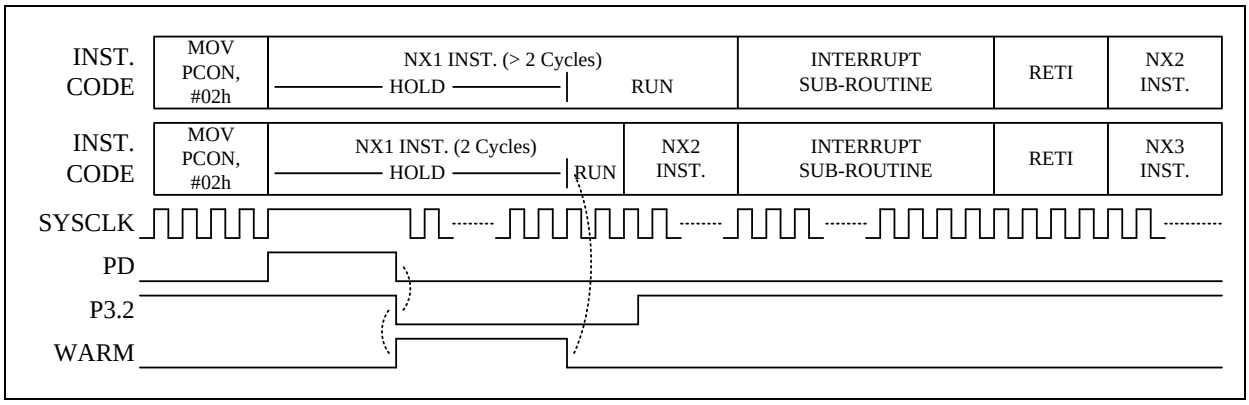
Each interrupt enable bit (e.g. TM3IE, EX0) and the EA bit must be set to 1 to establish the Halt/Stop mode interrupt function. All enabled interrupts (pins, Timer3) can wake up the CPU from Halt/Stop mode. Once Halt/Stop is woken up, if "the first instruction after PD (PCON.1) is set" is a two-cycle instruction, it will execute immediately before the interrupt is serviced, if "the first instruction after PD (PCON.1) is set" is a four-cycle or more long instruction, it will execute after the interrupt is serviced.

In addition to setting EX0/EX1/EX2, the INT0~2 pin interrupt needs to set EA=1 and the pin trigger state stays long enough (greater than 128 system clocks) to be sampled by the system clock, that is to say, when EA is not set to 1 or if the pin trigger state does not stay long enough, the CPU will only wake up without entering the interrupt subroutine.

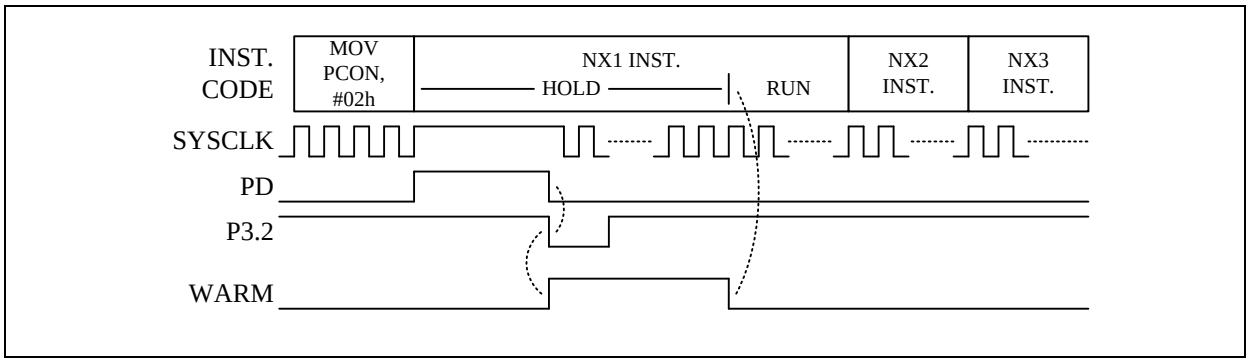
In addition to setting P0WKUP/P1WKUP/P2WKUP/P3WKUP, Port0~3 WKUP pin interrupt needs to set EA=1, that is to say, when EA is not set to 1, the CPU will only be woken up and will not enter the interrupt subroutine.

Note: *It is recommended to place the NX1/NX2 with NOP Instruction in figures below.*

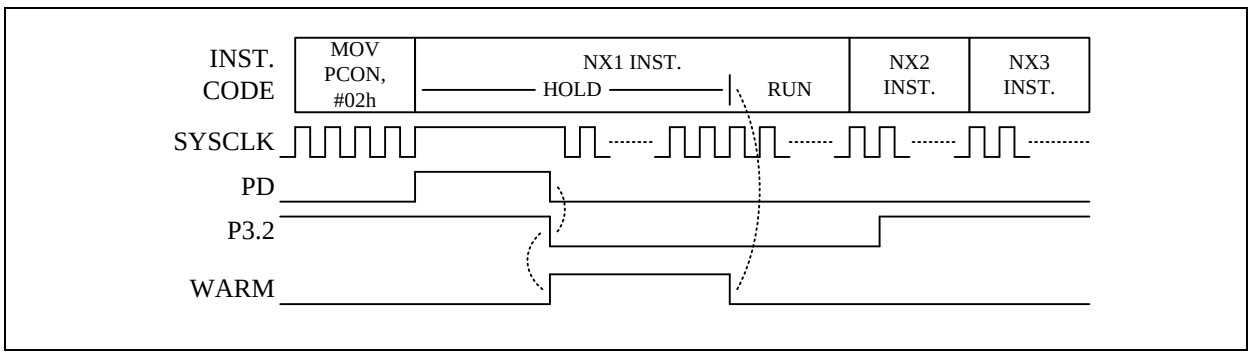
Note: *The chip cannot enter Halt/Stop mode if the INTn pin is low and the INTn wake-up function is enabled. (INTn=0 and EXn=1, n=0~2)*



EA=EX0=1, P3.2 (INT0) is sampled after warm-up, Halt/Stop mode wake-up and Interrupt



EA=EX0=1, Halt/Stop mode wake-up but not Interrupt. P3.2 (INT0) pulse too narrow



EX0= 1, EA=0, P3.2 (INT0) Halt/Stop mode wake-up but not Interrupt

7. I/O Ports

The Chip has total 26 multi-function I/O pins. All I/O pins follow the standard 8051 “Read-Modify-Write” feature. The instructions that read the SFR rather than the Pin State are the ones that read a port or port bit value, possibly change it, and then rewrite it to the SFR (ex: ANL P1, A; INC P2; CPL P3.0).

7.1 Port0~Port 3

These pins can operate in four different modes as below.

Pin Mode	Port0~Port3 pin function		Px.n SFR data	Pin State	Resistor Pull-up	Digital Input
	P3.0~P3.2	Others				
Mode 0	Open Drain (PSEUDOEN=0)	Open Drain	0	Drive Low	N	N
	Pseudo Open Drain (PSEUDOEN=1)		1	Pull-up	Y	Y
Mode 1	Open Drain (PSEUDOEN=0)	Open Drain	0	Drive Low	N	N
	Pseudo Open Drain (PSEUDOEN=1)		1	Hi-Z	N	Y
Mode 2	CMOS Output		0	Drive Low	N	N
			1	Drive High	N	N
Mode 3	Analog signal (digital input buffer is disabled)		X (don’t care)	–	N	N

Port0~Port3 I/O Pin Function Table

If a Port0~ Port3 pin is used for Schmitt-trigger input, S/W must set the I/O pin to Mode0 or Mode1 and set the corresponding Port Data SFR to 1 to disable the pin’s output driving circuitry.

When user selects Mode0 or Mode1, the function is Open drain output low, when Port data=0, the function is output low, when port data=1, the port type is Hi-Z, so user can use digital input in this setting. User can choose mode0 or mode1 for in-out type such as I2C SDA pin. The difference of Mode0 and Mode1 is whether have pull-up resistor or not, when port data = 1, Mode0 have an internal pull-up resister but mode1 haven’t, user can add external pull-up resistors by yourself when using Mode1 if you need.

When user selects Mode2, the function is CMOS output, user can choose output low or high by port data value. When user selects Mode3, the function is for analog signal, such as ADC pin, the port type is Hi-Z and the digital input Schmitt-trigger is disabled in this mode.

Beside I/O port function, each Port0~Port3 pin has one or more alternative functions, such as LCD, LED, ADC and Touch Key. Most of the functions are activated by setting the individual pin mode control SFR to Mode3. Port1/Port3 pins have standard 8051 auxiliary definition such as INT0/1/2, T0/1/2, or RXD/TXD. These pin functions need to set the pin mode SFR to Mode0 or Mode1 and keep the P1.n/P3.n SFR at 1.

Pin Name	8051	Wake-up Interrupt	ADC	TK	LCD	LED MX	LED DMX	PWM	others	Mode3
P0.7		Y	AD24	TK19	LCDC07	SEG6		PWM6(1)		AD24
P0.6		Y	AD25	TK20	LCDC06	SEG7		PWM5(1)		AD25
P0.5		Y	AD26	TK21	LCDC05			PWM4(1)		AD26
P0.4		Y	AD27	TK22	LCDC04			PWM3(1)		AD27
P0.3	TXD2(1)	Y	AD20	TK18	LCDC03	COM3	LED3			AD20
P0.2	RXD2(1)	Y	AD21		LCDC02	COM2	LED2		SDA(1)	AD21
P0.1	RXD(1)	Y	AD22		LCDC01	COM1	LED1		SCL(1)/PSDA(1)	AD22
P0.0	TXD(1)	Y	AD23		LCDC00	COM0	LED0		PSCL(1)	AD23
P1.7	TXD2	Y	AD11	TK11	LCDC17	SEG2			MISO	AD11
P1.6		Y	AD10	TK10	LCDC16	SEG3		PWM3		AD10
P1.5		Y	AD9	TK9	LCDC15	SEG4		PWM2		AD9
P1.4	TCO	Y	AD8	TK8	LCDC14	SEG5		PWM1		AD8
P1.3		Y	AD7	TK7	LCDC13			PWM0N		AD7
P1.2		Y	AD6	TK6	LCDC12			PWM0P		AD6
P1.1	T2EX	Y	AD5	TK5	LCDC11					AD5
P1.0	T2/T2O	Y	AD4	TK4	LCDC10					AD4
P2.1	XO	Y	AD19	TK17	LCDC21	COM5/SEG9	LED5	PWM0P(1)		AD19
P2.0	XI	Y	AD18	TK16	LCDC20	COM4/SEG8	LED4	PWM0N(1)		AD18
P3.7	XINT2	Y	AD17	TK15	LCDC37	COM6/SEG10	LED6	PWM6	RSTn	AD17
P3.6	RXD2	Y	AD14	TK12	LCDC36	SEG1			SCK	AD14
P3.5	T1/T1O	Y	AD15	TK13	LCDC35	SEG0		PWM4	MOSI	AD15
P3.4	T0/T0O	Y	AD16	TK14	LCDC34	COM7/SEG11	LED7	PWM5		AD16
P3.3	XINT1	Y	AD0	TK0	LCDC33			PWM2(1)		AD0
P3.2	XINT0	Y	AD1	TK1	LCDC32			PWM1(1)	VBGO	AD1
P3.1	TXD	Y	AD2	TK2	LCDC31				SDA/PSDA	AD2
P3.0	RXD	Y	AD3	TK3	LCDC30				SCL/PSCL	AD3

Port0~Port3 multi-function Table

The necessary SFR setting for Port0~ Port3 pin's alternative function is list below.

Alternative Function	Mode	Px.n SFR data	Pin State	Other necessary SFR setting
T0, T1, T2, T2EX, INT0, INT1, INT2	**0**	1	Input with Pull-up	-
	1	1	Input	
RXD, RXD2	**0**	1	UART RX (Input with Pull-up)	PINMOD
	1	1	UART RX (Input)	
TXD,TXD2	**2**	1	UART TX Output (CMOS Push-Pull)	PINMOD
T0O, T1O, T2O CKO	**0**	X	Clock Open Drain Output with Pull-up	PINMOD
	1	X	Clock Open Drain Output	
	2	X	Clock Output (CMOS Push-Pull)	
VBGO	**X**	X	Bandgap Voltage output	VBGOUT
COM0~COM7* SEG0~SEG11*	**X**	X	LCD Waveform Output LED MX Waveform Output	P0LOE P1LOE P2LOE P3LOE LXDCON LXDCON2
LED0~LED7* ***(see Note below)***	**X**	X	LED DMX Waveform Output	
TK0~TK22	**X**	X	Touch Key Channel	TKCHS ATKCH0 ATKCH1 ATKCH2
AD0~AD11 AD14~AD27	**3**	X	ADC Channel	ADCHSEL
PWM0P/PWM0N PWM1~PWM6	**0**	X	PWM Open Drain Output with Pull-up	PWMCON PWMOE0 PWMOE1
	2	X	PWM Output (CMOS Push-Pull)	
SPI Master Mode MISO	**1**	1	SPI Data Input	SPCON
SPI Master Mode SCK, MOSI	**2**	X	SPI Clock/Data Output (CMOS Push-Pull)	
SPI Slave Mode MISO	**2**	X	SPI Data Output (CMOS Push-Pull)	
SPI Slave Mode SCK, MOSI	**1**	1	SPI Clock/Data Input	
Master I^2C SCL	**0**	X	I^2C Clock Output (Open Drain Output, Pull-up)	MICON PINMOD
	2	X	I^2C Clock Output (CMOS Push-Pull)	
Master I^2C SDA	**0**	1	I^2C Data (Pull-up)	
XI, XO	**0**	1	Crystal oscillation	CLKCON

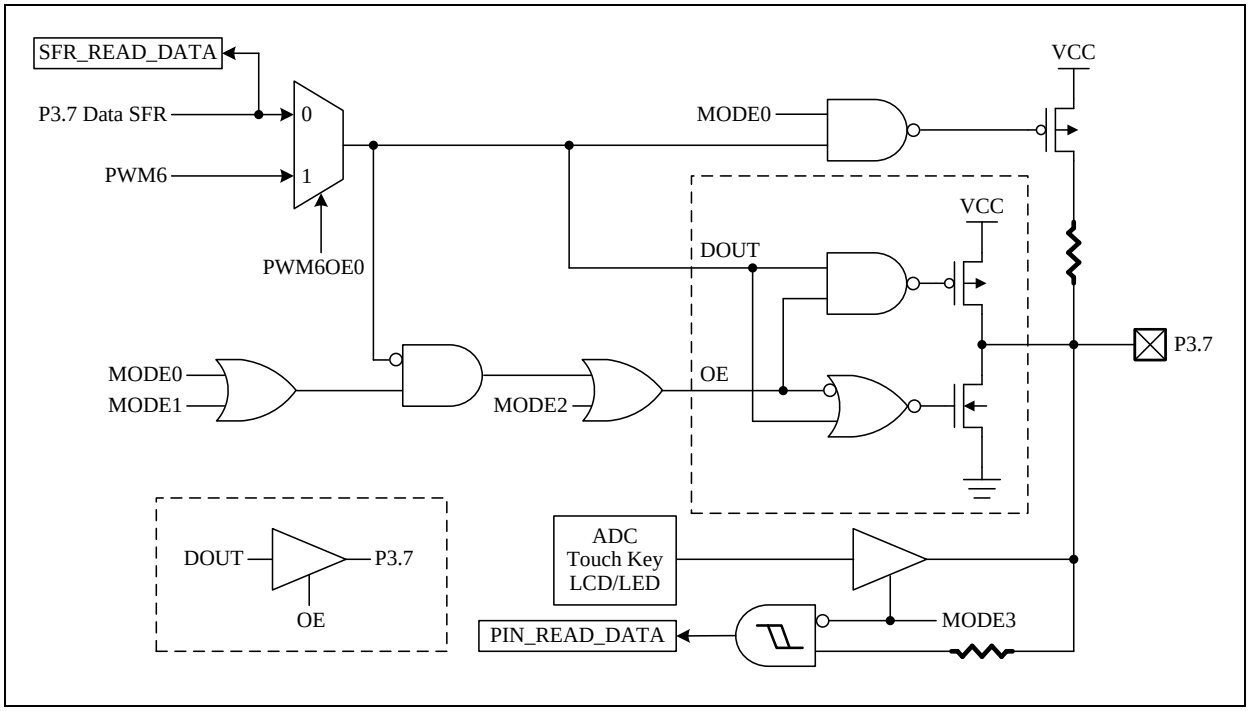
For tables above, a "**CMOS Output**" pin means it can sink and drive at least 4 mA current. It is not recommended to use such pin as input function.

An "**Open Drain**" pin means it can sink at least 4 mA current but only drive a small current (<20 μA). It can be used as input or output function and typically needs an external pull up resistor.

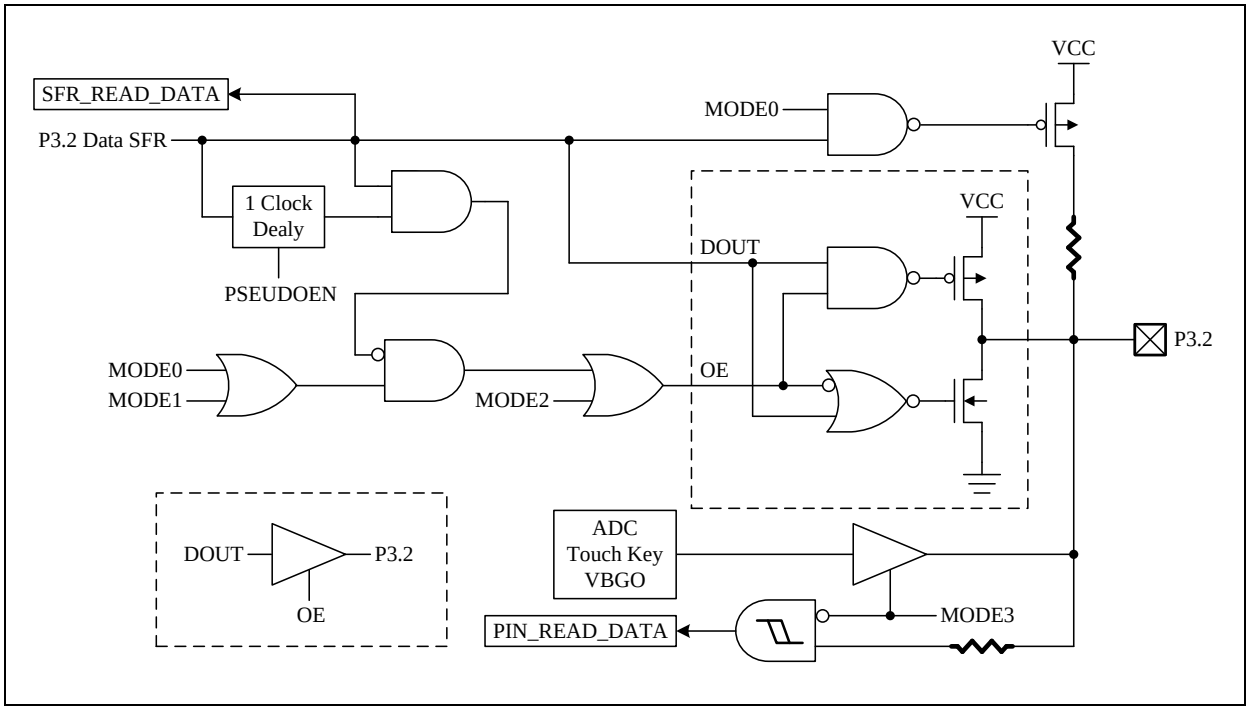
An 8051 standard pin is a "**Pseudo Open Drain**" pin. It can sink at least 4 mA current when output is at low level, and drives at least 4 mA current for 1~2 clock cycle when output transits from low to high, then keeps driving a small current (<20 μA) to maintain the pin at high level. It can be used as input or output function.

Note: *for the necessary SFR setting above, LCD/LED pin has the highest priority. Therefore, if a pin is not used for Segment (ex: pin is I/O, ADC, TK, I^2C, UART and SPI…), S/W must disable the LCD/LED function.*

The chip also supports I/O High-sink function. It is an option and is turned off by default. For efficient control, we divide the High-sink pins into three groups (Group 0: P0.0~P0.3, P2.0~P2.1, P3.4, P3.7; Group 1: P0.6~P0.7, P1.4~P1.7, P3.5~P3.6; Group 2: P0.4~P0.5, P1.0~P1.3, P3.0~P3.3). It is enabled by setting SFR HSNK0EN, HSNK1EN and HSNK2EN.



P3.7 Pin Structure



P3.2 Pin Structure

SFR **80h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

80h.7~0 **P0:** Port0 data

SFR **90h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

90h.7~0 **P1:** Port1 data

SFR **A0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

A0h.1~0 **P2.1~P2.0:** P2.1~P2.0 data

SFR **B0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

B0h.7~0 **P3:** Port3 data

SFR **91h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0MODL	P0MOD3		P0MOD2		P0MOD1		P0MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

91h.7~6 **P0MOD3:** P0.3 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P0.3 is ADC input

91h.5~4 **P0MOD2:** P0.2 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P0.2 is ADC input

91h.3~2 **P0MOD1:** P0.1 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P0.1 is ADC input

91h.1~0 **P0MOD0:** P0.0 pin control
- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P0.0 is ADC input

SFR **92h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0MODH	P0MOD7		P0MOD6		P0MOD5		P0MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

92h.7~6 **P0MOD7:** P0.7 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P0.7 is ADC input

92h.5~4 **P0MOD6:** P0.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P0.6 is ADC input

92h.3~2 **P0MOD5:** P0.5 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P0.5 is ADC input

92h.1~0 **P0MOD4:** P0.4 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P0.4 is ADC input

SFR **A2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODL	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A2h.7~6 **P1MOD3:** P1.3 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.3 is ADC input

A2h.5~4 **P1MOD2:** P1.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.2 is ADC input

A2h.3~2 **P1MOD1:** P1.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.1 is ADC input

A2h.1~0 **P1MOD0:** P1.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.0 is ADC input

SFR **A3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODH	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A3h.7~6 **P1MOD7:** P1.7 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.7 is ADC input

A3h.5~4 **P1MOD6:** P1.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.6 is ADC input

A3h.3~2 **P1MOD5:** P1.5 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.5 is ADC input

A3h.1~0 **P1MOD4:** P1.4 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.4 is ADC input

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2MODL	–	–	–	–	P2MOD1		P2MOD0	
R/W	–	–	–	–	R/W		R/W	
Reset	–	–	–	–	0	1	0	1

93h.3~2 **P2MOD1:** P2.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P2.1 is ADC input

93h.1~0 **P2MOD0:** P2.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P2.0 is ADC input

SFR **A4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODL	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A4h.7~6 **P3MOD3:** P3.3 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.3 is ADC input

A4h.5~4 **P3MOD2:** P3.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.2 is ADC input

A4h.3~2 **P3MOD1:** P3.1 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.1 is ADC input

A4h.1~0 **P3MOD0:** P3.0 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.0 is ADC input

SFR **A5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODH	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A5h.7~6 **P3MOD7:** P3.7 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.7 is ADC input

A5h.5~4 **P3MOD6:** P3.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.6 is ADC input

A5h.3~2 **P3MOD5:** P3.5 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.5 is ADC input

A5h.1~0 **P3MOD4:** P3.4 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.4 is ADC input

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PSEUDOEN	MSI2CPS	UART2PS	UART1PS	TCOE	T2OE	T1OE	T0OE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A6h.7 **PSEUDOEN:** P3.0~P3.2 pseudo open-drain state
0: Disable
1: Enable

A6h.6 **MSI2CPS:** Master/Slave I^2C pin select (SCL/SDA)
0: P3.0/P3.1
1: P0.1/P0.2

A6h.5 **UART2PS:** UART2 Pin Select (TX/RX)
0: P1.7/P3.6
1: P0.3/P0.2

A6h.4 **UART1PS:** UART1 Pin Select (TX/RX)
0: P3.1/P3.0
1: P0.0/P0.1

A6h.3 **TCOE:** System clock signal output (CKO) control
0: Disable "System clock divided by 2" output to P1.4 pin
1: Enable "System clock divided by 2" output to P1.4 pin

A6h.2 **T2OE:** Timer2 signal output (T2O) control
0: Disable "Timer2 overflow divided by 2" output to P1.0 pin
1: Enable "Timer2 overflow divided by 2" output to P1.0 pin

A6h.1 **T1OE:** Timer1 signal output (T1O) control
0: Disable "Timer1 overflow divided by 2" output to P3.5 pin
1: Enable "Timer1 overflow divided by 2" output to P3.5 pin

A6h.0 **T0OE:** Timer0 signal output (T0O) control
0: Disable "Timer0 overflow divided by 64" output to P3.4 pin
1: Enable "Timer0 overflow divided by 64" output to P3.4 pin

SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LXDCON	LXDEN	LXDDUTY			LEDBRITM	LXDBRIT		
R/W	R/W	R/W			R/W	R/W		
Reset	0	0	0	0	0	1	1	1

B1h.7 **LXDEN:** LCD/LED enable control
0: LCD/LED disable
1: LCD/LED enable

SFR **B6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE0	PWM2OE1	PWM2OE0	PWM1OE1	PWM1OE0	PWM0NOE1	PWM0POE1	PWM0NOE0	PWM0POE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B6h.7 **PWM2OE1:** PWM2 control
0: PWM2 disable
1: PWM2 enable and signal output to P3.3 pin

B6h.6 **PWM2OE0:** PWM2 control
0: PWM2 disable
1: PWM2 enable and signal output to P1.5 pin

B6h.5 **PWM1OE1:** PWM1 control
0: PWM1 disable
1: PWM1 enable and signal output to P3.2 pin

B6h.4 **PWM1OE0:** PWM1 control
0: PWM1 disable
1: PWM1 enable and signal output to P1.4 pin

B6h.3 **PWM0NOE1:** PWM0N control
0: PWM0N disable
1: PWM0N enable and signal output to P2.0 pin

B6h.2 **PWM0POE1:** PWM0P control
0: PWM0P disable
1: PWM0P enable and signal output to P2.1 pin

B6h.1 **PWM0NOE0:** PWM0N control
0: PWM0N disable
1: PWM0N enable and signal output to P1.3 pin

B6h.0 **PWM0POE0:** PWM0P control
0: PWM0P disable
1: PWM0P enable and signal output to P1.2 pin

SFR **B7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE1	PWM6OE1	PWM6OE0	PWM5OE1	PWM5OE0	PWM4OE1	PWM4OE0	PWM3OE1	PWM3OE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B7h.7 **PWM6OE1:** PWM6 control
0: PWM6 disable
1: PWM6 enable and signal output to P0.7 pin

B7h.6 **PWM6OE0:** PWM6 control
0: PWM6 disable
1: PWM6 enable and signal output to P3.7 pin

B7h.5 **PWM5OE1:** PWM5 control
0: PWM5 disable
1: PWM5 enable and signal output to P0.6 pin

B7h.4 **PWM5OE0:** PWM5 control
0: PWM5 disable
1: PWM5 enable and signal output to P3.4 pin

B7h.3 **PWM4OE1:** PWM4 control
0: PWM4 disable
1: PWM4 enable and signal output to P0.5 pin

B7h.2 **PWM4OE0:** PWM4 control
0: PWM4 disable
1: PWM4 enable and signal output to P3.5 pin

B7h.1 **PWM3OE1:** PWM3 control
0: PWM3 disable
1: PWM3 enable and signal output to P0.4 pin

B7h.0 **PWM3OE0:** PWM3 control
0: PWM3 disable
1: PWM3 enable and signal output to P1.6 pin

SFR **86h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0LOE	P0LOE7	P0LOE6	P0LOE5	P0LOE4	P0LOE3	P0LOE2	P0LOE1	P0LOE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

86h.7 **P0LOE7:** LCDC07 / LED SEG6 (P0.7) enable control
0: Disable
1: Enable

86h.6 **P0LOE6:** LCDC06 / LED SEG7 (P0.6) enable control
0: Disable
1: Enable

86h.5 **P0LOE5:** LCDC05 (P0.5) enable control
0: Disable
1: Enable

86h.4 **P0LOE4:** LCDC04 (P0.4) enable control
0: Disable
1: Enable

86h.3 **P0LOE3:** LCDC03 / LED COM3 / LED3 (P0.3) enable control
0: Disable
1: Enable

86h.2 **P0LOE2:** LCDC02 / LED COM2 / LED2 (P0.2) enable control
0: Disable
1: Enable

86h.1 **P0LOE1:** LCDC01 / LED COM1 / LED1 (P0.1) enable control
0: Disable
1: Enable

86h.0 **P0LOE0:** LCDC00 / LED COM0 / LED0 (P0.0) enable control
0: Disable
1: Enable

SFR **ACh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1LOE	P1LOE7	P1LOE6	P1LOE5	P1LOE4	P1LOE3	P1LOE2	P1LOE1	P1LOE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

ACh.7 **P1LOE7:** LCDC17 / LED SEG2 (P1.7) enable control
0: Disable
1: Enable

ACh.6 **P1LOE6:** LCDC16 / LED SEG3 (P1.6) enable control
0: Disable
1: Enable

ACh.5 **P1LOE5:** LCDC15 / LED SEG4 (P1.5) enable control
0: Disable
1: Enable

ACh.4 **P1LOE4:** LCDC14 / LED SEG5 (P1.4) enable control
0: Disable
1: Enable

ACh.3 **P1LOE3:** LCDC13 (P1.3) enable control
0: Disable
1: Enable

ACh.2 **P1LOE2:** LCDC12 (P1.2) enable control
0: Disable
1: Enable

ACh.1 **P1LOE1:** LCDC11 (P1.1) enable control
0: Disable
1: Enable

ACh.0 **P1LOE0:** LCDC10 (P1.0) enable control
0: Disable
1: Enable

SFR **8Eh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2LOE	–	–	–	–	–	–	P2LOE1	P2LOE0
R/W	–	–	–	–	–	–	R/W	R/W
Reset	–	–	–	–	–	–	0	0

8Eh.1 **P2LOE1:** LCDC21 / LED COM5 or SEG9 (P2.1) enable control
0: Disable
1: Enable

8Eh.0 **P2LOE0:** LCDC20 / LED COM4 or SEG8 (P2.0) enable control
0: Disable
1: Enable

SFR **B3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3LOE	P3LOE7	P3LOE6	P3LOE5	P3LOE4	P3LOE3	P3LOE2	P3LOE1	P3LOE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B3h.7 **P3LOE7:** LCDC37 / LED COM6 or SEG10 / LED6 (P3.7) enable control
0: Disable
1: Enable

B3h.6 **P3LOE6:** LCDC36 / LED SEG1 (P3.6) enable control
0: Disable
1: Enable

B3h.5 **P3LOE5:** LCDC35 / LED SEG0 (P3.5) enable control
0: Disable
1: Enable

B3h.4 **P3LOE4:** LCDC34 / LED COM7 or SEG11 / LED7 (P3.4) enable control
0: Disable
1: Enable

B3h.3 **P3LOE3:** LCDC33 (P3.3) enable control
0: Disable
1: Enable

B3h.2 **P3LOE2:** LCDC32 (P3.2) enable control
0: Disable
1: Enable

B3h.1 **P3LOE1:** LCDC31 (P3.1) enable control
0: Disable
1: Enable

B3h.0 **P3LOE0:** LCDC30 (P3.0) enable control
0: Disable
1: Enable

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	1	0	0	0	1	1

D8h.7 **SCKTYPE:** Slow clock type. This bit can be changed only in Fast mode (SELFCK=1).
0: SRC
1: SXT, P2.0 and P2.1 are crystal pins

D8h.6 **FCKTYPE:** Fast clock type. This bit can be changed only in Slow mode (SELFCK=0).
0: FRC
1: FXT, P2.0 and P2.1 are crystal pins, oscillator gain is high for FXT

SFR **BCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPCON	SPEN	MSTR	CPOL	CPHA	–	LSBF	SPCR	
R/W	R/W	R/W	R/W	R/W	–	R/W	R/W	
Reset	0	0	0	0	–	0	0	0

BCh.7 **SPEN:** SPI enable
0: SPI disable
1: SPI enable, P1.7, P3.5, P3.6 are SPI functional pins.

SFR **C1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIADR	SA							SIEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	0	0	1	0	0

C1h.0 **SIEN:** Slave I²C enable
0: disable
1: enable

SFR **E1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MICON	MIEN	MIACKO	MIIF	MIACKI	MISTART	MISTOP	MICR	
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	0

E1h.7 **MIEN**: Master I^2C enable
0: disable
1: enable

SFR **EFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX3	–	HSNK2EN	HSNK1EN	HSNK0EN	WARMTIME	–	FJMPE	FJMPS
R/W	–	R/W	R/W	R/W	R/W	–	R/W	R/W
Reset	–	0	0	0	0	–	0	0

8Eh.6 **HSNK2EN:** Pin H-sink enable (Group 2 = P0.4~P0.5, P1.0~P1.3, P3.0~P3.3)
0: Group 2 H-sink disable
1: Group 2 H-sink enable

8Eh.5 **HSNK1EN:** Pin H-sink enable (Group 1 = P0.6~P0.7, P14~P17, P3.5~P3.6)
0: Group 1 H-sink disable
1: Group 1 H-sink enable

8Eh.4 **HSNK0EN:** Pin H-sink enable (Group 0 = P0.0~P0.3, P2.0~P2.1, P3.4, P3.7)
0: Group 0 H-sink disable
1: Group 0 H-sink enable

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W		R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

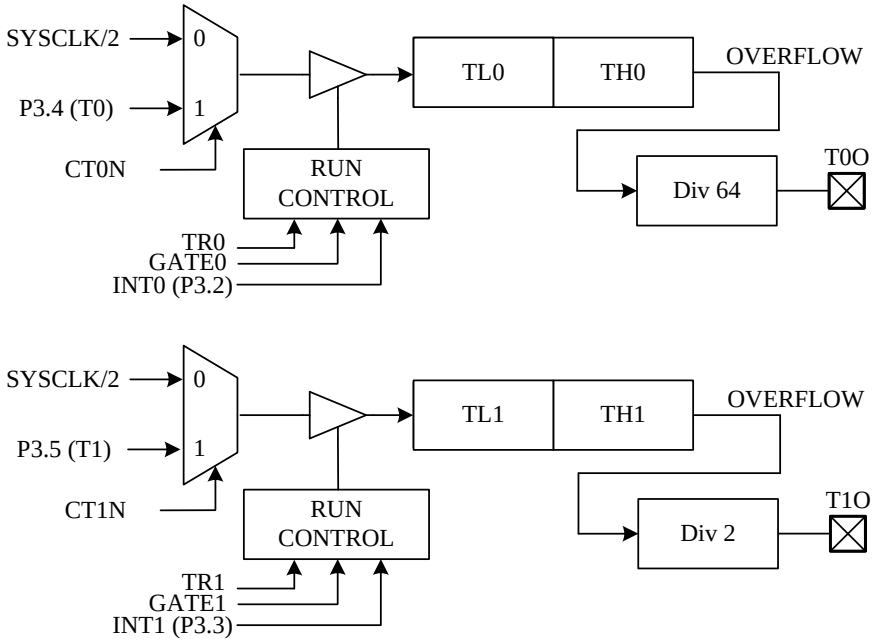
F7h.4 **VBGOUT:** V_{BG} voltage output to P3.2
0: Disable
1: Enable

8. Timers

Timer0, Timer1 and Timer2 are provided as standard 8051 compatible timer/counter. Compare to the traditional 12T 8051, the Chip's Timer0/1/2 use 2 System clock cycle as the time base unit. That is, in timer mode, these timers increase at every "2 System clock" rate; in counter mode, T0/T1/T2 pin input pulse must be wider than 2 System clock to be seen by this device. In addition to the standard 8051 timers function. The T0O pin can output the "Timer0 overflow divided by 64" signal, The T1O pin can output the "Timer1 overflow divided by 2" signal, and the T2O pin can output the "Timer2 overflow divided by 2" signal. Timer3 is provided for a real-time clock count, when its time base is SXT.

8.1 Timer0 / Timer1

TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the Timer0/1, with the timer/counter values stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).



Timer0 and Timer1 Structure

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.7 **TF1:** Timer1 overflow flag
Set by H/W when Timer/Counter 1 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.6 **TR1:** Timer1 run control
0: Timer1 stops
1: Timer1 runs

88h.5 **TF0:** Timer0 overflow flag
Set by H/W when Timer/Counter 0 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.4 **TR0:** Timer0 run control
0: Timer0 stops
1: Timer0 runs

SFR **89h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

89h.7 **GATE1:** Timer1 gating control bit
0: Timer1 enable when TR1 bit is set
1: Timer1 enable only while the INT1 pin is high and TR1 bit is set

89h.6 **CT1N:** Timer1 Counter/Timer select bit
0: Timer mode, Timer1 data increases at 2 System clock cycle rate
1: Counter mode, Timer1 data increases at T1 pin's negative edge

89h.5~4 **TMOD1:** Timer1 mode select
00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow.
11: Timer1 stops

89h.3 **GATE0:** Timer0 gating control bit
0: Timer0 enable when TR0 bit is set
1: Timer0 enable only while the INT0 pin is high and TR0 bit is set

89h.2 **CT0N:** Timer0 Counter/Timer select bit
0: Timer mode, Timer0 data increases at 2 System clock cycle rate
1: Counter mode, Timer0 data increases at T0 pin's negative edge

89h.1~0 **TMOD0:** Timer0 mode select
00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow.
11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.

SFR **8Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL0	TL0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ah.7~0 **TL0:** Timer0 data low byte

SFR **8Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL1	TL1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Bh.7~0 **TL1:** Timer1 data low byte

SFR **8Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH0	TH0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ch.7~0 **TH0:** Timer0 data high byte

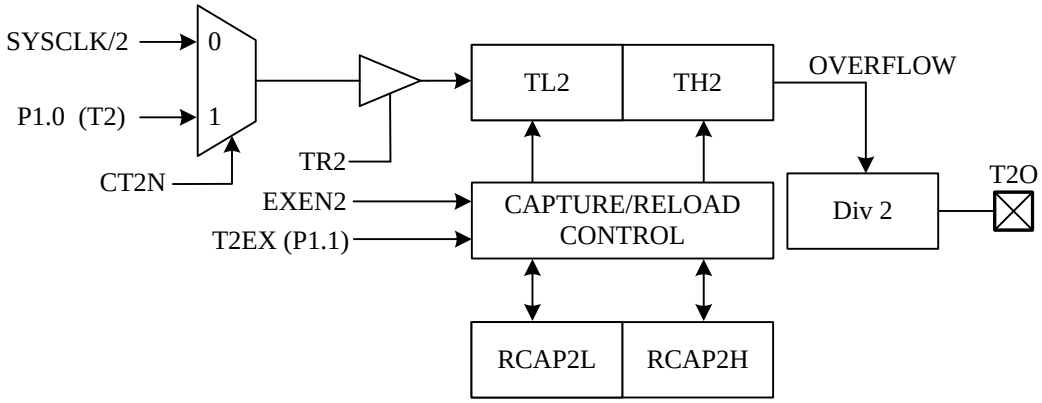
SFR **8Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH1	TH1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Dh.7~0 **TH1:** Timer1 data high byte

***Note**: See also Chapter 6 for more information on Timer0/1 interrupt enable and priority.*
***Note**: See also Chapter 7 for details on T0O, T1O pin output settings.*

8.2 Timer2

Timer2 is controlled through the TCON2 register with the low and high bytes of Timer/Counter2 stored in TL2 and TH2 and the low and high bytes of the Timer2 reload/capture registers stored in RCAP2L and RCAP2H.



Timer2 Structure

SFR **C8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

C8h.7 **TF2:** Timer2 overflow flag
Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.

C8h.6 **EXF2:** T2EX interrupt pin falling edge flag
Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.

C8h.5 **RCLK:** UART receive clock control bit
0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3
1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3

C8h.4 **TCLK:** UART transmit clock control bit
0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3
1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3

C8h.3 **EXEN2:** T2EX pin enable
0: T2EX pin disable
1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0

C8h.2 **TR2:** Timer2 run control
0: Timer2 stops
1: Timer2 runs

C8h.1 **CT2N:** Timer2 Counter/Timer select bit
0: Timer mode, Timer2 data increases at 2 System clock cycle rate
1: Counter mode, Timer2 data increases at T2 pin's negative edge

C8h.0 **CPRL2N:** Timer2 Capture/Reload control bit
0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1.
1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1.
If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.

SFR **CAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2L	RCP2L							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CAh.7~0 **RCP2L:** Timer2 reload/capture data low byte

SFR **CBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2H	RCP2H							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CBh.7~0 **RCP2H:** Timer2 reload/capture data high byte

SFR **CCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL2	TL2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CCh.7~0 **TL2:** Timer2 data low byte

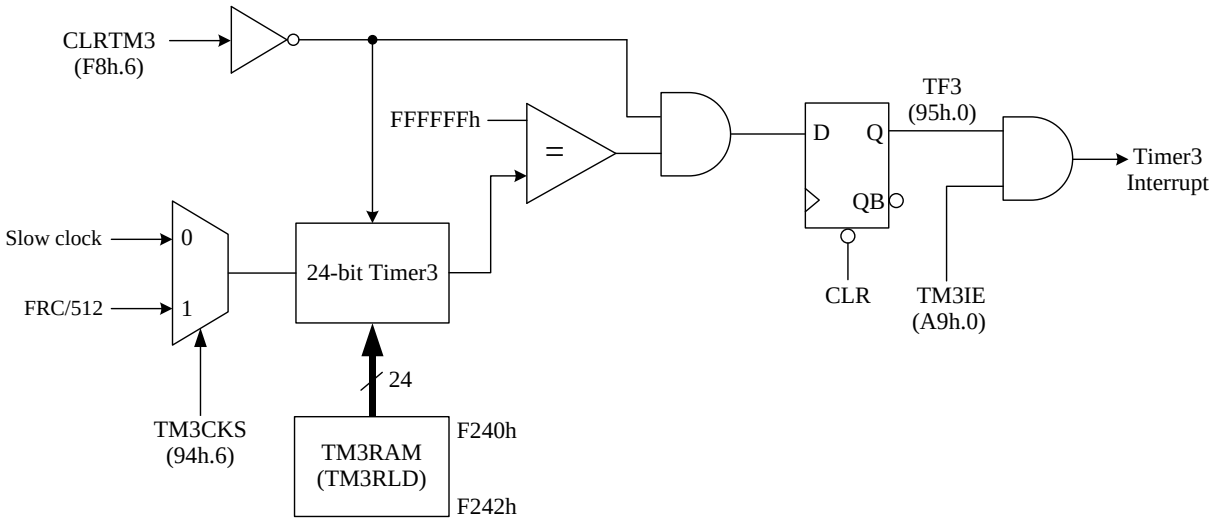
SFR **CDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH2	TH2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CDh.7~0 **TH2:** Timer2 data high byte

***Note**: See also Chapter 6 for more information on Timer2 interrupt enable and priority.*
***Note**: See also Chapter 7 for details on T2O pin output settings.*

8.3 Timer3

Timer3 works as a 24-bit time-base counter, which generates interrupts periodically. Besides, Timer3 increases itself periodically and automatically reloads a new "offset value" (TM3RLD) from TM3RAM while it rolls over and generates an interrupt flag (TF3). The TM3RAM is located in the 8051's External Data Memory space, addressing from F240h to F242h. Timer3 can be stopped counting if the CLRTM3 bit is set. The Timer3 clock source is Slow clock (SRC or SXT) or FRC/512. This is ideal for real-time-clock (RTC) functionality when the clock source is SXT.



Timer3 Structure

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	TKBUFS	TM3CKS	WDTPSC		ADCKS		TKOFC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.6 **TM3CKS:** Timer3 Clock Source select
0: Slow clock (SXT/SRC)
1: FRC/512

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVDIF	–	TKIF	ADIF	–	IE2	PCIF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.0 **TF3:** Timer3 Interrupt Flag
Set by H/W when Timer3 counts to FFFFFFh. Cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit.

Note: *S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.*

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W
Reset	0	0	0	0	1	1	–	0

F8h.6 **CLRTM3:** Set 1 to clear and hold Timer3, need S/W clear.

Note: *also refer to Chapter 6 for more information about Timer3 Interrupt enable and priority.*

8.4 T0O, T1O and T2O Output Control

This device can generate various frequency waveform pin output (in CMOS or Open-Drain format) for Buzzer. The T0O, T1O and T2O waveform is divided by Timer0/Timer1/Timer2 overflow signal. The T0O waveform is Timer0 overflow divided by 64, T1O waveform is Timer1 overflow divided by 2, and T2O waveform is Timer2 overflow divided by 2. User can control their frequency by Timers auto reload speed.

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PSEUDOEN	MSI2CPS	UART2PS	UART1PS	TCOE	T2OE	T1OE	T0OE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A6h.2 **T2OE:** Timer2 signal output (T2O) control
0: Disable "Timer2 overflow divided by 2" output to P1.0 pin
1: Enable "Timer2 overflow divided by 2" output to P1.0 pin

A6h.1 **T1OE:** Timer1 signal output (T1O) control
0: Disable "Timer1 overflow divided by 2" output to P3.5 pin
1: Enable "Timer1 overflow divided by 2" output to P3.5 pin

A6h.0 **T0OE:** Timer0 signal output (T0O) control
0: Disable "Timer0 overflow divided by 64" output to P3.4 pin
1: Enable "Timer0 overflow divided by 64" output to P3.4 pin

9. UARTs

This Chip has two UARTs, UART1 and UART2.

The **UART1** uses SCON and SBUF SFRs. SCON is the control register, SBUF is the data register. Data is written to SBUF for transmission and SBUF is read to obtain received data. The received data and transmitted data registers are completely independent. In the 8051 standard, the calculation of the UART Baud Rate depends on Timer1/Timer2, but the user can also use the UART's independent Timer to define a new Baud Rate by UART1CON.

The **UART2** uses SCON2 and SBUF2 SFRs. SCON2 is the control register, SBUF2 is the data register. Data is written to SBUF2 for transmission and SBUF2 is read to obtain received data. The received data and transmitted data registers are completely independent. The UART2 supports most of the functions of UART, but it does not support Mode0 and Mode2.

F_{SYSCLK} denotes System clock frequency, the UART Baud Rate is calculated as below.

UART1 Baud Rate setting: while SFR **UART1BRS=0 (**Baud Rate set as standard 8051)

- **Mode 0:**
  Baud Rate = $F_{SYSCLK}/2$
- **Mode 1, 3:** if using Timer1 auto reload mode
  Baud Rate = (SMOD + 1) x F_{SYSCLK}/ (32 x 2 x (256 – TH1))
- **Mode 1, 3:** if using Timer2
  Baud Rate = Timer2 overflow rate/16 = F_{SYSCLK}/ (32 x (65536 – RCP2H, RCP2L))
- **Mode 2:**
  Baud Rate = (SMOD + 1) x $F_{SYSCLK}/64$

UART1 Baud Rate setting: while SFR **UART1BRS=1**

- **Mode 0:**
  Baud Rate=$F_{SYSCLK}/2$
- **Mode 1, 3:**
  Baud Rate= F_{SYSCLK} /32/UART1BRP
- **Mode 2:**
  Baud Rate= (SMOD + 1) x $F_{SYSCLK}/64$

UART2 Baud Rate setting:

- **Mode 0, 2:** Invalid
- **Mode 1, 3:**
  Baud Rate= F_{SYSCLK} /32/UART2BRP

Note: *also refer to Chapter 6 for more information about UART Interrupt enable and priority.*

Note: *also refer to Chapter 8 for more information about how Timer2 controls UART clock.*

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.7 **SMOD:** UART1 double Baud Rate control bit
0: Disable UART1 double Baud Rate
1: Enable UART1 double Baud Rate

SFR **98h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

98h.7~6 **SM0,SM1:** UART1 serial port mode select bit 0,1
00: Mode0: 8 bit shift register, Baud Rate=F_{SYSCLK}/2
01: Mode1: 8 bit UART1, Baud Rate is variable
10: Mode2: 9 bit UART1, Baud Rate=F_{SYSCLK}/32 or /64
11: Mode3: 9 bit UART1, Baud Rate is variable

98h.5 **SM2:** Serial port mode select bit 2
SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

98h.4 **REN:** UART1 reception enable
0: Disable reception
1: Enable reception

98h.3 **TB8:** Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3

98h.2 **RB8:** Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit is Mode 1 if SM2=0

98h.1 **TI:** Transmit interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.

98h.0 **RI:** Receive interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

SFR **99h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF	SBUF							
R/W	R/W							
Reset	–	–	–	–	–	–	–	–

99h.7~0 **SBUF:** UART1 transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

SFR **DFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UART1CON	UART1BRS	UART1BRP						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

DFh.7 **UART1BRS:** UART1 Baud Rate source select.
0: 8051 default Baud Rate source select
1: UART1 Baud Rate select as UART1BRP

DFh.6~0 **UART1BRP:** Define UART1 Baud Rate prescaler.
UART1 Baud Rate = F_{SYSCLK}/32/UART1BRP

SFR **8Fh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UART2CON	–	UART2BRP						
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	0	0	0	0	0	0	0

8Fh.6~0 **UART2BRP:** Define UART2 Baud Rate prescaler.
UART2 Baud Rate = F_{SYSCLK}/32/UART2BRP

SFR **9Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON2	SM	–	–	REN2	TB82	RB82	TI2	RI2
R/W	R/W	–	–	R/W	R/W	R/W	R/W	R/W
Reset	0	–	–	0	0	0	0	0

9Ah.7 **SM:** UART2 Serial port mode select bit
0: Mode1: 8 bit UART2, Baud Rate is variable
1: Mode3: 9 bit UART2, Baud Rate is variable
(UART2 does not support Mode0/Mode2)

9Ah.4 **REN2:** UART2 reception enable
0: Disable reception
1: Enable reception

9Ah.3 **TB82:** Transmit Bit 8, the ninth bit to be transmitted in Mode 3

9Ah.2 **RB82:** Receive Bit 8, contains the ninth bit that was received in Mode3

9Ah.1 **TI2:** Transmit interrupt flag
Set by H/W at the beginning of the stop bit in Mode 1 & 3. Must be cleared by S/W.

9Ah.0 **RI2:** Receive interrupt flag
Set by H/W at the sampling point of the stop bit in Mode 1 & 3. Must be cleared by S/W.

SFR **9Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF2	SBUF2							
R/W	R/W							
Reset	–	–	–	–	–	–	–	–

9Bh.7~0 **SBUF2:** UART2 transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	ES2	LVDIE	SPI2CE	ADTKIE	EX2	PCIE	TM3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.6 **ES2:** Serial Port (UART2) interrupt enable
0: Disable Serial Port (UART2) interrupt
1: Enable Serial Port (UART2) interrupt

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PSEUDOEN	MSI2CPS	UART2PS	UART1PS	TCOE	T2OE	T1OE	T0OE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A6h.5 **UART2PS:** UART2 Pin Select (TX/RX)
0: P1.7/P3.6
1: P0.3/P0.2

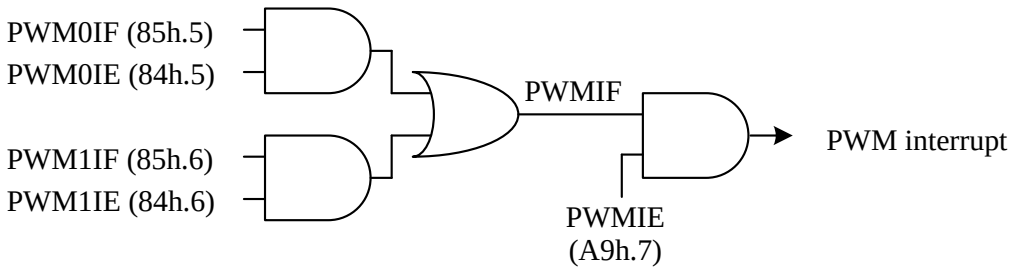
A6h.4 **UART1PS:** UART1 Pin Select (TX/RX)
0: P3.1/P3.0
1: P0.0/P0.1

10. PWMs

This Chip has seven 16-bit PWM modules, PWM0 to PWM6. The PWM can generate varies frequency waveform with 65536 duty resolution on the basis of the PWM clock. The PWM clock can select FRC double frequency (FRC x 2), FRC or F_{SYSCLK} as its clock source. Users should pay attention to the setting; the period of PWM must be greater than duty.

The pin mode SFR controls the PWM output waveform format. Mode1 makes the PWM open drain output and Mode2 makes the PWM CMOS push-pull output. (*see Chapter 7 for detail*)

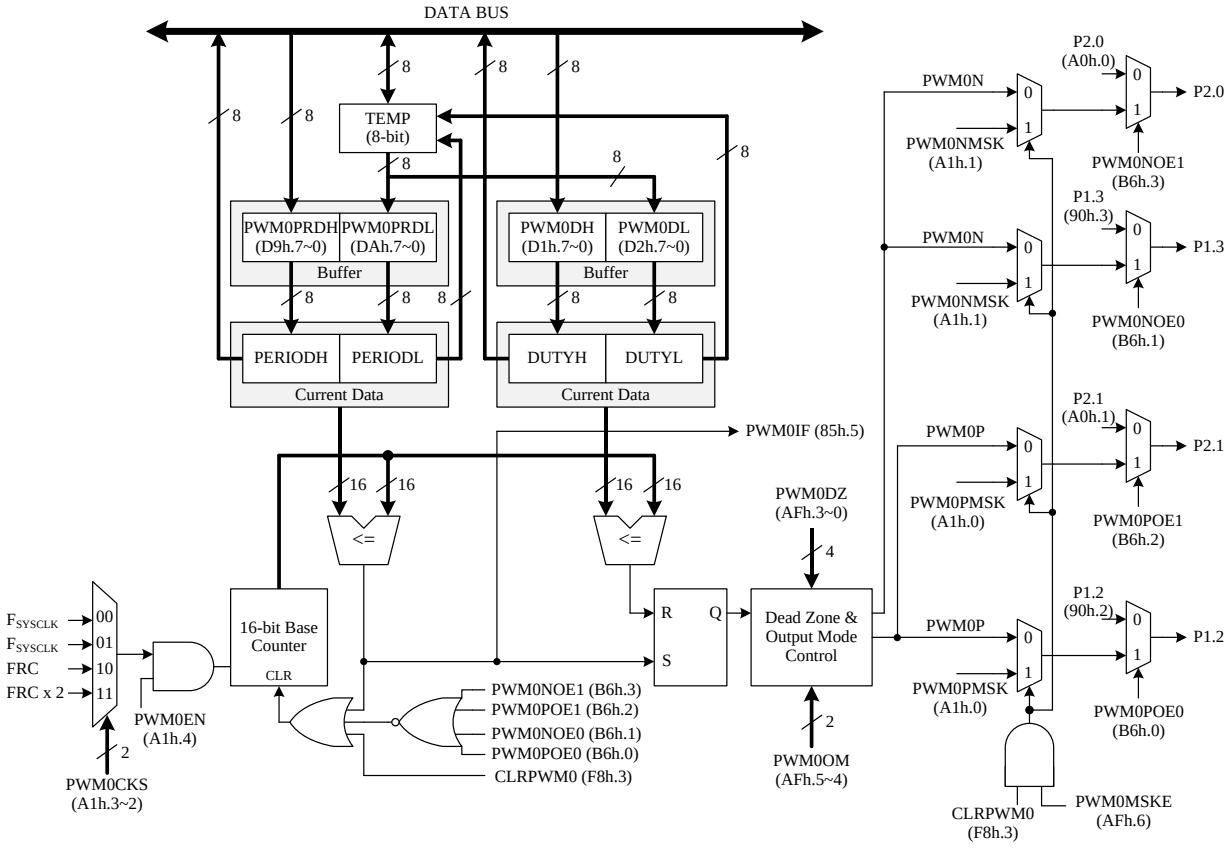
The 16-bit PWM0PRD, PWM1PRD and PWM0D ~ PWM6D registers all have a low and high byte structure. The high bytes can be directly accessed, but as the low bytes can only be accessed via an internal 8-bit buffer, reading or writing to these register pairs must be carried out in a specific way. The important point to notes is that data transfer to and from the 8-bit buffer and its related low byte only takes place when write or read operation to its corresponding high bytes is executed. Briefly speaking, **write low byte first and then high byte; read high byte first and then low byte.**



PWM interrupt structure

10.1 PWM0

The PWM0POE0 and PWM0POE1 are used to select the output for PWM0P, and the PWM0NOE0 and PWM0NOE1 are used to select the output for PWM0N. These four bits also can be PWM0 control bit. If those four bits are cleared, the PWM0 will be cleared and stopped, otherwise the PWM0 is running. The CLRPWM0 bit has the same function. When CLRPWM0 bit is set, the PWM0 will be cleared and held, otherwise the PWM0 is running. The PWM0 structure is shown as follow.



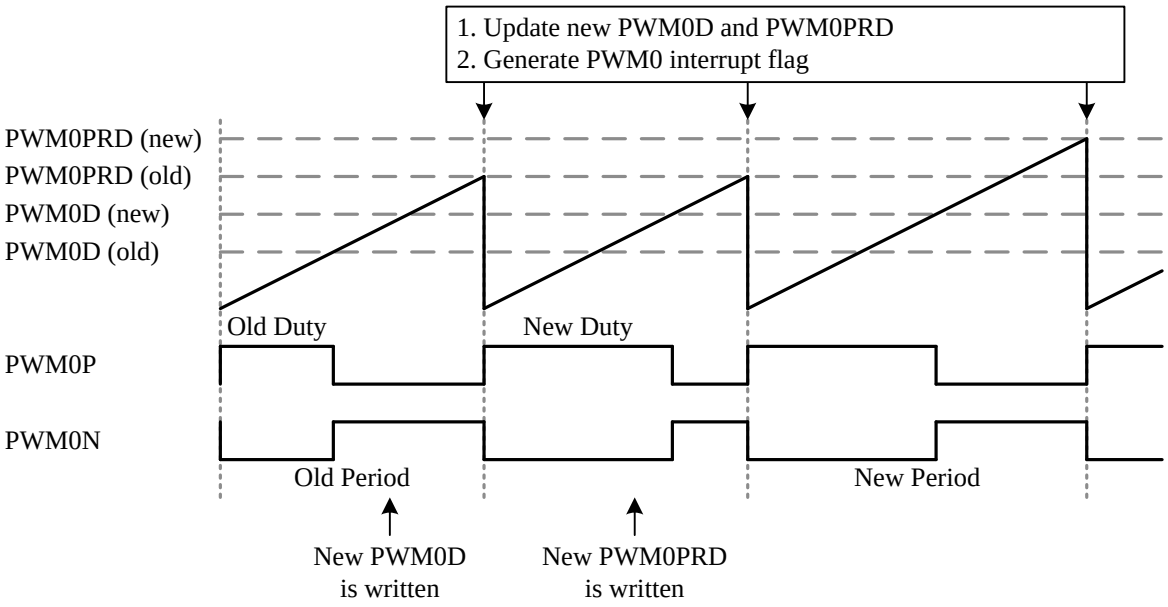
PWM0 Structure

The PWM0 duty cycle can be changed by writing to PWM0DH and PWM0DL. The PWM0 output signal resets to a low level whenever the 16-bit base counter matches the 16-bit PWM0 duty register {PWM0DH, PWM0DL}. The PWM0 period can be set by writing the period value to the PWM0PRDH and PWM0PRDL registers. After writing the PWM0D or PWM0PRD register, the new values will immediately save to their own buffer. H/W will update these values at the end of current period or while PWM0 is cleared. At the end of current period, H/W will set the PWM0IF bit and generate an interrupt if a PWM0 interrupt is enabled.

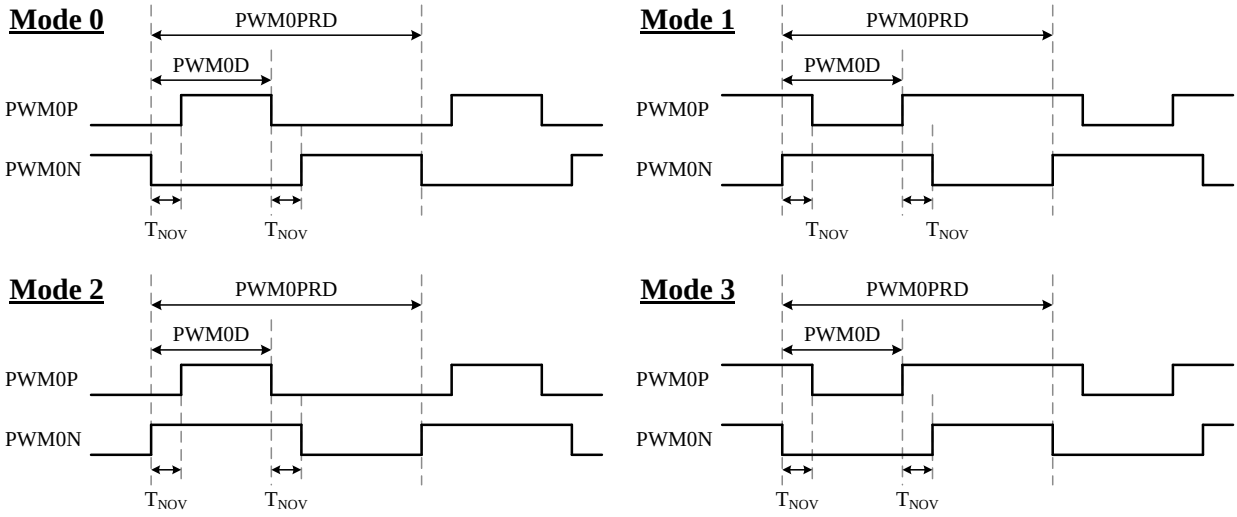
The PWM0 has two operation modes, normal mode and half-bridge mode. PWM0 output signal can be output via PWM0P and PWM0N with four different modes. These two outputs are non-overlapped with time interval T_{NOV}. Non-overlapping time interval is also named as dead zone or dead band. T_{NOV} is determined by setting PWM0DZ bits. The value 0~15 of PWM0DZ map onto 0~15, 16 PWM0CLK cycles respectively. If PWM0DZ=0, PWM0 outputs is directly passed to PWM0P and PWM0N so that waveforms of them have the same duty cycle. Note that, if high pulse width or low pulse width of PWM0 output is shorter than T_{NOV}, the real waveforms of these two outputs will different from the expected waveforms. If the PWM0MSKE bit is set, the outputs can be masked to force output fix signal while S/W set the CLRPWM0 bit is set by H/W.

10.1.1 Normal Mode

The normal mode PWM is a simple structure, which switches its output high and low at uniform repeatable intervals. The PWM0D is the output duty cycle, and the output period is PWM0PRD+1. The output waveform of PWM0 is shown below.



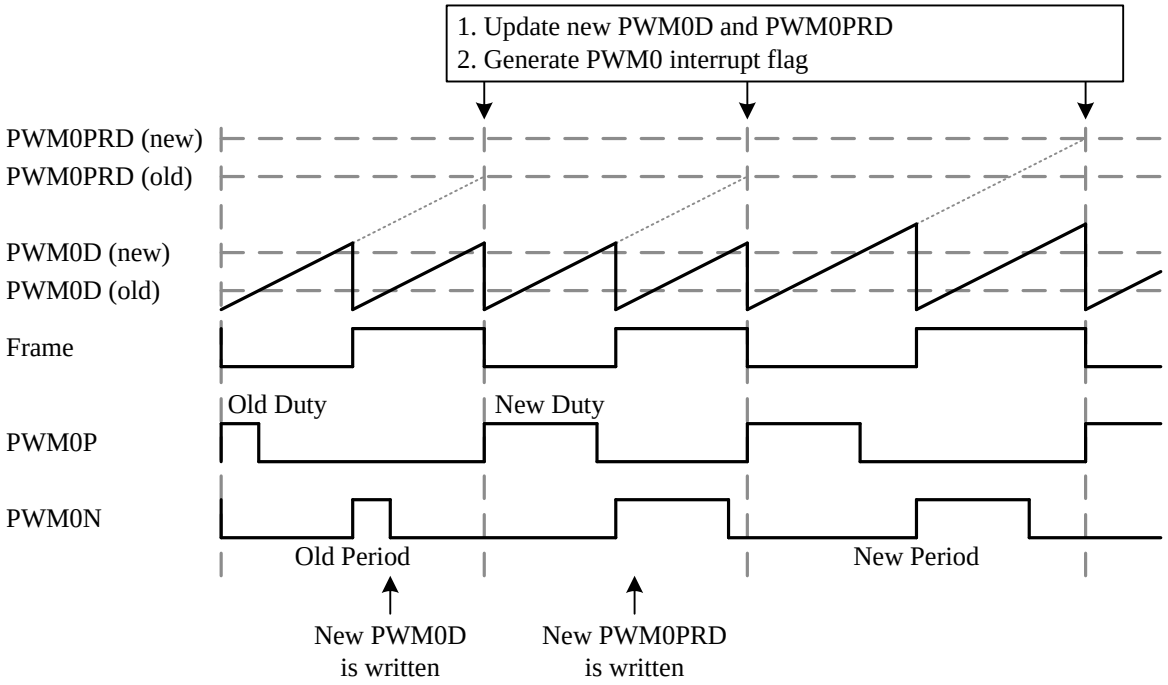
PWM0 normal mode output waveform (PWM0OM=0, PWM0DZ=0)



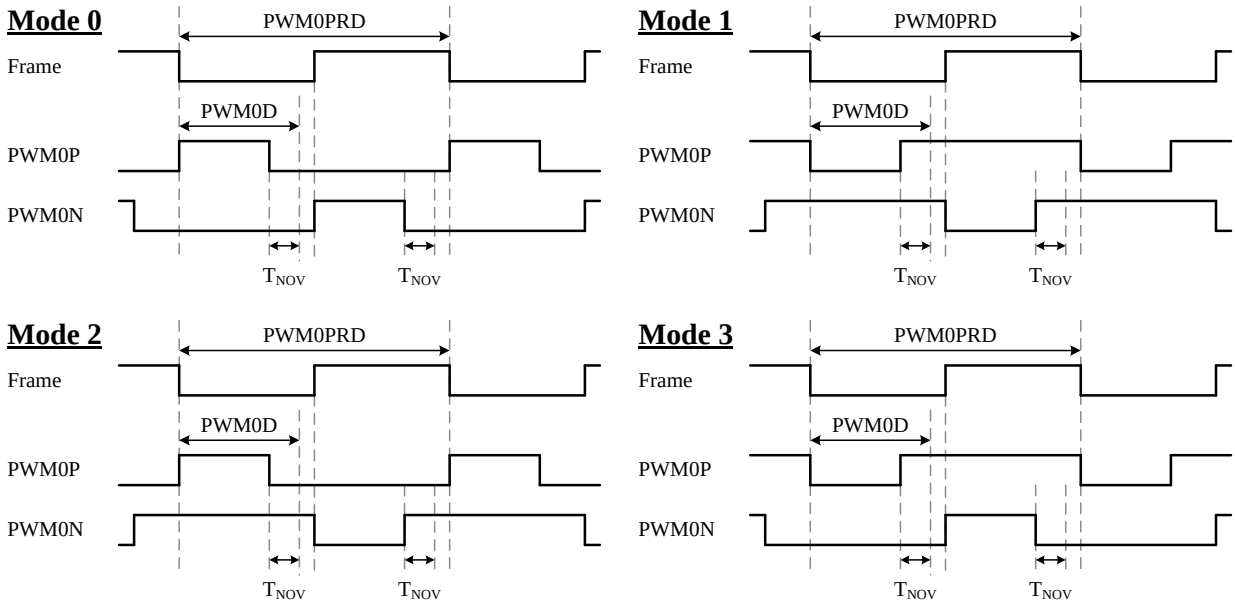
PWM0 normal mode output modes

10.1.2 Half-Bridge Mode

The half-bridge mode PWM is similar to the normal mode but Dead zone is prohibited in half-bridge mode (SFR PWM0DZ must be 0). It has two frames in a period, PWM0P only output in the first frame, PWM0N only output in the second frame. The width of these two frames must be same, so their width is the integer part of PWM0PRD/2. Because each output channel only output in one frame, the maximum duty cycle is same as the width of a frame. If the PWM0D is larger than PWM0PRD/2, H/W will force set the duty cycle to PWM0PRD/2. Following figure shows the output waveform and the output modes.



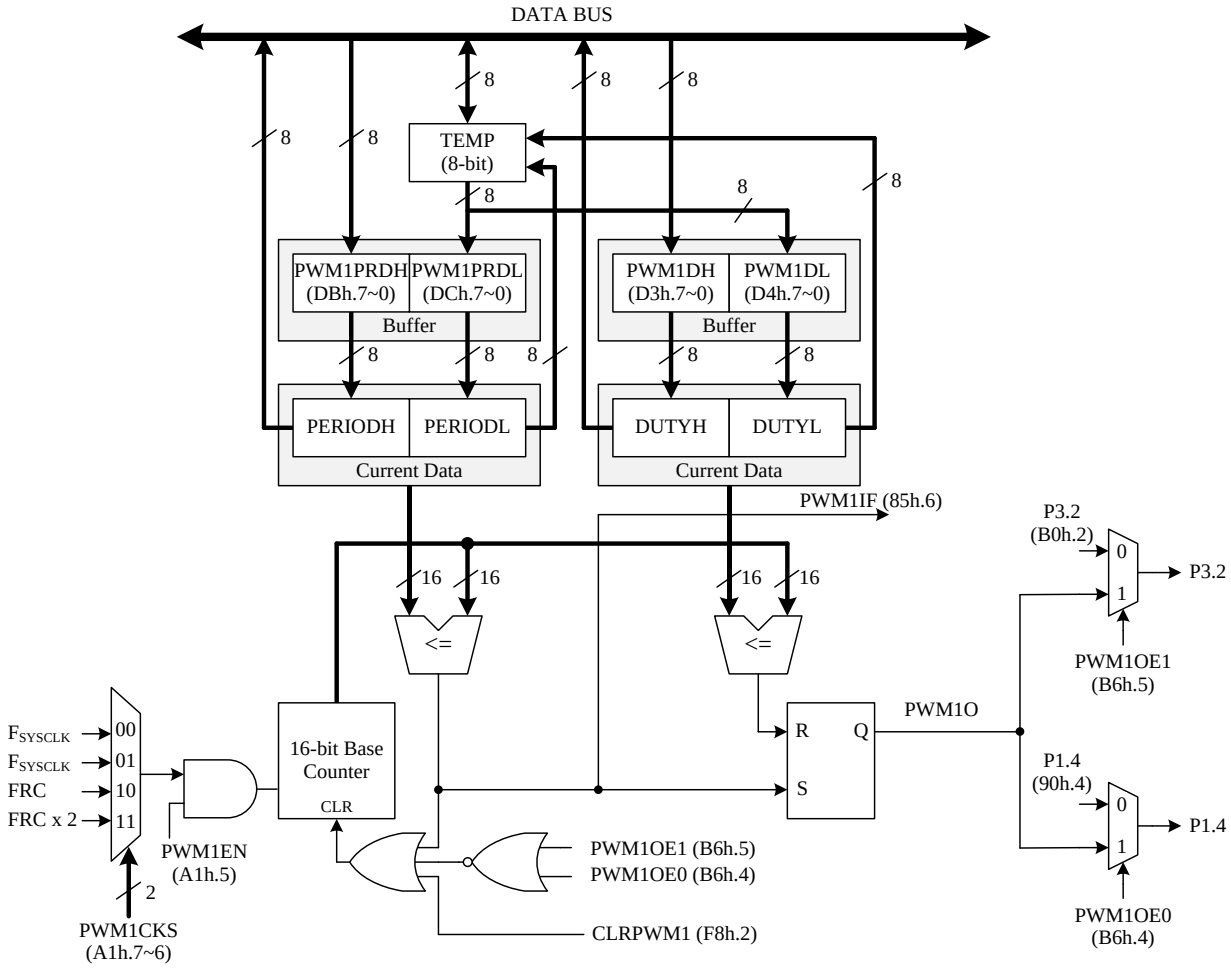
PWM0 half-bridge mode output waveform (PWM0OM=0, PWM0DZ=0)



PWM0 half-bridge mode output modes

10.2 PWM1~PWM6

The Chip has six 16-bit PWM modules PWM1~PWM6. PWM1~6 are sharing period, clock source and interrupt (PWM1IF). The following takes PWM1 as an example for description. The PWM can generate varies frequency waveform with 65536 duty resolution on the basis of the PWM clock. The PWM clock can select double frequency (FRC x 2), FRC or F_{SYSCLK} as its clock source.



PWM1~6 Structure

SFR **84h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE2	–	PWM1IE	PWM0IE	–	–	–	–	–
R/W	–	R/W	R/W	–	–	–	–	–
Reset	–	0	0	–	–	–	–	–

84h.6 **PWM1IE:** PWM1~PWM6 interrupt enable
0: Disable PWM1~PWM6 interrupt
1: Enable PWM1~PWM6 interrupt

84h.5 **PWM0IE:** PWM0 interrupt enable
0: Disable PWM0 interrupt
1: Enable PWM0 interrupt

SFR **85h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG2	–	PWM1IF	PWM0IF	–	–	–	–	–
R/W	–	R/W	R/W	–	–	–	–	–
Reset	–	0	0	–	–	–	–	–

85h.6 **PWM1IF:** PWM1~PWM6 interrupt flag
Set by H/W at the end of PWM1 period, S/W writes BFh to INTFLG2 to clear this flag.

85h.5 **PWM0IF:** PWM0 interrupt enable
Set by H/W at the end of PWM0 period, S/W writes DFh to INTFLG2 to clear this flag.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	ES2	LVDIE	SPI2CE	ADTKIE	EX2	PCIE	TM3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.7 **PWMIE:** PWM0/PWM1~PWM6 interrupt enable
0: Disable PWM0/PWM1~PWM6 interrupt
1: Enable PWM0/PWM1~PWM6 interrupt

SFR **A1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON	PWM1CKS		PWM1EN	PWM0EN	PWM0CKS		PWM0NMSK	PWM0PMSK
R/W	R/W		R/W	R/W	R/W		R/W	R/W
Reset	0	0	0	0	0	0	0	0

A1h.7~6 **PWM1CKS:** PWM1~PWM6 clock source
00: F_{SYSCLK}
01: F_{SYSCLK}
10: FRC
11: FRCx2 (V_{CC}>2.7V)

A1h.5 **PWM1EN:** PWM1~6 enable
0: PWM1~6 disable
1: PWM1~6 enable

A1h.4 **PWM0EN:** PWM0 enable
0: PWM0 disable
1: PWM0 enable

A1h.3~2 **PWM0CKS:** PWM0 clock source
00: F_{SYSCLK}
01: F_{SYSCLK}
10: FRC
11: FRCx2 (V_{CC}>2.7V)

A1h.1 **PWM0NMSK:** PWM0N mask data.
If CLRPWM0=1 and PMW0MSKE=1, PWM0N will output this mask data.

A1h.0 **PWM0PMSK:** PWM0P mask data.
If CLRPWM0=1 and PMW0MSKE=1, PWM0P will output this mask data.

SFR **AFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON2	PWM0MOD	PWM0MSKE	PWM0OM		PWM0DZ			
R/W	R/W	R/W	R/W		R/W			
Reset	0	0	0	0	0	0	0	0

AFh.7 **PWM0MOD:** PWM0 mode select
0: Normal mode
1: Half-bridge mode

AFh.6 **PWM0MSKE:** PWM0 mask output enable
0: Disable
1: Enable, PWM0P/PWM0N output data by PWM0PMSK/PWM0NMSK while CLRPWM0=1

AFh.5~4 **PWM0OM:** PWM0 output mode select
00: Mode0
01: Mode1
10: Mode2
11: Mode3

AFh.3~0 **PWM0DZ:** PWM0 dead zone (Dead zone is prohibited in half-bridge mode)
0000: 0 x T_{PWMCLK}
0001: 1 x T_{PWMCLK}
…
1111: 15 x T_{PWMCLK}

SFR **B6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE0	PWM2OE1	PWM2OE0	PWM1OE1	PWM1OE0	PWM0NOE1	PWM0POE1	PWM0NOE0	PWM0POE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B6h.7 **PWM2OE1:** PWM2 control
0: PWM2 disable
1: PWM2 enable and signal output to P3.3 pin

B6h.6 **PWM2OE0:** PWM2 control
0: PWM2 disable
1: PWM2 enable and signal output to P1.5 pin

B6h.5 **PWM1OE1:** PWM1 control
0: PWM1 disable
1: PWM1 enable and signal output to P3.2 pin

B6h.4 **PWM1OE0:** PWM1 control
0: PWM1 disable
1: PWM1 enable and signal output to P1.4 pin

B6h.3 **PWM0NOE1:** PWM0N control
0: PWM0N disable
1: PWM0N enable and signal output to P2.0 pin

B6h.2 **PWM0POE1:** PWM0P control
0: PWM0P disable
1: PWM0P enable and signal output to P2.1 pin

B6h.1 **PWM0NOE0:** PWM0N control
0: PWM0N disable
1: PWM0N enable and signal output to P1.3 pin

B6h.0 **PWM0POE0:** PWM0P control
0: PWM0P disable
1: PWM0P enable and signal output to P1.2 pin

SFR **B7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE1	PWM6OE1	PWM6OE0	PWM5OE1	PWM5OE0	PWM4OE1	PWM4OE0	PWM3OE1	PWM3OE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B7h.7 **PWM6OE1:** PWM6 control
0: PWM6 disable
1: PWM6 enable and signal output to P0.7 pin

B7h.6 **PWM6OE0:** PWM6 control
0: PWM6 disable
1: PWM6 enable and signal output to P3.7 pin

B7h.5 **PWM5OE1:** PWM5 control
0: PWM5 disable
1: PWM5 enable and signal output to P0.6 pin

B7h.4 **PWM5OE0:** PWM5 control
0: PWM5 disable
1: PWM5 enable and signal output to P3.4 pin

B7h.3 **PWM4OE1:** PWM4 control
0: PWM4 disable
1: PWM4 enable and signal output to P0.5 pin

B7h.2 **PWM4OE0:** PWM4 control
0: PWM4 disable
1: PWM4 enable and signal output to P3.5 pin

B7h.1 **PWM3OE1:** PWM3 control
0: PWM3 disable
1: PWM3 enable and signal output to P0.4 pin

B7h.0 **PWM3OE0:** PWM3 control
0: PWM3 disable
1: PWM3 enable and signal output to P1.6 pin

SFR **D1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DH	PWM0DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D1h.7~0 **PWM0DH:** PWM0 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DL	PWM0DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D2h.7~0 **PWM0DL:** PWM0 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DH	PWM1DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D3h.7~0 **PWM1DH:** PWM1 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DL	PWM1DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D4h.7~0 **PWM1DL:** PWM1 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2DH	PWM2DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D5h.7~0 **PWM2DH:** PWM2 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2DL	PWM2DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D6h.7~0 **PWM2DL:** PWM2 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRDH	PWM0PRDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

D9h.7~0 **PWM0PRDH:** PWM0 period high byte
write sequence: PWMxPRDL then PWMxPRDH
read sequence: PWMxPRDH then PWMxPRDL

SFR **DAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRDL	PWM0PRDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DAh.7~0 **PWM0PRDL:** PWM0 period low byte
write sequence: PWMxPRDL then PWMxPRDH
read sequence: PWMxPRDH then PWMxPRDL

SFR **DBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRDH	PWM1PRDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DBh.7~0 **PWM1PRDH:** PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 period high byte
write sequence: PWMxPRDL then PWMxPRDH
read sequence: PWMxPRDH then PWMxPRDL

SFR **DCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRDL	PWM1PRDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DCh.7~0 **PWM1PRDL:** PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 period low byte
write sequence: PWMxPRDL then PWMxPRDH
read sequence: PWMxPRDH then PWMxPRDL

SFR **DDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3DH	PWM3DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

DDh.7~0 **PWM3DH:** PWM3 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **DEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3DL	PWM3DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

DEh.7~0 **PWM3DL:** PWM3 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **E9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM4DH	PWM4DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

E9h.7~0 **PWM4DH:** PWM4 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **EAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM4DL	PWM4DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

EAh.7~0 **PWM4DL:** PWM4 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **EBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM5DH	PWM5DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

EBh.7~0 **PWM5DH:** PWM5 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **ECh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM5DL	PWM5DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

ECh.7~0 **PWM5DL:** PWM5 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **EDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM6DH	PWM6DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

EDh.7~0 **PWM6DH:** PWM6 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **EEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM6DL	PWM6DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

EEh.7~0 **PWM6DL:** PWM6 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W
Reset	0	0	0	0	1	1	–	0

F8h.3 **CLRPWM0:** PWM0 clear enable
0: PWM0 is running
1: PWM0 is cleared and held

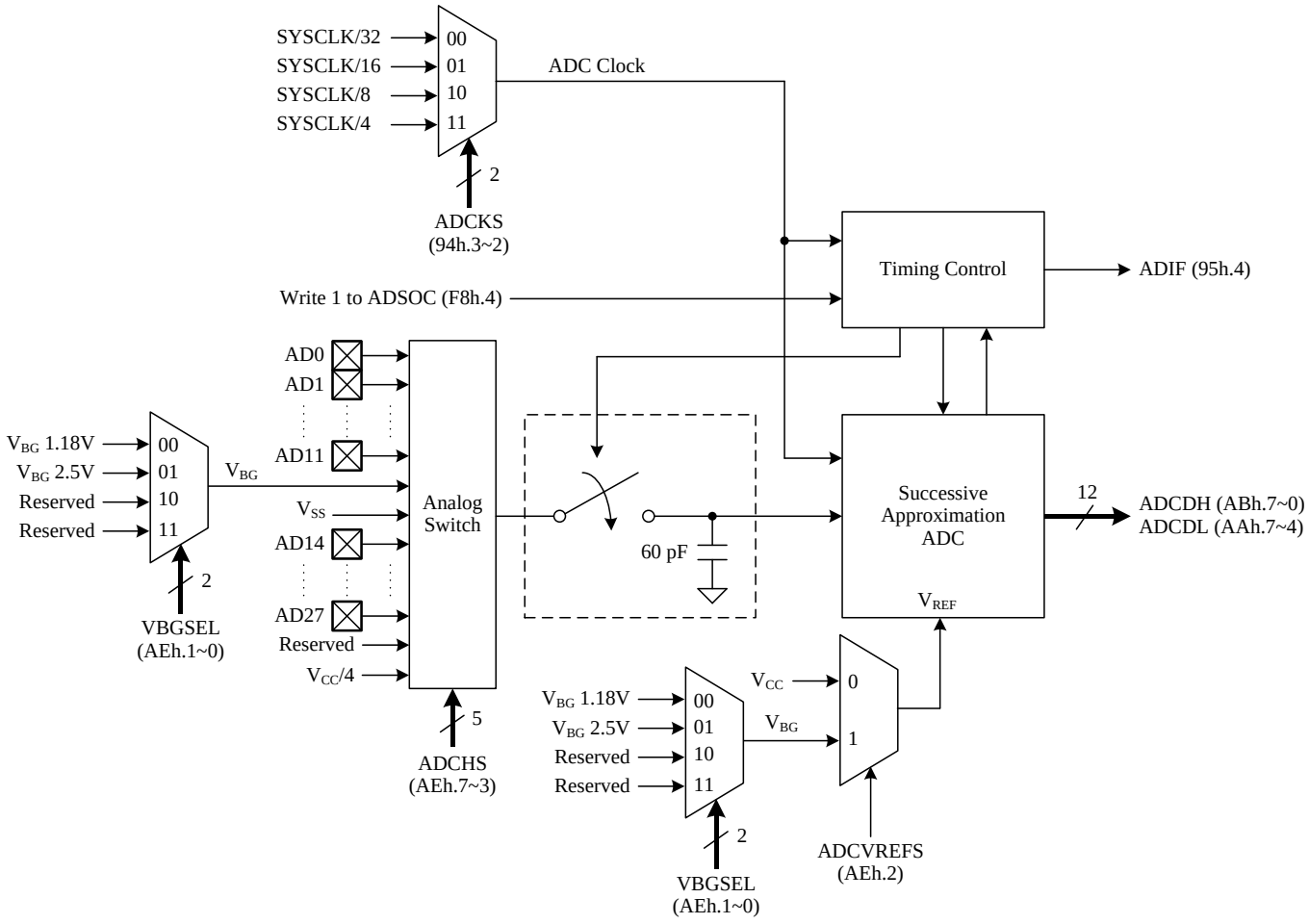
F8h.2 **CLRPWM1:** PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 clear enable
0: PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 is running
1: PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 is cleared and held

11. ADC

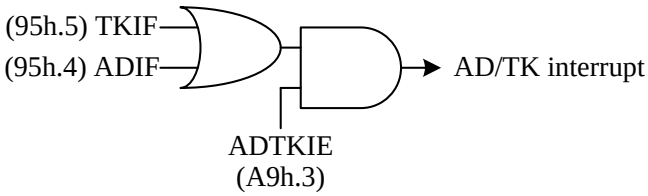
The Chip offers a 12-bit ADC consisting of a 26-channel analog input multiplexer, control register, clock generator, 12-bit successive approximation register, and output data register. Generally, ADC clock frequency is less than 1 MHz, user can refer to Electrical Characteristics Chapter for detail.

To use the ADC, set the ADCKS bits first to choose a proper ADC clock frequency. Then, user launch the ADC conversion by setting the ADSOC bit, and H/W will automatic clear it at the end of the conversion. After the end of the conversion, H/W will set the ADIF bit and generate an interrupt if an ADC interrupt is enabled. The ADIF bit can be cleared by writing 0 to this bit or set ADSOC bit. The analog input level must remain within the range from V_{SS} to V_{CC}.

Using the ADCVREFS option, the ADC internal reference voltage source (V_{REF}) can be selected as V_{CC} or V_{BG}.



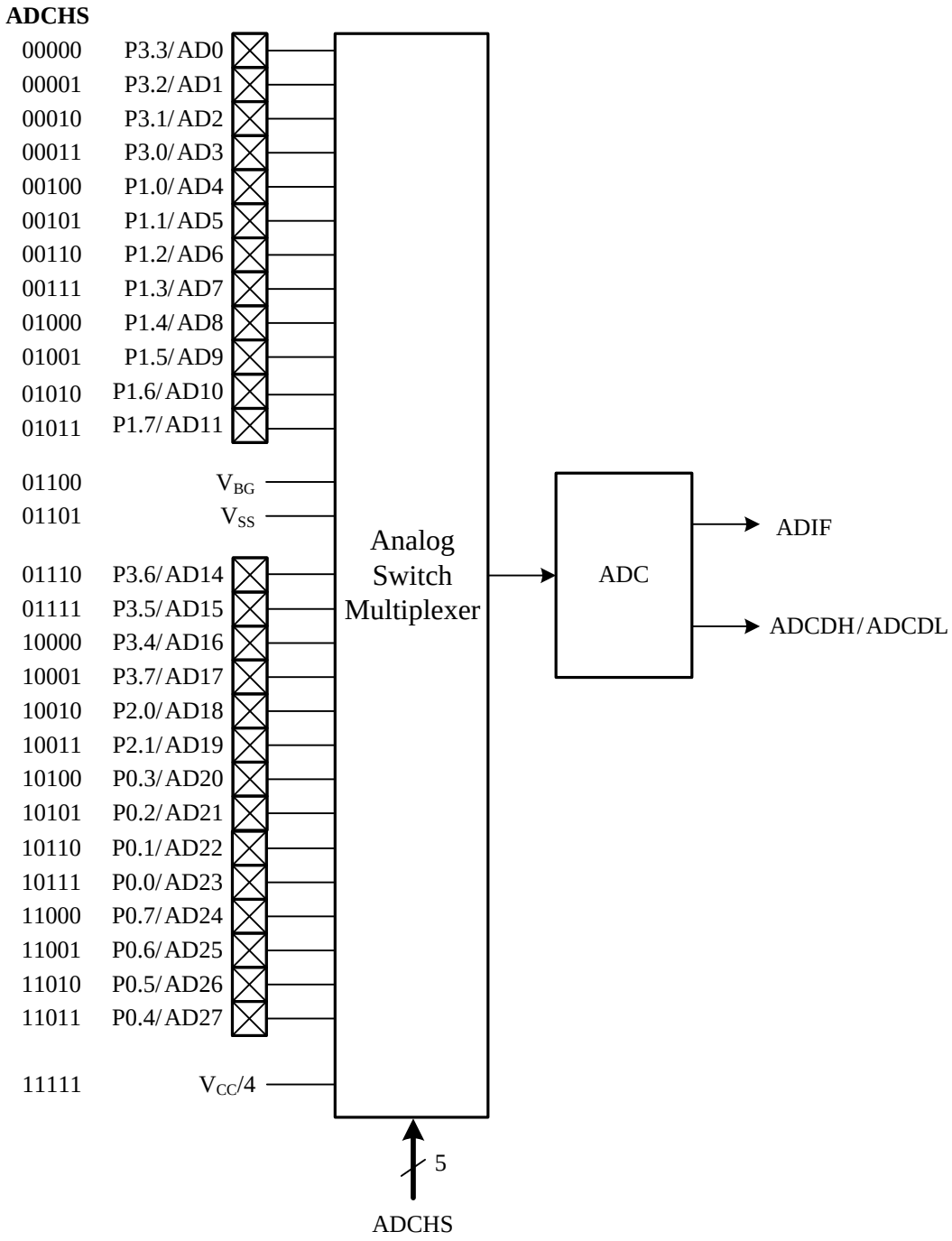
ADC Structure



ADC Interrupt Structure

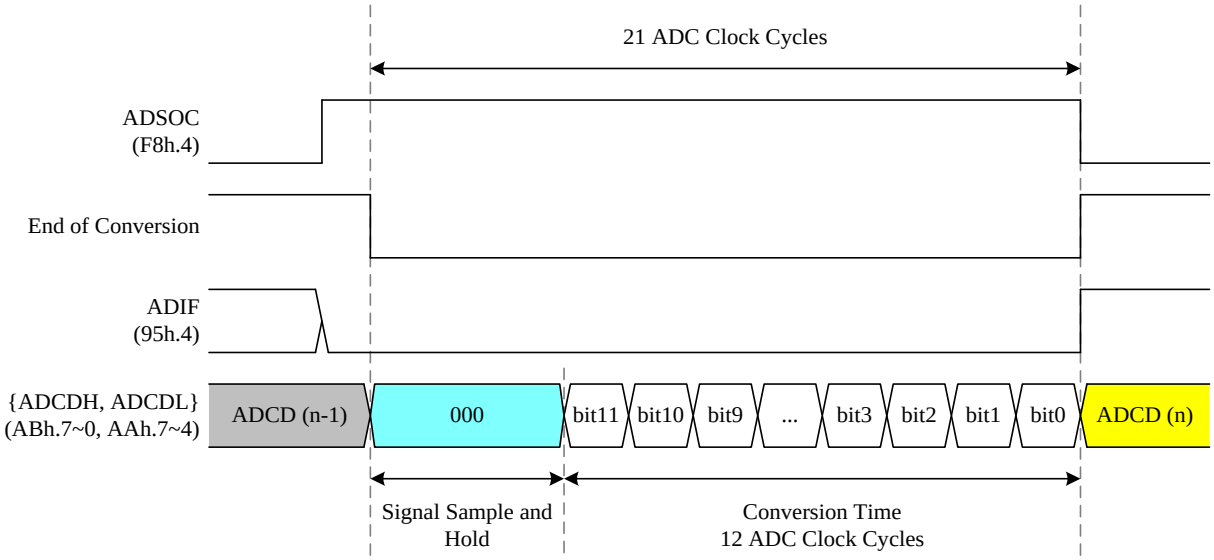
11.1 ADC Channels

The ADC channels are connected to the analog input pins via the analog switch multiplexer. The analog switch multiplexer is controlled by ADCHS register. The Chip offers up to 26 I/O input pins, designated AD0~AD11, AD14~AD21. In addition, there are 2 internal reference voltages (V_{BG} and $V_{CC}/4$). When ADCHS is set to 1100b, the analog input will connect to V_{BG}, and when ADCHS is set to 1101b, the analog input will connect to V_{SS}.



11.2 ADC Conversion Time

The conversion time is the time required for the ADC to convert the voltage. The ADC requires two ADC clock cycles to convert each bit and several clock cycles to sample and hold the input voltage. A total of 21 ADC clock cycles are required to perform the complete conversion. When the conversion time is complete, the ADIF interrupt flag is set by H/W, and the result is loaded into the ADCDH and ADCDL registers of the 12-bit A/D result.



SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	TKBUFS	TM3CKS	WDTPSC		ADCKS		TKOFC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.3~2 **ADCKS:** ADC clock rate select

00: $F_{SYSCLK}/32$

01: $F_{SYSCLK}/16$

10: $F_{SYSCLK}/8$

11: $F_{SYSCLK}/4$

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVDIF	–	TKIF	ADIF	–	IE2	PCIF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.4 **ADIF:** ADC interrupt flag

Set by H/W at the end of ADC conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.

Note: *S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.*

SFR **AAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDL	ADCDL				–	–	–	PWRDEC
R/W	R				–	–	–	W
Reset	–	–	–	–	–	–	–	–

AAh.7~4 **ADCDL:** ADC data bit 3~0

SFR **ABh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDH	ADCDH							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ABh.7~0 **ADCDH:** ADC data bit 11~4

SFR **AEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCHSEL	ADCHS					ADCVREFS	VBGSEL	
R/W	R/W					R/W	R/W	
Reset	1	1	1	0	0	0	0	0

AEh.7~3 **ADCHS:** ADC channel select

00000: AD0 (P3.3)
00001: AD1 (P3.2)
00010: AD2 (P3.1)
00011: AD3 (P3.0)
00100: AD4 (P1.0)
00101: AD5 (P1.1)
00110: AD6 (P1.2)
00111: AD7 (P1.3)
01000: AD8 (P1.4)
01001: AD9 (P1.5)
01010: AD10 (P1.6)
01011: AD11 (P1.7)
01100: V_{BG}
01101: V_{SS}
01110: AD14 (P3.6)
01111: AD15 (P3.5)
10000: AD16 (P3.4)
10001: AD17 (P3.7)
10010: AD18 (P2.0)
10011: AD19 (P2.1)
10100: AD20 (P0.3)
10101: AD21 (P0.2)
10110: AD22 (P0.1)
10111: AD23 (P0.0)
11000: AD24 (P0.7)
11001: AD25 (P0.6)
11010: AD26 (P0.5)
11011: AD27 (P0.4)
others: Reserved
11111: $V_{CC}/4$

AEh.2 **ADCVREFS:** ADC reference voltage select

0: V_{CC}
1: V_{BG}

AEh.1~0 **VBGSEL:** V_{BG} voltage select. When ADCVREF is selected as V_{BG}, VBGSEL is prohibited from using 1.18V.

00: 1.18V
01: 2.5V (need V_{CC}>2.8V)
10: Reserved
11: Reserved

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	CLRPWM1	OPOUT	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	0	0

F8h.4 **ADSOC:** Start ADC conversion

Set the ADSOC bit to start ADC conversion, and the ADSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.

Note: *See also Chapter 6 for more information on ADC interrupt enable and priority.*

Note: *Also refer to Chapter 7 for details on ADC pin input settings.*

12. Touch Key (FTK)

The Touch Key offers an easy simple and reliable method to implement finger touch detection. During the key scan operation, the device support a 23 channels touch key detection.

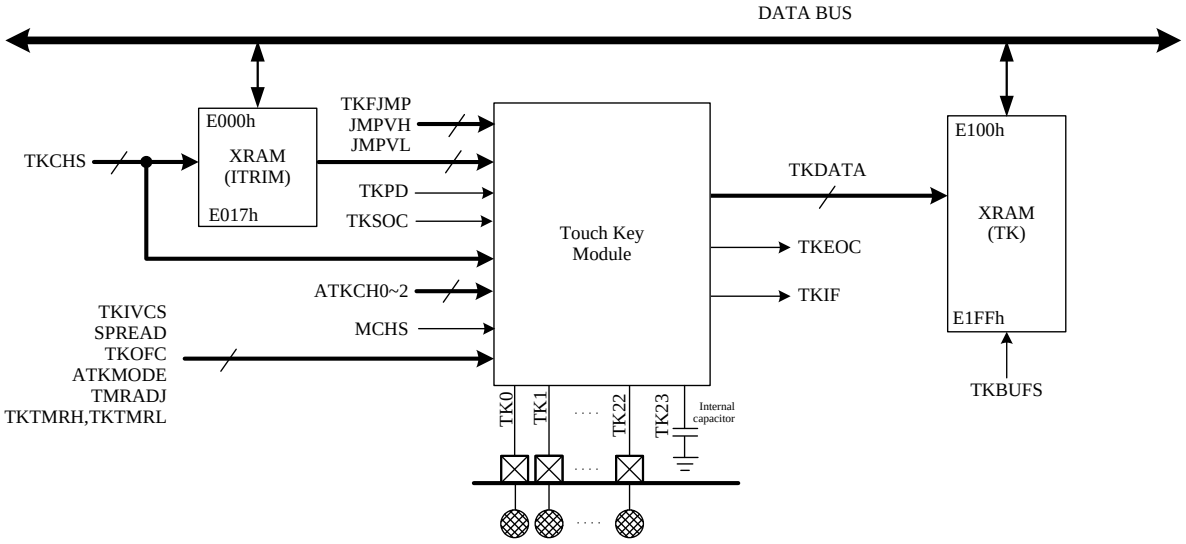
To use the Touch Key, user should setup correctly. There are two ways to set I/O as TK channel. Set Pin Mode as Mode3 or set SFR ATKCH0~2 to force I/O as TK channel automatically when TK scanning. If ATKCH0~2 are set, the corresponding I/O pins will be set as TK channels when TK scanning and will no longer be affected by PxMODL and PxMODH.

TKPINSEL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKCH0	TK7	TK6	TK5	TK4	TK3	TK2	TK1	TK0
ATKCH1	TK15	TK14	TK13	TK12	TK11	TK10	TK9	TK8
ATKCH2	TKCAP	TK22	TK21	TK20	TK19	TK18	TK17	TK16

Set ATKCH0~2 to choose I/O as TK channel

In the TK Mode, user assigns TKPD=0 to turn on the TK module, then set the TKSOC bit to start touch key conversion, and user need to clear TKSOC manually. TKEOC=0 means conversion is in process. TKEOC=1 means the conversion is finish, and the touch key counting result is stored into the TKRAM. After TKEOC=1, user must wait at least 50 μs for next conversion. Reducing/increasing TKTMR can reduce/increase the TKDATA to accommodate the condition of the system.

The FTK has an internal built-in reference capacitor to simulate the KEY behavior. Set TKCHS=23 and start the scanning can get the TK Data Count of internal reference capacitor (TKCAP). Since the internal capacitor would not be affected by water or mobile phone, it is useful for comparing the environment background noise. Setting the TKFJMP, the frequency of Touch Key clock can be change automatically by H/W controlled while ATKMODE =1 or 2. It may help to improve the ability to resist noise.



FTK Structure

SFR ATKCH0~2 are used to specify scan TK channel, and each bit is mapped to TK pin. TK scan will scan from low bit to high bit. If ATKMODE=0, TK can scan up to 24 channels, TK00~TK22 and TKCAP (TK23), each channel is scanned once. If ATKMODE=1, TK can scan up to 24 channels, each channel is scanned twice. If ATKMODE=2, TK can scan up to 16 channels, each channel is scanned 4 times. If ATKMODE=3, TK can scan up to 8 channels, each channel is scanned 8 times. TKCHS is used to specify the first channel for TK to start scanning.

For example:

Condition ATKMODE=0, scan TK16/TK14/TK8/TK7/TK6/TK2

⇨ ATKCH2=0000_0001, ATKCH1=0100_0001, ATKCH0=1100_0100

⇨ TKCHS=0x02 (Specify the first scan channel)

⇨ TKBUFS=0 (stored TK data to TKRAM's 1st half)

The arrangement of TK data stored in TKRAM is as follows.

	TKRAM
E100h	TK0 DATAL
E101h	TK0 DATAH
E102h	TK1 DATAL
E103h	TK1 DATAH
	…
E128h	TK20 DATAL
E129h	TK20 DATAH
	…
E12Eh	TK23 DATAL
E12Fh	TK23 DATAH

Condition ATKMODE=1, scan TK16/TK14/TK8/TK7/TK6/TK2

⇨ ATKCH2=0000_0001, ATKCH1=0100_0001, ATKCH0=1100_0100

⇨ TKCHS=0x02 (Specify the first scan channel)

⇨ TKBUFS=0 (stored TK data to TKRAM's 1st half)

The arrangement of TK data stored in TKRAM is as follows.

	TKRAM
E100h	TK2 1st DATAL
E101h	TK2 1st DATAH
E102h	TK2 2nd DATAL
E103h	TK2 2nd DATAH
E104h	TK6 1st DATAL
E105h	TK6 1st DATAH
E106h	TK6 2nd DATAL
E107h	TK6 2nd DATAH
	…
E114h	TK16 1st DATAL
E115h	TK16 1st DATAH
E116h	TK16 2nd DATAL
E117h	TK16 2nd DATAH

The TK scan result is 16-bit data, which are DATAH 8-bit and DATAL 8-bit. DATAH/L must be read in order to get the correct 16-bit data: first read the low byte (DATAL), then read the high word byte (DATAH).

Condition ATKMODE=2, scan TK16/TK14/TK8/TK7/TK6/TK2

- ⇨ ATKCH2=0000_0001, ATKCH1=0100_0001, ATKCH0=1100_0100
- ⇨ TKCHS=0x02 (Specify the first scan channel)
- ⇨ TKBUFS=0 (stored TK data to TKRAM's 1st half)

The arrangement of TK data stored in TKRAM is as follows.

	TKRAM
E100h	TK2 1st DATAL
E101h	TK2 1st DATAH
E102h	TK2 2nd DATAL
E103h	TK2 2nd DATAH
E104h	TK2 3rd DATAL
E105h	TK2 3rd DATAH
E106h	TK2 4th DATAL
E107h	TK2 4th DATAH
E108h	TK6 1st DATAL
E109h	TK6 1st DATAH
E10Ah	TK6 2nd DATAL
E10Bh	TK6 2nd DATAH
E10Ch	TK6 3rd DATAL
E10Dh	TK6 3rd DATAH
E10Eh	TK6 4th DATAL
E10Fh	TK6 4th DATAH
	…
E128h	TK16 1st DATAL
E129h	TK16 1st DATAH
E12Ah	TK16 2nd DATAL
E12Bh	TK16 2nd DATAH
E12Ch	TK16 3rd DATAL
E12Dh	TK16 3rd DATAH
E12Eh	TK16 4th DATAL
E12Fh	TK16 4th DATAH

The TK scan result is 16-bit data, which are DATAH 8-bit and DATAL 8-bit. DATAH/L must be read in order to get the correct 16-bit data: first read the low byte (DATAL), then read the high word byte (DATAH).

Condition ATKMODE=3, scan TK16/TK14/TK8/TK7/TK6/TK2

- ⇨ ATKCH2=0000_0001, ATKCH1=0100_0001, ATKCH0=1100_0100
- ⇨ TKCHS=0x02 (Specify the first scan channel)
- ⇨ TKBUFS=1 (stored TK data to TKRAM's 2nd half)

The arrangement of TK data stored in TKRAM is as follows.

	TKRAM
E180h	TK2 1st DATAL
E181h	TK2 1st DATAH
E182h	TK2 2nd DATAL
E183h	TK2 2nd DATAH
E184h	TK2 3rd DATAL
E185h	TK2 3rd DATAH
E186h	TK2 4th DATAL
E187h	TK2 4th DATAH
E188h	TK2 5th DATAL
E189h	TK2 5th DATAH
E18Ah	TK2 6th DATAL
E18Bh	TK2 6th DATAH
E18Ch	TK2 7th DATAL
E18Dh	TK2 7th DATAH
E18Eh	TK2 8th DATAL
E18Fh	TK2 8th DATAH
	…
E1D0h	TK16 1st DATAL
E1D1h	TK16 1st DATAH
E1D2h	TK16 2nd DATAL
E1D3h	TK16 2nd DATAH
E1D4h	TK16 3rd DATAL
E1D5h	TK16 3rd DATAH
E1D6h	TK16 4th DATAL
E1D7h	TK16 4th DATAH
E1D8h	TK16 5th DATAL
E1D9h	TK16 5th DATAH
E1DAh	TK16 6th DATAL
E1DBh	TK16 6th DATAH
E1DCh	TK16 7th DATAL
E1DDh	TK16 7th DATAH
E1DEh	TK16 8th DATAL
E1DFh	TK16 8th DATAH

The TK scan result is 16-bit data, which are DATAH 8-bit and DATAL 8-bit. DATAH/L must be read in order to get the correct 16-bit data: first read the low byte (DATAL), then read the high word byte (DATAH).

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	TKBUFS	TM3CKS	WDTPSC		ADCKS		TKOFC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.7 **TKBUFS:** TKRAM Ping-Pong buffer select
0: HW stored TKDATA to TKRAM's 1st half (E100h~E17Fh)
1: HW stored TKDATA to TKRAM's 2nd half (E180h~E1FFh)

94h.1~0 **TKOFC:** TK ICLD capacitor select
00: the smallest
11: the biggest

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVDIF	–	TKIF	ADIF	–	IE2	PCIF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.5 **TKIF:** Touch Key Interrupt Flag
Set by H/W at the end of Touch Key conversion if F_{SYSCLK} is fast enough. S/W writes DFh to INTFLG or sets the TKSOC bit to clear this flag.

SFR **A7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKCHS	–	–	–	TKCHS				
R/W	–	–	–	R/W				
Reset	–	–	–	1	1	1	1	1

A7h.4~0 **TKCHS:** Touch Key channel select
00000: TK0 (P3.3)
00001: TK1 (P3.2)
00010: TK2 (P3.1)
00011: TK3 (P3.0)
00100: TK4 (P1.0)
00101: TK5 (P1.1)
00110: TK6 (P1.2)
00111: TK7 (P1.3)
01000: TK8 (P1.4)
01001: TK9 (P1.5)
01010: TK10 (P1.6)
01011: TK11 (P1.7)
01100: TK12 (P3.6)
01101: TK13 (P3.5)
01110: TK14 (P3.4)
01111: TK15 (P3.7)
10000: TK16 (P2.0)
10001: TK17 (P2.1)
10010: TK18 (P0.3)
10011: TK19 (P0.7)
10100: TK20 (P0.6)
10101: TK21 (P0.5)
10110: TK22 (P0.4)
10111: TK reference capacitor
others: Reserved

SFR **ADh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKCON	TKPD	TKEOC	TMRADJ	TKIVCS	SPREAD	MCHS	ATKMODE	
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Reset	1	1	0	1	0	0	0	0

ADh.7 **TKPD:** Touch Key power down (Auto disable in Idle/Halt/Stop mode when Touch Key end of conversion)
0: Touch Key enable
1: Touch Key disable

ADh.6 **TKEOC:** Touch Key end of conversion flag, TKEOC may have 3 us delay after TKSOC=1, so F/W must wait enough time before polling this Flag.
0: Indicates conversion is in progress
1: Indicates conversion is finished

ADh.5 **TMRADJ:** Touch Key scan length auto-adjustment selection
0: TK scan length define by TKTMR[11:0]
1: TK scan length auto-adjustment

ADh.4 **TKIVCS:** Touch Key internal voltage control select
0: V_{CHG}=2.8V; V_{INT}=1.4V
1: V_{CHG}=3.6V; V_{INT}=1.8V

ADh.3 **SPREAD:** Touch Key spread spectrum
0: Disable
1: Enable

ADh.2 **MCHS:** Touch Key scan channel select
0: select ATK Scan channel
1: select Bundle Scan channel

ADh.1~0 **ATKMODE:** Touch Key scan mode
00: TK scan method, each channel scan 1 time, max 23 TK channels + TK reference key
01: TK scan method, each channel scan 2 times, max 23 TK channels + TK reference key
10: TK scan method, each channel scan 4 times, max 16 TK channels
11: TK scan method, each channel scan 8 times, max 8 TK channels

Note: *also refer to Chapter 6 for more information about Touch Key Interrupt enable and priority.*

SFR **B4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKTMRL	TKTMRL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

B4h.7~0 **TKTMRL:** Touch Key scan length bit 7~0 adjustment
00: shortest
FF: longest

SFR **B5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKCON2	TKFJMP	JMPVH			TKTMRH			
R/W	R/W	R/W			R/W			
Reset	0	0	0	0	0	0	0	0

B5h.7 **TKFJMP:** Internal Touch Key clock frequency auto adjust option
0: Disable
1: Enable (Available in ATKMODE=1 or 2)

B5h.6~5 **JMPVH:** Touch Key clock frequency MSB 3bit (Coarse tune) select, only available in TKFJMP=0
[JMPVH, JMPVL]=000_000=frequency slowest
[JMPVH, JMPVL]=111_111=frequency fastest

B5h.3~0 **TKTMRH:** Touch Key scan length 11~8 adjustment
0000: shortest
1111: longest

SFR **D7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKCON3	–	–	–	–	–	JMPVL		
R/W	–	–	–	–	–	R/W		
Reset	–	–	–	–	–	0	0	0

D7h.2~0 **JMPVL:** Touch Key clock frequency LSB 3bit (Fine tune) select, only available in TKFJMP=0
[JMPVH, JMPVL]=000_000=frequency slowest
[JMPVH, JMPVL]=111_111=frequency fastest

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W
Reset	0	0	0	0	1	1	–	0

F8h.5 **TKSOC:** Touch Key Start of Conversion
Set 1 to start Touch Key conversion, and S/W need to write 0 to clear this flag.

SFR **C5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKCH0	ATKCH0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

C5h.7 TK7 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C5h.6 TK6 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C5h.5 TK5 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C5h.4 TK4 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C5h.3 TK3 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C5h.2 TK2 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C5h.1 TK1 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C5h.0 TK0 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

SFR **C6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKCH1	ATKCH1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

C6h.7 TK15 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C6h.6 TK14 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C6h.5 TK13 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C6h.4 TK12 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C6h.3 TK11 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C6h.2 TK10 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C6h.1 TK9 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C6h.0 TK8 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

SFR **C7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKCH2	ATKCH2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

C7h.7 TKCAP (TK23) internal reference capacitor channel scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C7h.6 TK22 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C7h.5 TK21 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C7h.4 TK20 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C7h.3 TK19 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

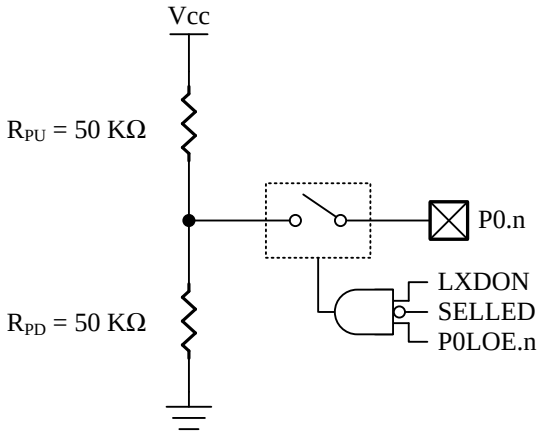
C7h.2 TK18 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C7h.1 TK17 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

C7h.0 TK16 scan enable: 0: disable 1: enable
(if MCHS=0, Select ATK Scan channel; if MCHS=1, Select Bundle Scan channel)

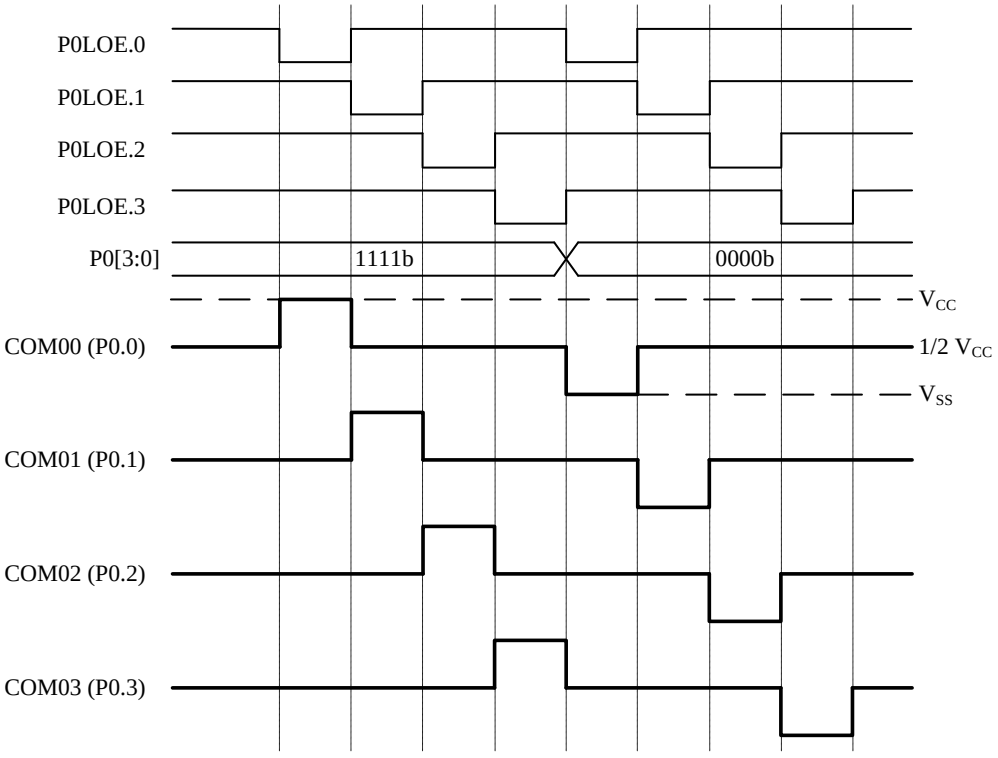
13. S/W Controller LCD Driver

The chip supports an S/W controlled method to driving LCD. All of the IO pins can be the Common pins. User can flexibly adjust the Common pins and Segment pins. It is capable of driving the LCD panel with 169 dots (Max.) by 13 Commons (COM) and 13 Segments (SEG). The P0.0~P0.7 are used for Common pins COM00~COM07. The P1.0~P1.7 are used for Common pins COM10~COM17. The P2.0~P2.1 are used for Common pins COM20~COM21. The P3.0~P3.7 are used for Common pins COM30~COM37. Common pins are capable of driving 1/2 bias by setting the corresponding registers LXDON, SELLED, P0LOE, P1LOE, P2LOE or P3LOE. Refer to the following figures.



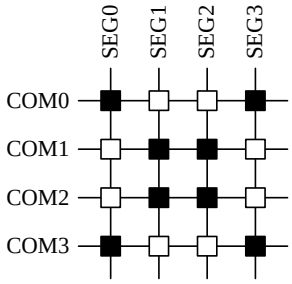
LCD COM00~07 Circuit

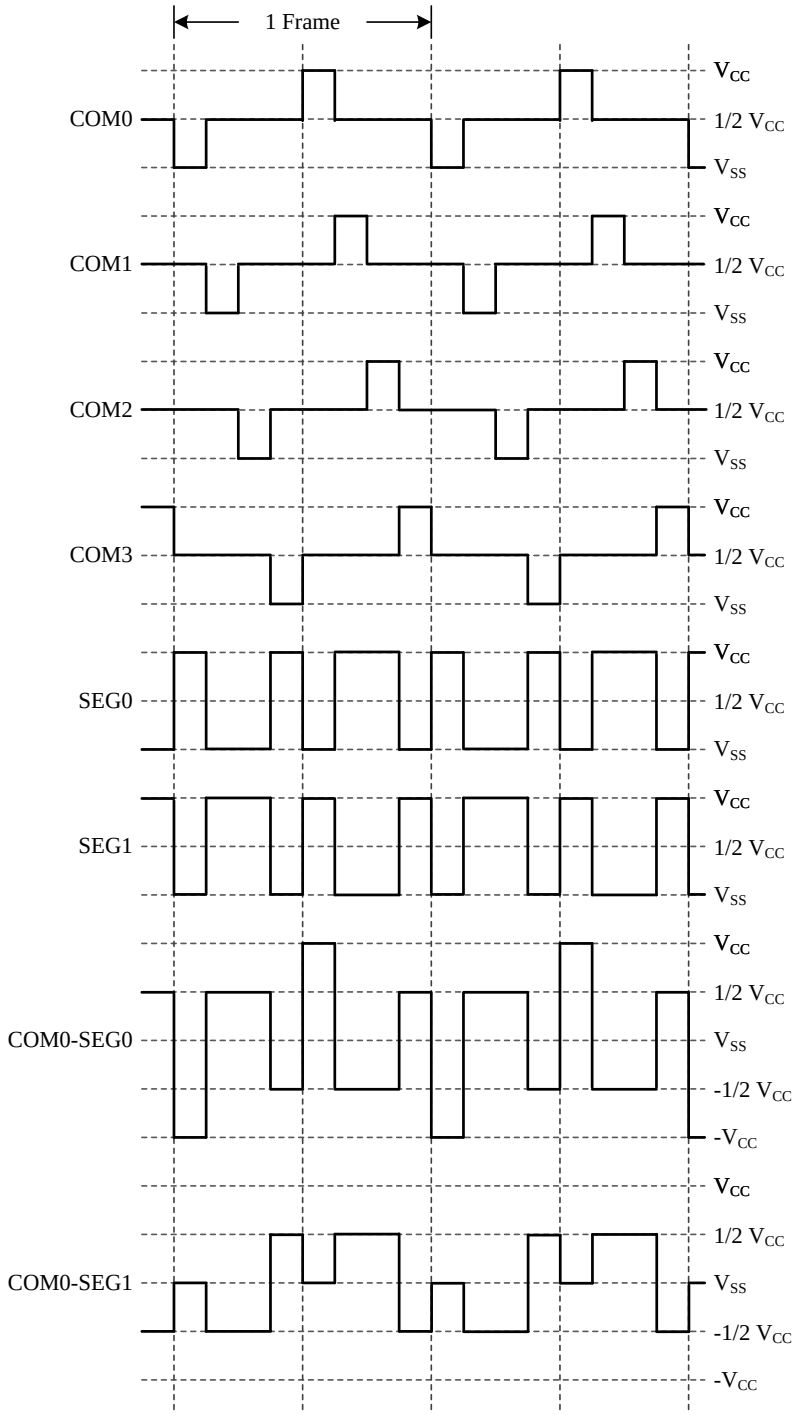
The frequency of any repeating waveform output on the COM pin can be used to represent the LCD frame rate. The figure below shows an LCD frame.



S/W Controlled LCD COM00~03 Scanning

1/4 Duty, 1/2 Bias Output Waveform





SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LXDCON	LXDON	LEDDUTY			LEDBRITM	LEDBRIT		
R/W	R/W	R/W			R/W	R/W		
Reset	0	0	0	0	0	1	1	1

B1h.7 **LXDON:** LCD/LED enable
0: LCD/LED disable
1: LCD/LED enable

SFR **B2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LXDCON2	–	LEDPSC		SELLED	–	–	LEDMODE	
R/W	–	R/W		R/W	–	–	R/W	
Reset	–	0	0	0	–	–	0	0

B2h.4 **SELLED:** LCD/LED function select
0: LCD
1: LED

SFR **86h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0LOE	P0LOE7	P0LOE6	P0LOE5	P0LOE4	P0LOE3	P0LOE2	P0LOE1	P0LOE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

86h.7 **P0LOE7:** LCDC07 / LED SEG6 (P0.7) enable control
0: Disable
1: Enable

86h.6 **P0LOE6:** LCDC06 / LED SEG7 (P0.6) enable control
0: Disable
1: Enable

86h.5 **P0LOE5:** LCDC05 (P0.5) enable control
0: Disable
1: Enable

86h.4 **P0LOE4:** LCDC04 (P0.4) enable control
0: Disable
1: Enable

86h.3 **P0LOE3:** LCDC03 / LED COM3 / LED3 (P0.3) enable control
0: Disable
1: Enable

86h.2 **P0LOE2:** LCDC02 / LED COM2 / LED2 (P0.2) enable control
0: Disable
1: Enable

86h.1 **P0LOE1:** LCDC01 / LED COM1 / LED1 (P0.1) enable control
0: Disable
1: Enable

86h.0 **P0LOE0:** LCDC00 / LED COM0 / LED0 (P0.0) enable control
0: Disable
1: Enable

SFR **ACh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1LOE	P1LOE7	P1LOE6	P1LOE5	P1LOE4	P1LOE3	P1LOE2	P1LOE1	P1LOE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

ACh.7 **P1LOE7:** LCDC17 or LED SEG2 (P1.7) enable control
0: Disable
1: Enable

ACh.6 **P1LOE6:** LCDC16 or LED SEG3 (P1.6) enable control
0: Disable
1: Enable

ACh.5 **P1LOE5:** LCDC15 or LED SEG4 (P1.5) enable control
0: Disable
1: Enable

ACh.4 **P1LOE4:** LCDC14 or LED SEG5 (P1.4) enable control
0: Disable
1: Enable

ACh.3 **P1LOE3:** LCDC13 (P1.3) enable control
0: Disable
1: Enable

ACh.2 **P1LOE2:** LCDC12 (P1.2) enable control
0: Disable
1: Enable

ACh.1 **P1LOE1:** LCDC11 (P1.1) enable control
0: Disable
1: Enable

ACh.0 **P1LOE0:** LCDC10 (P1.0) enable control
0: Disable
1: Enable

SFR **8Eh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2LOE	–	–	–	–	–	–	P2LOE1	P2LOE0
R/W	–	–	–	–	–	–	R/W	R/W
Reset	–	–	–	–	–	–	0	0

8Eh.1 **P2LOE1:** LCDC21 or LED COM5/SEG9 or LED5 (P2.1) enable control
0: Disable
1: Enable

8Eh.0 **P2LOE0:** LCDC20 or LED COM4/SEG8 or LED4 (P2.0) enable control
0: Disable
1: Enable

SFR **B3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3LOE	P3LOE7	P3LOE6	P3LOE5	P3LOE4	P3LOE3	P3LOE2	P3LOE1	P3LOE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B3h.7 **P3LOE7:** LCDC37 or LED COM6/SEG10 or LED6 (P3.7) enable control
0: Disable
1: Enable

B3h.6 **P3LOE6:** LCDC36 or LED SEG1 (P3.6) enable control
0: Disable
1: Enable

B3h.5 **P3LOE5:** LCDC35 or LED SEG0 (P3.5) enable control
0: Disable
1: Enable

B3h.4 **P3LOE4:** LCDC34 or LED COM7/SEG11 or LED7 (P3.4) enable control
0: Disable
1: Enable

B3h.3 **P3LOE3:** LCDC33 (P3.3) enable control
0: Disable
1: Enable

B3h.2 **P3LOE2:** LCDC32 (P3.2) enable control
0: Disable
1: Enable

B3h.1 **P3LOE1:** LCDC31 (P3.1) enable control
0: Disable
1: Enable

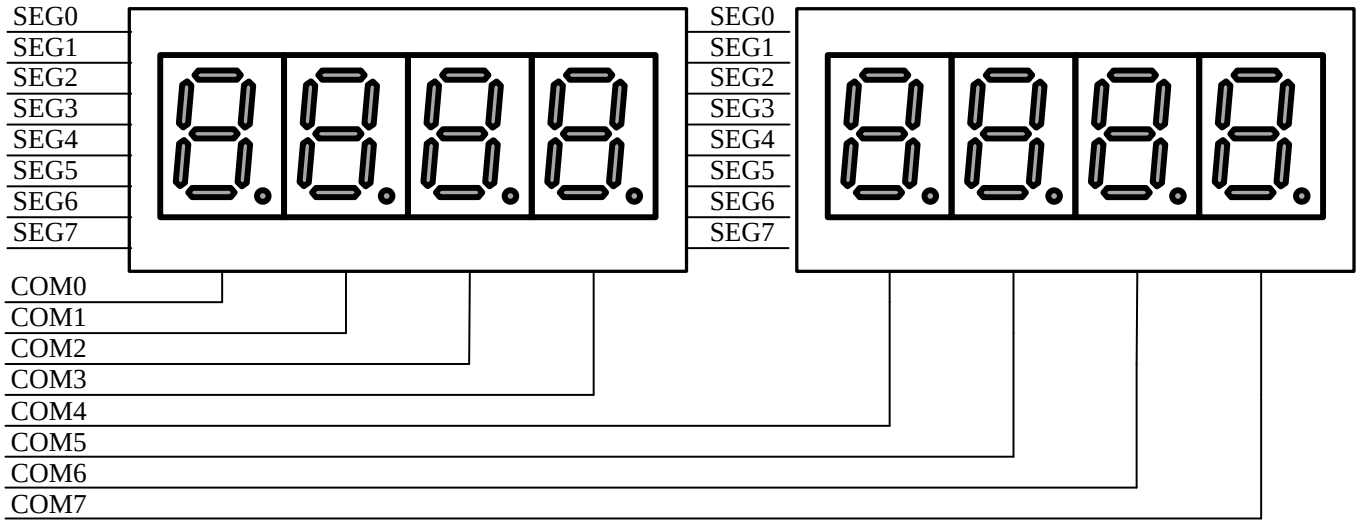
B3h.0 **P3LOE0:** LCDC30 (P3.0) enable control
0: Disable
1: Enable

14. LED Controller/Driver

The module can be configured with two drive modes: LED matrix mode and LED dot matrix mode. By register configuration, it only supports one mode of operation at the same time.

14.1 LED Matrix (MX) Mode

The Chip supports an LED controller and driver at matrix mode. If LEDMODE=00b, LXDON=SELLED=1. The LED matrix mode will enable. It provides 8 Segment pins and 8 Common pins to drive an LED module with 64 pixels or 12 Segment pins and 4 Common pins to drive an LED module with 48 pixels. The COM pins have a high sink current. The brightness of the LED can be set by LEDBRIT. When it is set to 111b, it is the highest brightness. In addition, LEDBRITM is used to set the brightness and uniformity bit. When LEDBRITM=0, better display uniformity can be obtained. When LEDBRITM= 1, better display brightness can be obtained.



The display configuration in XRAM corresponds to the lighting status of the corresponding address. (1 means lighting, 0 means not lighting).

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	COM
C800h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	COM0
C801h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	COM1
C802h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	COM2
C803h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	COM3
C804h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	COM4
C805h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	COM5
C806h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	COM6
C807h	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	COM7
C808h					SEG11	SEG10	SEG9	SEG8	COM0
C809h					SEG11	SEG10	SEG9	SEG8	COM1
C80Ah					SEG11	SEG10	SEG9	SEG8	COM2
C80Bh					SEG11	SEG10	SEG9	SEG8	COM3
C80Ch					SEG11	SEG10	SEG9		COM4
C80Dh					SEG11	SEG10			COM5
C80Eh					SEG11				COM6
C80Fh									COM7

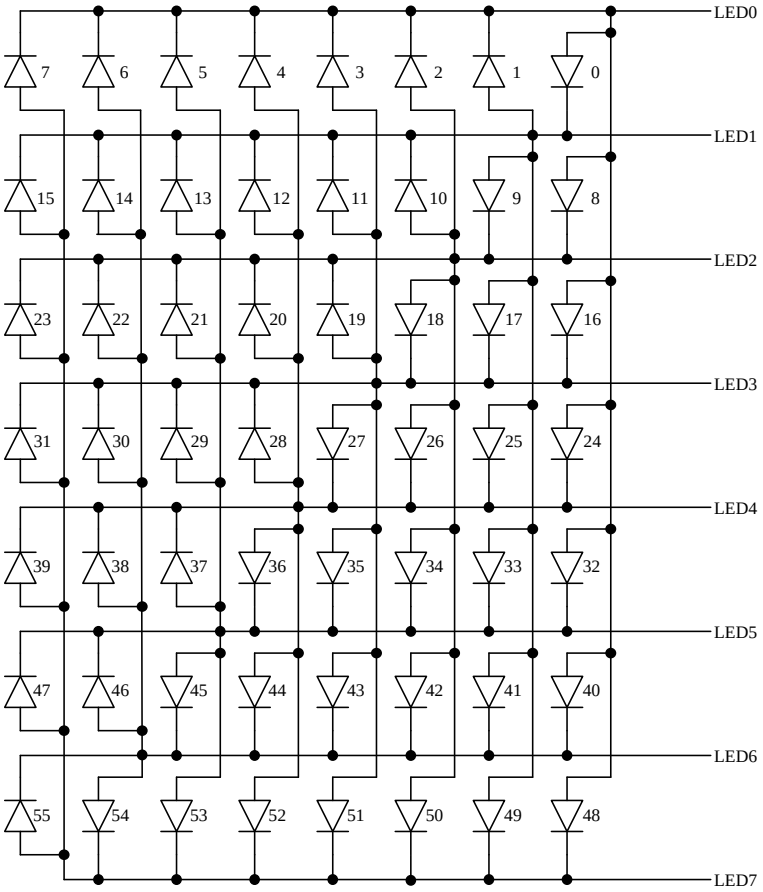
LED matrix drive mode corresponding display configuration table

14.2 LED Dot Matrix (DMX) Mode

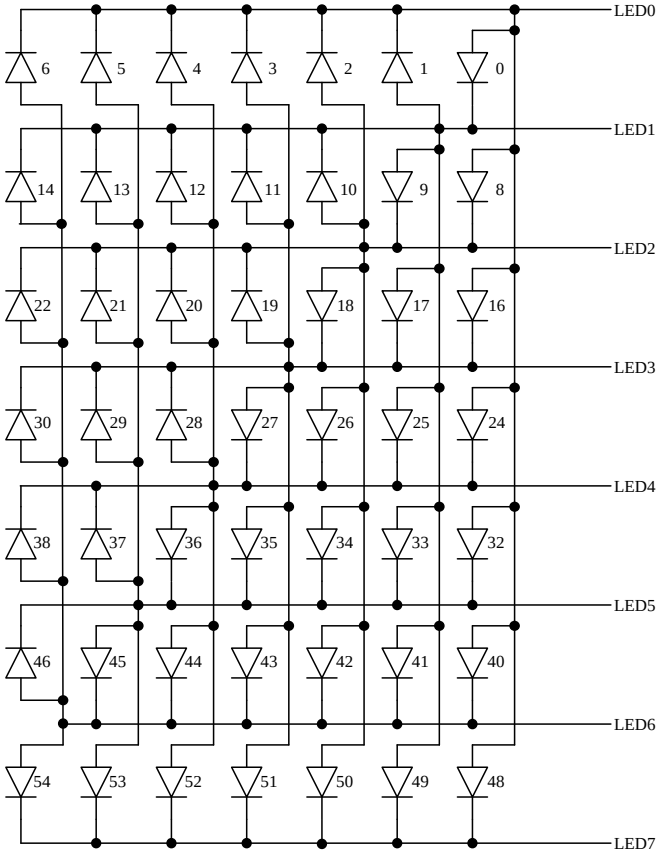
If LEDMODE=10b, LXDON=SELLED=1. The LED dot matrix mode will enable. The LED dot matrix is a universal 7*8 dot matrix. Corresponding to LED0~LED7 ports, up to 7x8=56 LED dots can be configured to drive, the corresponding position of the LED is marked in the 7*8 dot matrix in the figure below Address, the display configuration in XRAM corresponds to the lighting status of the corresponding address (1 means lighting, 0 means not lighting). Support up to 56 lights LED drive. Using LXDDUTY to choose dot matrix 4*4, 5*5, 6*6, 6*7, 7*7 and 7*8, the corresponding LED address remains unchanged. The brightness of the LED can be set by LEDBRIT. When it is set to 111b, it is the highest brightness. In addition, LEDBRITM is used to set the brightness and uniformity bit. When LEDBRITM=0, better display uniformity can be obtained. When LEDBRITM= 1, better display brightness can be obtained.

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C800h	7	6	5	4	3	2	1	0
C801h	15	14	13	12	11	10	9	8
C802h	23	22	21	20	19	18	17	16
C803h	31	30	29	28	27	26	25	24
C804h	39	38	37	36	35	34	33	32
C805h	47	46	45	44	43	42	41	40
C806h	55	54	53	52	51	50	49	48

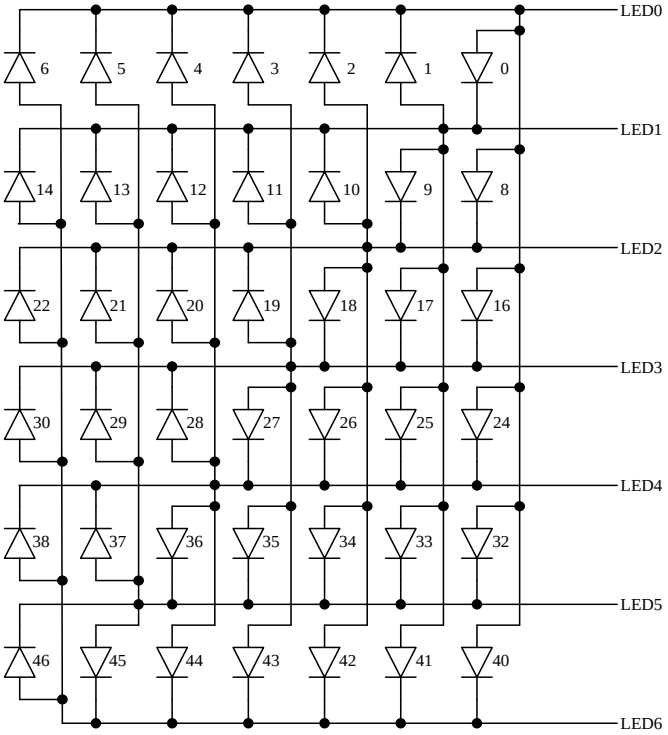
LED dot matrix drive mode corresponding display configuration table



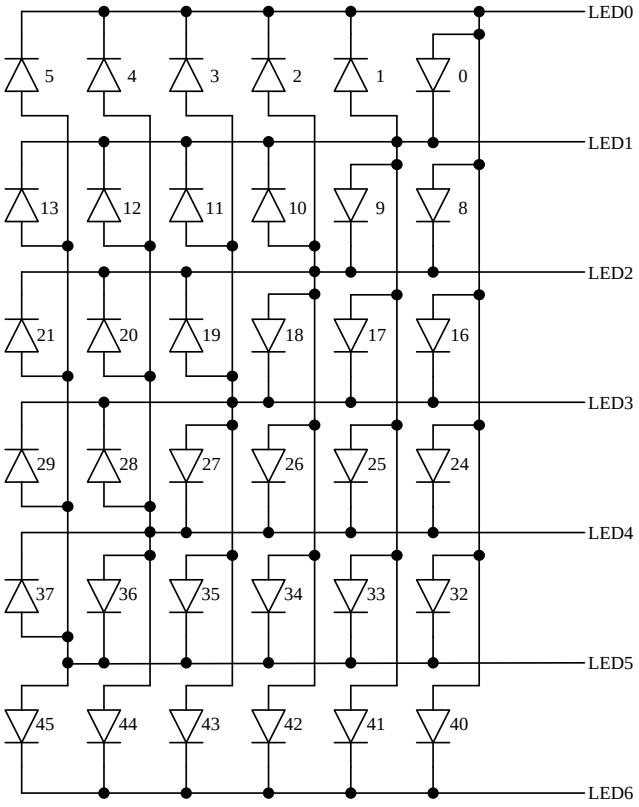
LED 7*8 dot matrix



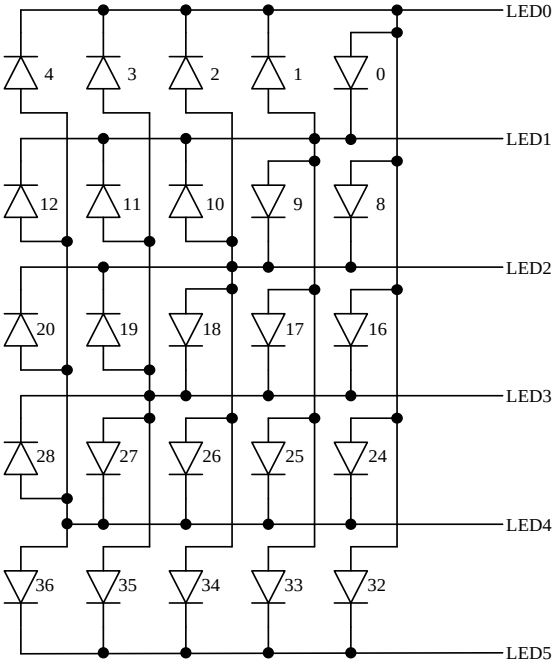
LED 7*7 dot matrix



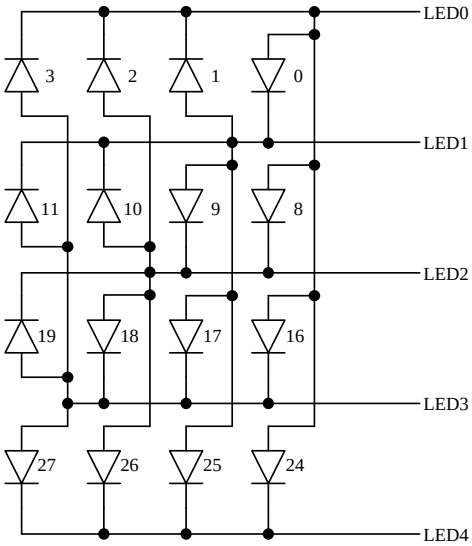
LED 6*7 dot matrix



LED 6*6 dot matrix



LED 5*5 dot matrix



LED 4*4 dot matrix

SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LXDCON	LXDON	LEDDUTY			LEDBRITM	LEDBRIT		
R/W	R/W	R/W			R/W	R/W		
Reset	0	0	0	0	0	1	1	1

B1h.7 **LXDON:** LCD/LED enable
0: LCD/LED disable
1: LCD/LED enable

B1h.6~4 **LEDDUTY:** LED duty select
LED select: Matrix mode (if SELLED=1, LEDMODE=00b)
000: 1/2 Duty, COM 0~1
001: 1/3 Duty, COM 0~2
010: 1/4 Duty, COM 0~3
011: 1/5 Duty, COM 0~4
100: 1/6 Duty, COM 0~5
101: 1/7 Duty, COM 0~6
110: 1/8 Duty, COM 0~7
111: 1/8 Duty, COM 0~7

LED select: Dot Matrix mode (if SELLED=1, LEDMODE=10b)
000: 4x4, LED 0~4
001: 5x5, LED 0~5
010: 6x6, LED 0~6
011: 6x7, LED 0~6
100: 7x7, LED 0~7
101: 7x8, LED 0~7
110: Reserved
111: Reserved

B1h.3 **LEDBRITM:** LED Brightness Mode
0: Uniform brightness mode
1: Brightness enhancement mode

B1h.2~0 **LEDBRIT:** LED Brightness control
000: Level 0 (Darkest)
…
111: Level 7 (Brightest)

SFR **B2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LXDCON2	–	LEDPSC		SELLED	–	–	LEDMODE	
R/W	–	R/W		R/W	–	–	R/W	
Reset	–	0	0	0	–	–	0	0

B2h.6~5 **LEDPSC:** LED clock prescaler select
00: LED clock is FRC divided by 64
01: LED clock is FRC divided by 32
10: LED clock is FRC divided by 16
11: LED clock is FRC divided by 8

B2h.4 **SELLED:** LCD/LED function select
0: LCD
1: LED

B2h.1~0 **LEDMODE:** LED Mode select
00: Matrix scan mode
01: Reserved
10: Dot Matrix scan mode
11: Reserved

SFR **86h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0LOE	P0LOE7	P0LOE6	P0LOE5	P0LOE4	P0LOE3	P0LOE2	P0LOE1	P0LOE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

86h.7 **P0LOE7:** LCDC07 / LED SEG6 (P0.7) enable control
0: Disable
1: Enable

86h.6 **P0LOE6:** LCDC06 / LED SEG7 (P0.6) enable control
0: Disable
1: Enable

86h.5 **P0LOE5:** LCDC05 (P0.5) enable control
0: Disable
1: Enable

86h.4 **P0LOE4:** LCDC04 (P0.4) enable control
0: Disable
1: Enable

86h.3 **P0LOE3:** LCDC03 / LED COM3 / LED3 (P0.3) enable control
0: Disable
1: Enable

86h.2 **P0LOE2:** LCDC02 / LED COM2 / LED2 (P0.2) enable control
0: Disable
1: Enable

86h.1 **P0LOE1:** LCDC01 / LED COM1 / LED1 (P0.1) enable control
0: Disable
1: Enable

86h.0 **P0LOE0:** LCDC00 / LED COM0 / LED0 (P0.0) enable control
0: Disable
1: Enable

SFR **ACh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1LOE	P1LOE7	P1LOE6	P1LOE5	P1LOE4	P1LOE3	P1LOE2	P1LOE1	P1LOE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

ACh.7 **P1LOE7:** LCDC17 or LED SEG2 (P1.7) enable control
0: Disable
1: Enable

ACh.6 **P1LOE6:** LCDC16 or LED SEG3 (P1.6) enable control
0: Disable
1: Enable

ACh.5 **P1LOE5:** LCDC15 or LED SEG4 (P1.5) enable control
0: Disable
1: Enable

ACh.4 **P1LOE4:** LCDC14 or LED SEG5 (P1.4) enable control
0: Disable
1: Enable

ACh.3 **P1LOE3:** LCDC13 (P1.3) enable control
0: Disable
1: Enable

ACh.2 **P1LOE2:** LCDC12 (P1.2) enable control
0: Disable
1: Enable

ACh.1 **P1LOE1:** LCDC11 (P1.1) enable control
0: Disable
1: Enable

ACh.0 **P1LOE0:** LCDC10 (P1.0) enable control
0: Disable
1: Enable

SFR **8Eh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2LOE	–	–	–	–	–	–	P2LOE1	P2LOE0
R/W	–	–	–	–	–	–	R/W	R/W
Reset	–	–	–	–	–	–	0	0

8Eh.1 **P2LOE1:** LCDC21 or LED COM5/SEG9 or LED5 (P2.1) enable control
0: Disable
1: Enable

8Eh.0 **P2LOE0:** LCDC20 or LED COM4/SEG8 or LED4 (P2.0) enable control
0: Disable
1: Enable

SFR **B3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3LOE	P3LOE7	P3LOE6	P3LOE5	P3LOE4	P3LOE3	P3LOE2	P3LOE1	P3LOE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B3h.7 **P3LOE7:** LCDC37 or LED COM6/SEG10 or LED6 (P3.7) enable control
0: Disable
1: Enable

B3h.6 **P3LOE6:** LCDC36 or LED SEG1 (P3.6) enable control
0: Disable
1: Enable

B3h.5 **P3LOE5:** LCDC35 or LED SEG0 (P3.5) enable control
0: Disable
1: Enable

B3h.4 **P3LOE4:** LCDC34 or LED COM7/SEG11 or LED7 (P3.4) enable control
0: Disable
1: Enable

B3h.3 **P3LOE3:** LCDC33 (P3.3) enable control
0: Disable
1: Enable

B3h.2 **P3LOE2:** LCDC32 (P3.2) enable control
0: Disable
1: Enable

B3h.1 **P3LOE1:** LCDC31 (P3.1) enable control
0: Disable
1: Enable

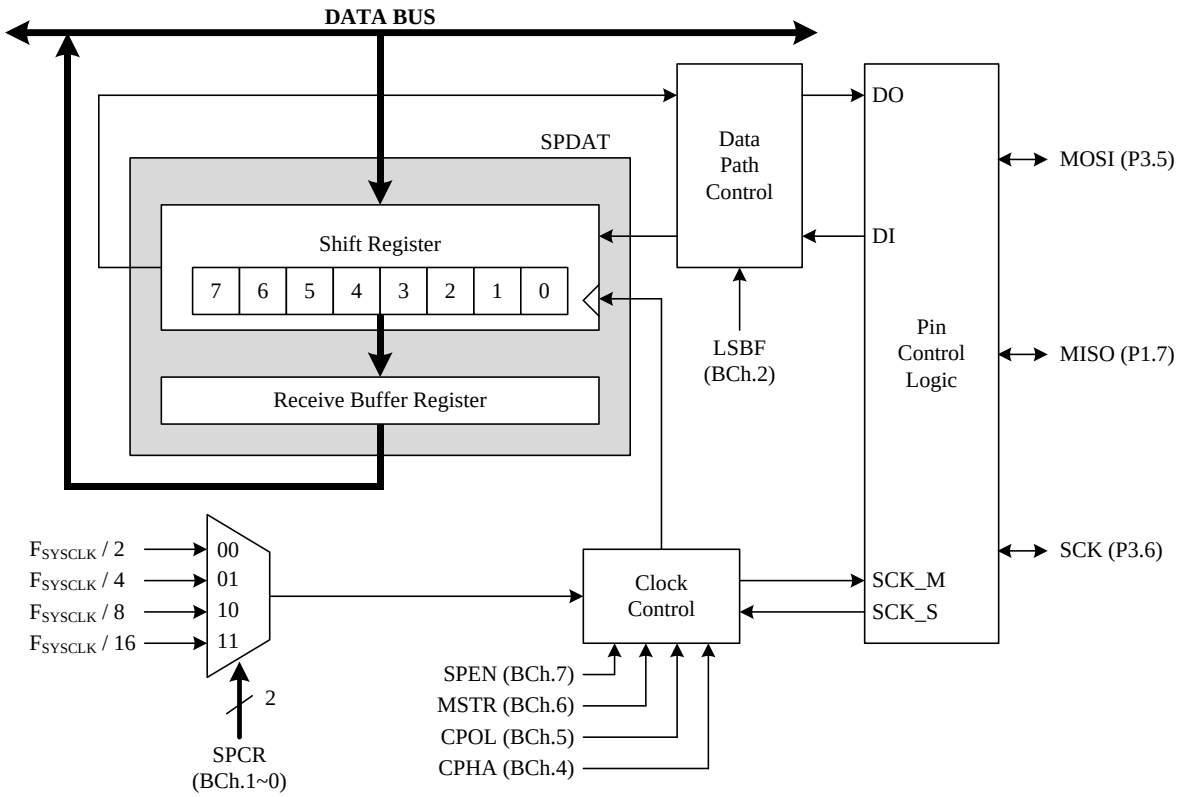
B3h.0 **P3LOE0:** LCDC30 (P3.0) enable control
0: Disable
1: Enable

15. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) module is capable of full-duplex, synchronous, serial communication between the MCU and peripheral devices. The peripheral devices can be other MCUs, A/D converter, sensors, or flash memory, etc. The SPI runs at a clock rate up to the system clock divided by two. Firmware can read the status flags, or the operation can be interrupt driven. Following figure shows the SPI system block diagram.

The features of the SPI module include:

- Master or Slave mode operation
- 3-wire mode operation
- Full-duplex operation
- Programmable transmit bit rate
- Single buffer receive
- Serial clock phase and polarity options
- MSB-first or LSB-first shifting selectable



SPI Function Pin	P1/P3 Mode	P1.n/P3.n SFR data
Master Mode, MISO	**Mode1**	1
Master Mode, SCK, MOSI	**Mode2**	X
Slave Mode, MISO	**Mode2**	X
Slave Mode, SCK, MOSI	**Mode1**	1

Pin Mode Setting for SPI

The three signals used by SPI are described below. The MOSI (P3.5) signal is an output from a Master Device and an input to Slave Devices. The signal is an output when SPI is operating in Master mode and an input when SPI is operating in Slave mode. The MISO (P1.7) signal is an output from a Slave Device and an input to a Master Device. The signal is an input when SPI is operating in Master mode and an output when SPI is operating in Slave mode. Data is transferred most-significant bit (MSB) or least-significant bit (LSB) first by setting the LSBF bit. The SCK (P3.6) signal is an output from a Master Device and an input to Slave Devices. It is used to synchronize the data on the MOSI and MISO lines of Master and Slave. SPI generates the signal with four programmable clock rates in Master mode.

Master Mode

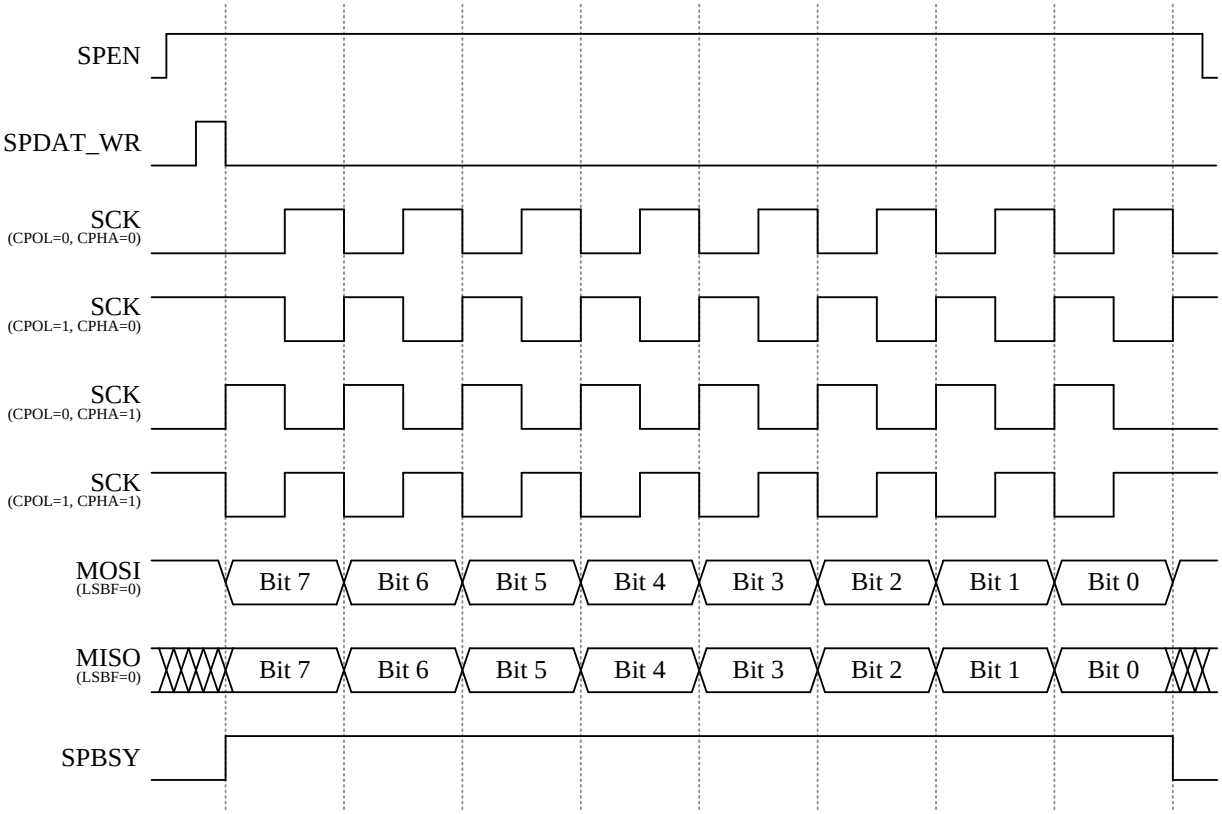
The SPI operates in Master mode by setting the MSTR bit in the SPCON. To start transmit, writing a data to the SPDAT. If SPBSY=0, the data will be transferred to the shift register and starts shift out on the MOSI line. The data of the Slave shift in from the MISO line at the same time. When the SPIF bit becomes set at the end of transfer, the receive data is written to receiver buffer and the RCVBF bit in the SPSTA is set. To prevent an overrun condition, software must read the SPDAT before next byte enters the shift register. The SPBSY bit will be set when writing a data to SPDAT to start transmit, and be cleared at the end of the eighth SCK period in Master mode.

Slave Mode

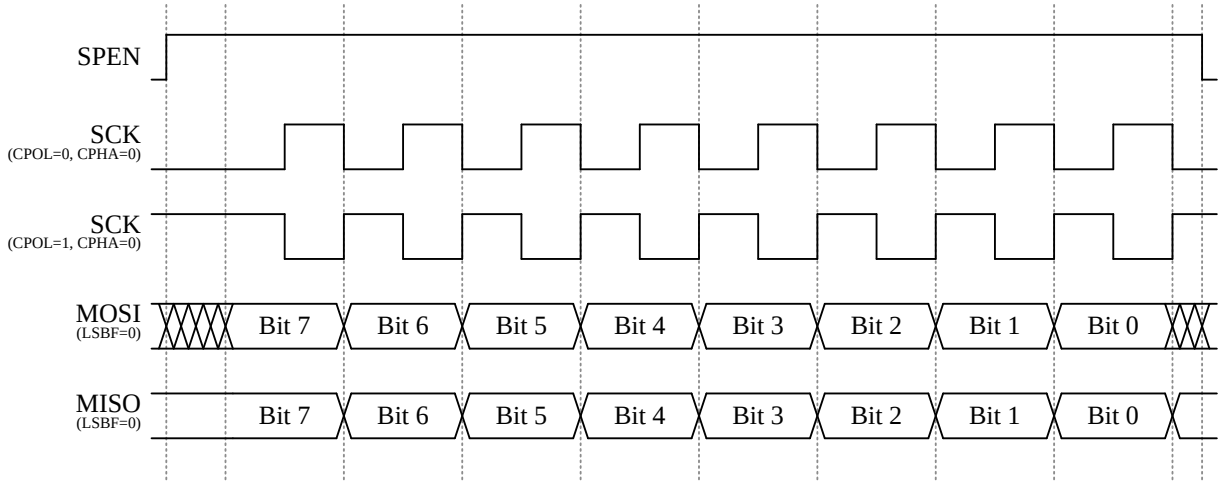
The SPI operates in Slave mode by clearing the MSTR bit in the SPCON. The transmission will start when the SPEN bit in the SPCON is set. The data from a Master will shift into the shift register through the MOSI line, and shift out from the shift register on the MISO line. When a byte enters the shift register, the data will be transferred to receiver buffer if RCVBF=0. If RCVBF=1, the newer received data will not be transferred to receiver buffer and the RCVOVF bit is set. After a byte enters the shift register, the SPIF and RCVBF bits are set. To prevent an overrun condition, software must read the SPDAT or write 0 to RCVBF before next byte enters the shift register. **The maximum SCK frequency allowed in Slave mode is $F_{SYSCLK}/4$.**

Serial Clock

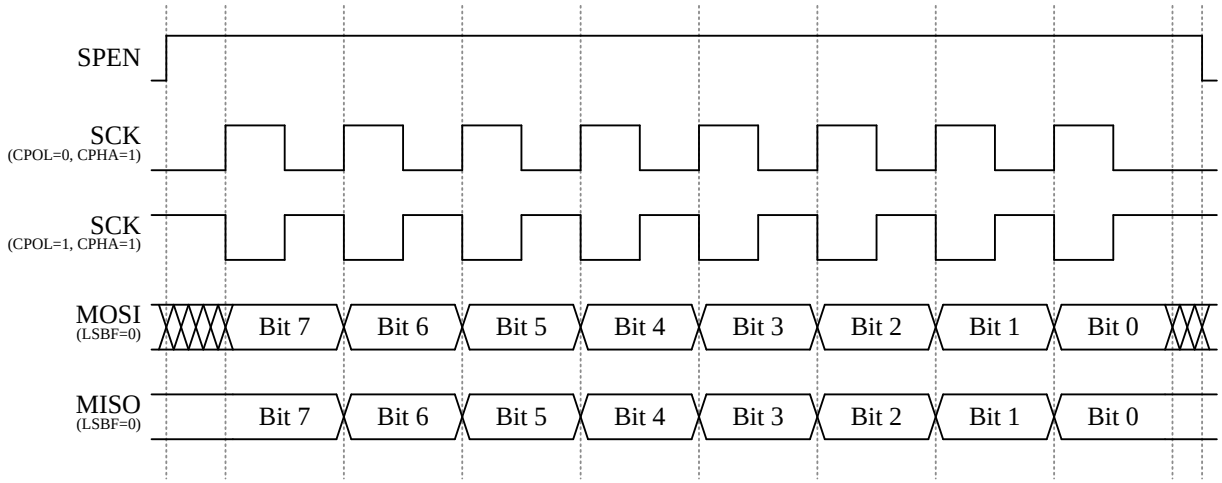
The SPI has four clock types by setting the CPOL and CPHA bits in the SPCON register. The CPOL bit defines the level of the SCK in SPI idle state. The level of the SCK in idle state is low when CPOL=0, and is high when CPOL=1. The CPHA bit defines the edges used to sample and shift data. The SPI sample data on the first edge of SCK period and shift data on the second edge of SCK period when CPHA=0. The SPI sample data on the second edge of SCK period and shift data on first edge of SCK period when CPHA=1. Figures below show the detail timing in Master and Slave modes. Both Master and Slave devices must be configured to use the same clock type before the SPEN bit is set. The SPCR controls the Master mode serial clock frequency. This register is ignored when operating in Slave mode. The SPI clock can select System clock divided by 2, 4, 8, or 16 in Master mode.



Master Mode Timing



Slave Mode Timing (CPHA=0)



Slave Mode Timing (CPHA=1)

In both Master and Slave modes, the SPIF interrupt flag is set by H/W at the end of a data transfer. If write data to SPDAT when SPBSY=1, the WCOL interrupt flag will be set by H/W. When this occurs, the data write to SPDAT will be ignored, and shift register will not be written.

SFR **BCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPCON	SPEN	MSTR	CPOL	CPHA	–	LSBF	SPCR	
R/W	R/W	R/W	R/W	R/W	–	R/W	R/W	
Reset	0	0	0	0	–	0	0	0

BCh.7 **SPEN:** SPI enable
0: SPI disable
1: SPI enable

BCh.6 **MSTR:** Master mode enable
0: Slave mode
1: Master mode

BCh.5 **CPOL:** SPI clock polarity
0: SCK is low in idle state
1: SCK is high in idle state

BCh.4 **CPHA:** SPI clock phase
0: Data sample on first edge of SCK period
1: Data sample on second edge of SCK period

BCh.2 **LSBF:** LSB first
0: MSB first
1: LSB first

BCh.1~0 **SPCR:** SPI clock rate
00: $F_{SYSCLK}/2$
01: $F_{SYSCLK}/4$
10: $F_{SYSCLK}/8$
11: $F_{SYSCLK}/16$

SFR **BDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPSTA	SPIF	WCOL	–	RCVOVF	RCVBF	SPBSY	–	–
R/W	R/W	R/W	–	R/W	R/W	R	–	–
Reset	0	0	–	0	0	0	–	–

BDh.7 **SPIF:** SPI interrupt flag

This is set by H/W at the end of a data transfer. Cleared by H/W when an interrupt is vectored into. Writing 0 to this bit will clear this flag.

BDh.6 **WCOL:** Write collision interrupt flag

Set by H/W if write data to SPDAT when SPBSY is set. Write 0 to this bit or rewrite data to SPDAT when SPBSY is cleared will clear this flag.

BDh.4 **RCVOVF:** Received buffer overrun flag

Set by H/W at the end of a data transfer and RCVBF is set. Write 0 to this bit or read SPDAT register will clear this flag.

BDh.3 **RCVBF:** Receive buffer full flag

Set by H/W at the end of a data transfer. Write 0 to this bit or read SPDAT register will clear this flag.

BDh.2 **SPBSY:** SPI busy flag

Set by H/W when a SPI transfer is in progress.

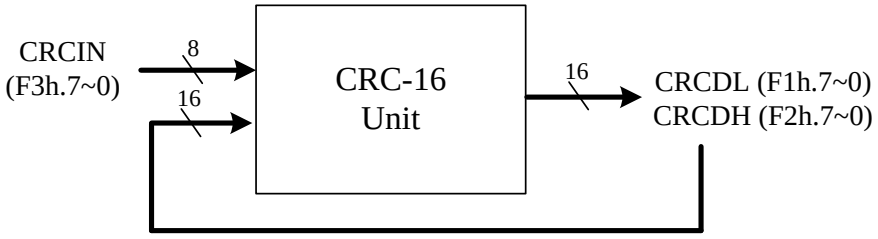
SFR **BEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPDAT	SPDAT							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

BEh.7~0 **SPDAT:** SPI transmit and receive data

The SPDAT register is used to transmit and receive data. Writing data to SPDAT place the data into shift register and start a transfer when in master mode. Reading SPDAT returns the contents of the receive buffer.

16. Cyclic Redundancy Check (CRC)

The chip supports an integrated 16-bit Cyclic Redundancy Check function. The Cyclic Redundancy Check (CRC) calculation unit is an error detection technique test algorithm and uses to verify data transmission or storage data correctness. The CRC calculation takes a 8-bit data stream or a block of data as input and generates a 16-bit output remainder. The data stream is calculated by the same generator polynomial.



CRC Block Diagram

The CRC generator provides the 16-bit CRC result calculation based on the CRC-16-IBM polynomial. In this CRC generator, there are only one polynomial available for the numeric values calculation. It can't support the 16-bit CRC calculations based on any other polynomials. Each write operation to the CRCIN register creates a combination of the previous CRC value stored in the CRCDH and CRCDL registers. It will take one MCU instruction cycle to calculate.

CRC-16-IBM (Modbus) Polynomial representation: $X^{16} + X^{15} + X^2 + 1$

SFR **F1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCDL	CRCDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

F1h.7~0 **CRCDL:** 16-bit CRC checksum data bit 7~0

SFR **F2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCDH	CRCDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

F2h.7~0 **CRCDL:** 16-bit CRC checksum data bit 15~8

SFR **F3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCIN	CRCIN							
W	W							
Reset	–	–	–	–	–	–	–	–

F3h.7~0 **CRCIN:** CRC input data register

17. Multiplier and Divider

The chip provide multiplier and divider have the following functions. The 8 bit operation is fully compatible with industry standard 8051.

- ●8 bits × 8 bits = 16 bit (standard 8051)
- ●8 bits ÷ 8 bits = 8 bits, 8 bits remainder (standard 8051)
- ●16 bits × 16 bits = 32 bit
- ●16 bits ÷ 16 bits = 16 bits, 16 bits remainder
- ●32 bits ÷ 16 bits = 32 bits, 16 bits remainder

No matter 8bit / 16bit / 32bit operation, it's easy to execute by MUL AB and DIV AB instruction. There is extra SFR EXA/EXA2/EXA3/EXB for 16bit / 32bit multiply and divide operation.

For 8 bit multiplier/divider operation, be sure SFR bit muldiv16=0 and div32=0.

For 16 bit multiplier operation, multiplicand, multiplier and product as follows. 16 bit multiplier takes 16 System clock cycles to execute.

Condition	**SFR bit muldiv16=1 and div32=0**			
Multiplication	**Byte3**	**Byte2**	**Byte1**	**Byte0**
Multiplicand	-	-	EXA	A
Multiplier	-	-	EXB	B
Product	EXB	B	A	EXA
OV	Product (EXB or B) !=0		-	-

For 16 bit divider operation, dividend, divisor, quotient, remainder read as follows. 16 bit divider takes 16 System clock cycles to execute.

Condition	**SFR bit muldiv16=1 and div32=0**			
Division	**Byte3**	**Byte2**	**Byte1**	**Byte0**
Dividend	-	-	EXA	A
Divisor	-	-	EXB	B
Quotient	-	-	A	EXA
Remainder	-	-	B	EXB
OV	Divisor EXB = B =0			

For 32 bits ÷ 16 bits operation, dividend, divisor, quotient, remainder read as follows. 32 bit divider takes 32 System clock cycles to execute.

Condition	**SFR bit muldiv16=1 and div32=1**			
Division	**Byte3**	**Byte2**	**Byte1**	**Byte0**
Dividend	EXA3	EXA2	EXA	A
Divisor	-	-	EXB	B
Quotient	A	EXA	EXA2	EXA3
Remainder	-	-	B	EXB
OV	Divisor EXB=B =0			

SFR **CEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA2	EXA2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CEh.7~0 **EXA2:** Expansion accumulator 2

SFR **CFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA3	EXA3							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CFh.7~0 **EXA3:** Expansion accumulator 3

SFR **E6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA	EXA							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E6h.7~0 **EXA:** Expansion accumulator

SFR **E7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXB	EXB							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E7h.7~0 **EXB:** Expansion B register

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.3 **DIV32: (**only active when MULDVI16=1)
0: instruction DIV as 16/16 bit division operation
1: instruction DIV as 32/16 bit division operation

F7h.0 **MULDIV16:**
0: instruction MUL/DIV as 8*8, 8/8 operation
1: instruction MUL/DIV as 16*16, 16/16 or 32/16 operation

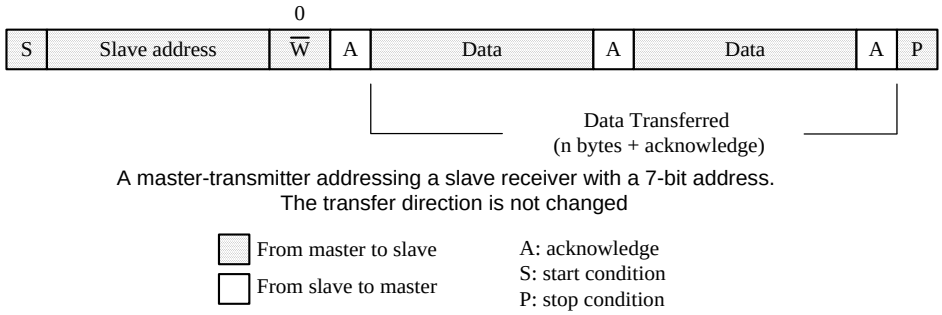
ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MUL AB	Multiply A by B	1	8/16	A4
DIV AB	Divide A by B	1	8/16/32	84

18. Master I²C Interface

Master I²C interface transmit mode:

At the beginning write slave address and direction bit to MIDAT and set MISTART. After the START condition (MISTART), the 7 bits slave address and one bit direction bit are sent. When MIIF convert to 1, address and direction bit transmission was complete. After sending the address and direction bit, user should clear MIIF and write MIDAT to start first data transmission. When MIIF convert to 1, data transfer to slave was complete. User can write MIDAT again to transfer next data to slave. Set MISTOP to finish transmit mode.

MISTART must remain at 1 for the next transfer. After the final data transmit/receive, set MISTOP to finish transmit/receive protocol. MISTART should remain 0 longer than a SCL clock before starting the next Master I²C protocol. SCL clock can be adjusted via MICR.



Master I²C Transmit flow:

(1) Write slave address and direction bit to MIDAT

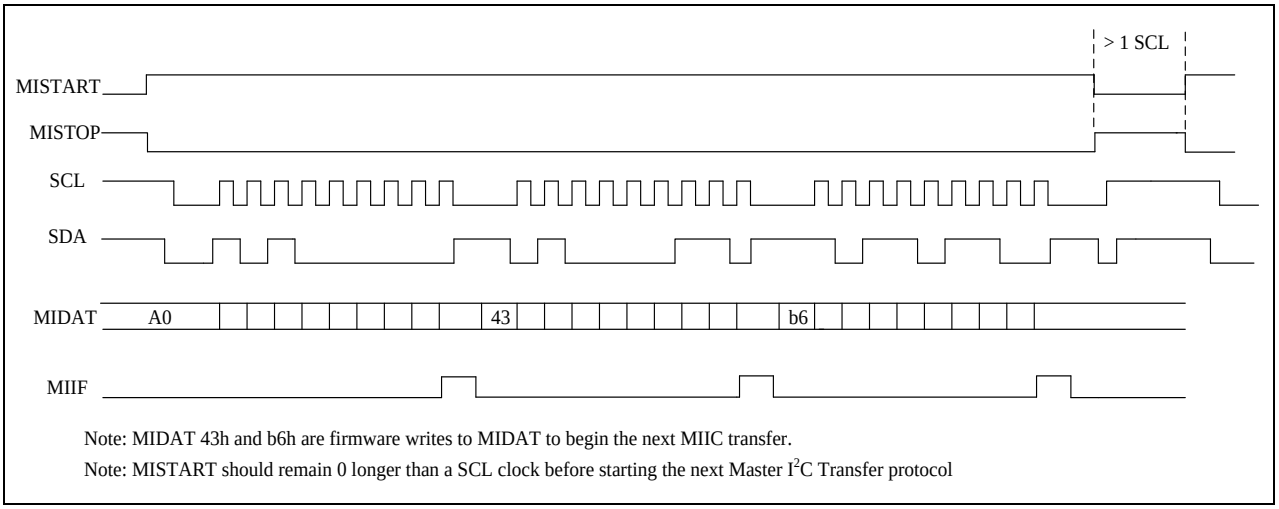
(2) Clear MISTOP and set MISTART to start I²C transmission

(3) Wait until MIIF convert to 1 (interrupt will be issued according to the user's request) and Clear MIIF

(4) Write data to MIDAT to start next transfer (MISTART must remain at 1)

(5) Wait until MIIF convert to 1 (interrupt will be issued according to the user's request) and Clear MIIF, Loop (4) ~ (5) for next transfer.

(6) Clear MISTART and set MISTOP to stop the I²C transfer



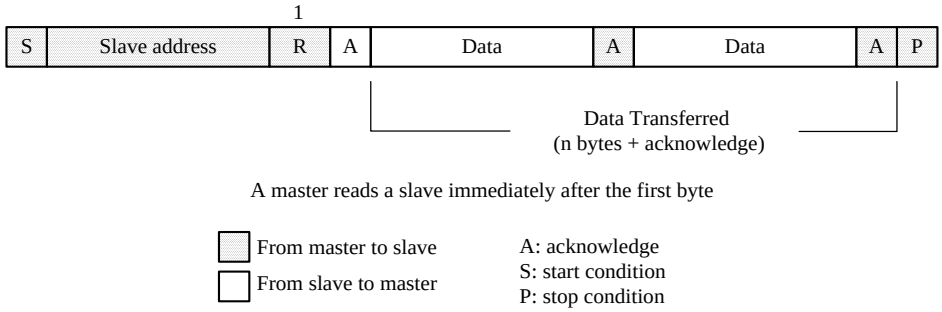
Master Transmit Timing

Note: MISTART should remain 0 longer than a SCL period before starting the next Master I²C protocol.

Master I²C interface Receive mode:

At the beginning write slave address and direction bit to MIDAT and set MISTART. After the START condition (MISTART), the 7 bits slave address and one bit direction bit are sent. When MIIF convert to 1, address and direction bit transmission was complete. After sending the address and direction bit, user should clear MIIF and read MIDAT to start first receive data (The first reading of MIDAT does not represent the data returned by the slave). When MIIF convert to 1, data receive from slave was complete. User can read MIDAT to get data from slave, and start next receive. Set MISTOP to finish receive mode.

MISTART must remain at 1 for the next transfer. After final data transmit/receive, set MISTOP to finish transmit/receive protocol. MISTART should remain 0 longer than a SCL clock before starting the next Master I²C protocol. SCL clock can be adjusted via MICR.



Master I²C Receive flow:

(1) Write slave address and direction bit to MIDAT

(2) Clear MISTOP and set MISTART to start I²C transmission

(3) Wait until MIIF convert to 1 (interrupt will be issued according to the user's request)

(4) Clear MIIF

(5) Read data from MIDAT to start first receive data

(The first reading of MIDAT does not represent the data returned by the slave)

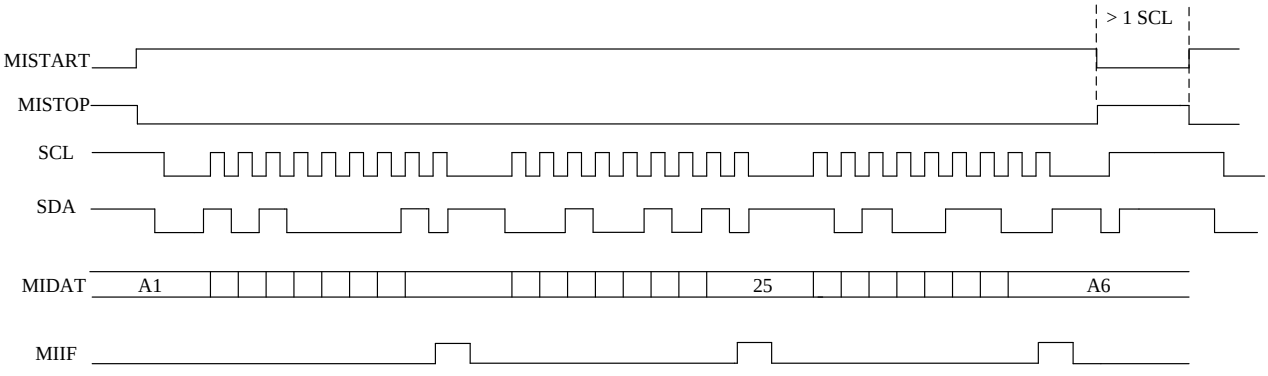
(6) Wait until MIIF convert to 1

(7) Clear MIIF

(8) Read slave data from MIDAT and receive next data

(9) Loop (6) ~(8)

(10) Set MISTOP to stop the I²C transfer



Note: MIDAT 25h and A6h are data from slave

Note: MISTART should remain 0 longer than a SCL clock before starting the next Master I²C Transfer protocol

Master Receive Timing

I²C Function Pin	PINMODxx	Px.n SFR data	Pin State
I²C Master SCL	**Mode0**	X	I²C Clock Output (Open Drain Output, Pull-up)
	Mode2	X	I²C Clock Output (CMOS Push-Pull)
I²C Master SDA	**Mode0**	1	I²C DATA (Pull-up)

Pin Mode Setting for Master I²C

SFR **E1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MICON	MIEN	MIACKO	MIIF	MIACKI	MISTART	MISTOP	MICR	
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	0

E1h.7 **MIEN**: Master I²C enable
- 0: disable
- 1: enable

E1h.6 **MIACKO**: When Master I²C receive data, send acknowledge to I²C Bus
- 0: ACK to slave device
- 1: NACK to slave device

E1h.5 **MIIF**: Master I²C Interrupt flag
- 0: write 0 to clear it
- 1: Master I²C transfer one byte complete

E1h.4 **MIACKI**: When Master I²C transfer, acknowledgement form I²C bus (read only)
- 0: ACK received
- 1: NACK received

E1h.3 **MISTART**: Master I²C Start bit
- 1: start I²C bus transfer

E1h.2 **MISTOP**: Master I²C Stop bit
- 1: send STOP signal to stop I²C bus

E1h.1~0 **MICR:** Master I²C (SCL) clock frequency selection
- 00: $F_{SYSCLK}/4$ (ex. If F_{SYSCLK}=16MHz, I²C clock is 4 MHz)
- 01: $F_{SYSCLK}/16$ (ex. If F_{SYSCLK}=16MHz, I²C clock is 1 MHz)
- 10: $F_{SYSCLK}/64$ (ex. If F_{SYSCLK}=16MHz, I²C clock is 250 KHz)
- 11: $F_{SYSCLK}/256$ (ex. If F_{SYSCLK}=16MHz, I²C clock is 62.5 KHz)

SFR **E2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MIDAT	MIDAT							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E2h.7~0 **MIDAT**: Master I^2C data shift register
(W):After Start and before Stop condition, write this register will resume transmission to I^2C bus
(R): After Start and before Stop condition, read this register will resume receiving from I^2C bus

SFR **C2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SICON	MIIE	TXDIE	RCD2IE	RCD1IE	–	TXDF	RCD2F	RCD1F
R/W	R/W	R/W	R/W	R/W	–	R/W	R/W	R/W
Reset	0	0	0	0	–	1	0	0

C2h.7 **MIIE:** I^2C Master interrupt enable
0: disable
1: enable

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	ES2	LVDIE	SPI2CE	ADTKIE	EX2	PCIE	TM3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

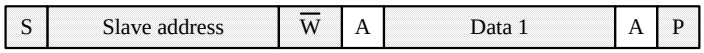
A9h.4 **SPI2CE:** SPI/I²C interrupt enable
0: Disable SPI/I²C interrupt
1: Enable SPI/I²C interrupt

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PSEUDOEN	MSI2CPS	UART2PS	UART1PS	TCOE	T2OE	T1OE	T0OE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A6h.4 **MSI2CPS:** Master/Slave I^2C pin select
0: SCL/SDA = P3.0/P3.1
1: SCL/SDA = P0.1/P0.2

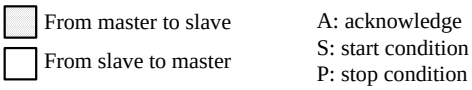
19. Slave I²C Interface

The chip provides Slave I²C interface receive protocol as following. Slave I²C module allow to receive one or two byte data each time after start condition. Before receiving DATA1, be aware that RCD1F must be 0. After DATA1 reception is completed, RCD1F will be converted to 1 and an interrupt will be issued according to the user's request. User can use firmware to clear RCD1F before receiving next DATA1 again. User can write RCD1F to 0 to clear RCD1F. DATA2 and RCD2F operate in the same way as DATA1 and RCD1. After DATA1 or DATA2 reception is completed, the Master side should restart the transfer protocol to transmit the next DATA1 and DATA2.

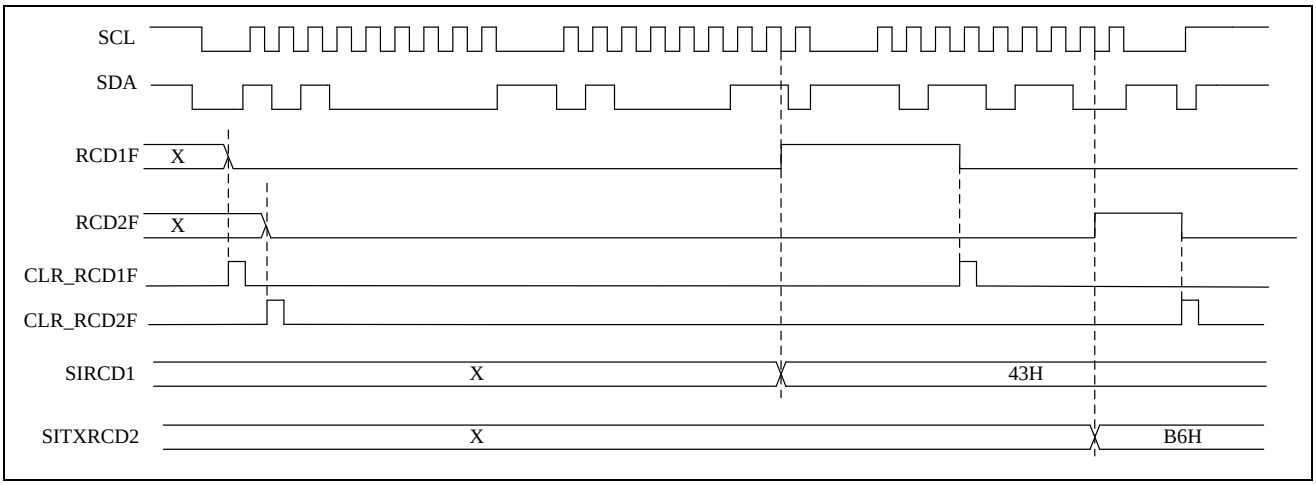


Slave I²C Receive Byte protocol

Slave I²C Receive Two Byte protocol

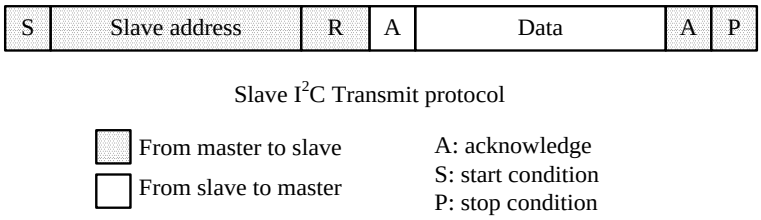


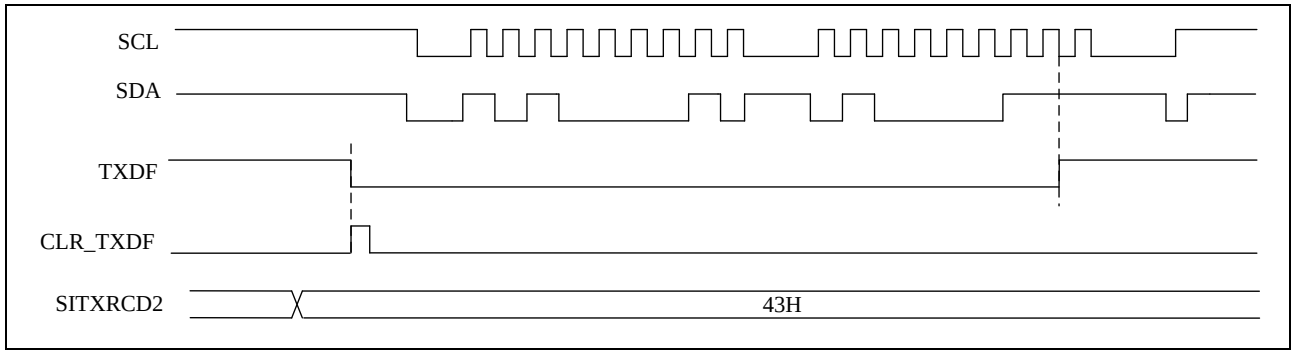
A: acknowledge
S: start condition
P: stop condition



Slave Receive Timing

The chip provides Slave I²C interface transmission protocol as following. Slave I²C module allow to transmit one byte data each time after start condition. Before data transmitting, be aware that TXDF must be 0. After data transmission is completed, TXDF will be converted to 1 and an interrupt will be issued according to the user's request. User can use firmware to clear TXDF before transmitting next data again. User can write TXDF to 0 to clear TXDF. After each transmission is completed, the host should restart the transmission protocol to transmit the next data.





Slave Transmit Timing

I²C Function Pin	PINMODxx	Px.n SFR data	Pin State
I²C Slave SCL	**Mode1**	1	I²C Clock Input (Hi-Z)
I²C Master/Slave SDA	**Mode0**	1	I²C DATA (Pull-up)

Pin Mode Setting for Slave I²C

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PSEUDOEN	MSI2CPS	UART2PS	UART1PS	TCOE	T2OE	T1OE	T0OE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A6h.4 **MSI2CPS:** Master/Slave I²C pin select
0: SCL/SDA = P3.0/P3.1
1: SCL/SDA = P0.1/P0.2

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	ES2	LVDIE	SPI2CE	ADTKIE	EX2	PCIE	TM3IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.4 **SPI2CE:** SPI/I²C interrupt enable
0: Disable SPI/I²C interrupt
1: Enable SPI/I²C interrupt

SFR **C1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIADR	SA							SIEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	0	0	1	0	0

C1h.7~1 **SA:** Slave I²C address assigned

C1h.0 **SIEN:** Slave I²C enable
0: disable
1: enable

SFR **C2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SICON	MIIE	TXDIE	RCD2IE	RCD1IE	–	TXDF	RCD2F	RCD1F
R/W	R/W	R/W	R/W	R/W	–	R/W	R/W	R/W
Reset	0	0	0	0	–	1	0	0

C2h.6 **TXDIE:** Slave I²C transmission completed interrupt enable
0: disable
1: enable

C2h.5 **RCD2IE:** Slave I²C DATA2 (SITXRCD2) reception completed interrupt enable
0: disable
1: enable

C2h.4 **RCD1IE:** Slave I²C DATA1 (SIRCD1) reception completed interrupt enable
0: disable
1: enable

C2h.2 **TXDF:** Slave I²C transmission completed interrupt flag
0: write 0 to clear it
1: Set by H/W when Slave I²C transmission complete

C2h.1 **RCD2F:** Slave I²C DATA2 (SITXRCD2) reception completed interrupt flag
0: write 0 to clear it
1: Set by H/W when Slave I²C DATA2 (SITXRCD2) reception complete

C2h.0 **RCD1F:** Slave I²C DATA1 (SIRCD1) reception completed interrupt flag
0: write 0 to clear it
1: Set by H/W when Slave I²C DATA1 (SIRCD1) reception complete

SFR **C3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIRCD1	SIRCD1							
R/W	R	R	R	R	R	R	R	R
Reset	–	–	–	–	–	–	–	–

C3h.7~0 **SIRCD1:** Slave I²C data receive register1 (DATA1)

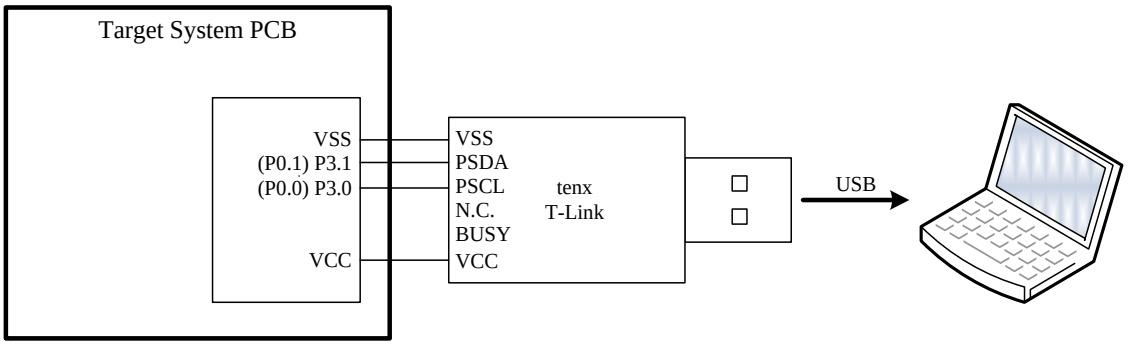
SFR **C4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SITXRCD2	SITXRCD2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	–	–	–	–	–

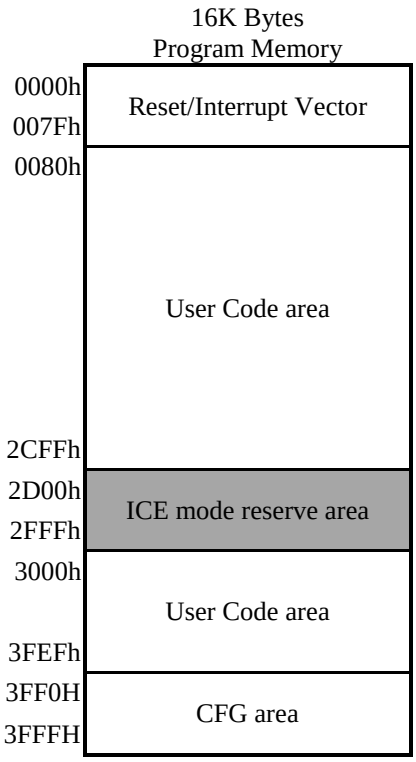
C4h.7~0 **SITXRCD2:** Slave I²C transmit and receive data register
(R): Slave I²C data receive register2 (DATA2)
(W): Slave I²C data transmission register (TXD)

20. In Circuit Emulation (ICE) Mode

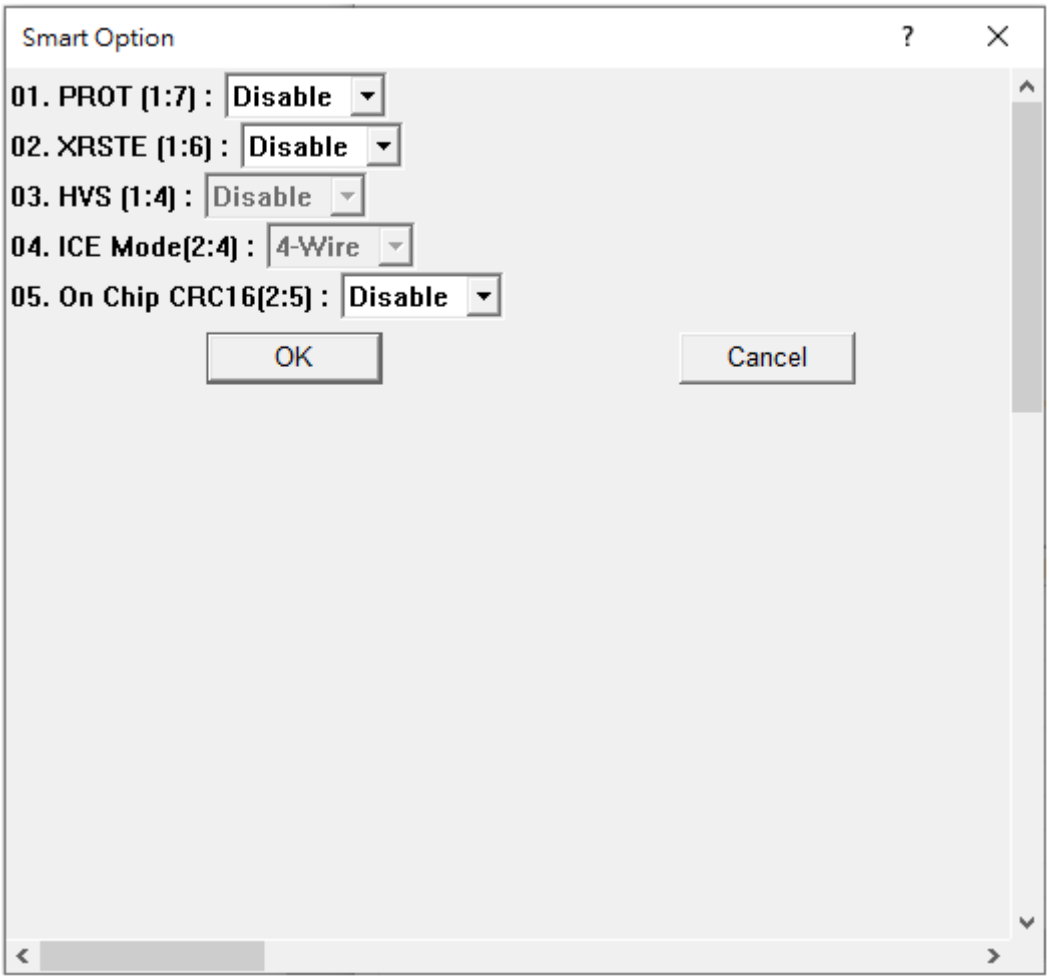
This device can support the In Circuit Emulation Mode. To use the ICE Mode, user just needs to connect P3.0 and P3.1 pin to the tenx proprietary EV Module. The benefit is that user can emulate the whole system without changing the on board target device. But there are some limits for the ICE mode as below.

1. The device must be un-protect.
2. The device's P3.0 and P3.1 pins must work in input Mode (P3MOD0 = 0/1 and P3MOD1=0/1).
3. The Program Memory's addressing space 2D00h~2FFFh and 0033h~003Ah are occupied by tenx EV module. So user Program cannot access these spaces.
4. The T-Link communication pin's function cannot be emulated.
5. The P3.0 and P3.1 pin's can be replaced by P0.0 and P0.1. (Only emulation can be replaced, mass production writer only supports P3.0/P3.1)
6. The VDD level is controlled by T-Link module.





ICE tool settings introduction



No.	Item	Description
01	PROT	**Enable:** Flash code is protect, Writer cannot access the ROM code **Disable:** Flash code is not protect, Writer can access the ROM code (default)
02	XRSTE	**Enable:** P3.7 is external reset pin **Disable:** P3.7 is normal I/O pin (default)
03	HVS	Reserved
04	ICE Mode	Reserved
05	On Chip CRC16	**Enable:** On chip CRC-16 function enable **Disable:** On chip CRC-16 function disable (default)

SFR & CFGW MAP

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h	1111-1111	**P0**	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
81h	0000-0111	**SP**	SP							
82h	0000-0000	**DPL**	DPL							
83h	0000-0000	**DPH**	DPH							
84h	x00x-xxxx	**INTE2**	–	PWM1IE	PWM0IE	–	–	–	–	–
85h	x00x-xxxx	**INTFLG2**	–	PWM1IF	PWM0IF	–	–	–	–	–
86h	0000-0000	**P0LOE0**	P0LOE7	P0LOE6	P0LOE5	P0LOE4	P0LOE3	P0LOE2	P0LOE1	P0LOE0
87h	0xxx-0000	**PCON**	SMOD	–	–	–	GF1	GF0	PD	IDL
88h	0000-0000	**TCON**	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89h	0000-0000	**TMOD**	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
8Ah	0000-0000	**TL0**	TL0							
8Bh	0000-0000	**TL1**	TL1							
8Ch	0000-0000	**TH0**	TH0							
8Dh	0000-0000	**TH1**	TH1							
8Eh	xxxx-xx00	**P2LOE**	–	–	–	–	–	–	P2LOE1	P2LOE0
8Fh	x000-0000	**UART2CON**	–	UART2BRP						
90h	1111-1111	**P1**	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
91h	0101-0101	**P0MODL**	P0MOD3		P0MOD2		P0MOD1		P0MOD0	
92h	0101-0101	**P0MODH**	P0MOD7		P0MOD6		P0MOD5		P0MOD4	
93h	xxxx-0101	**P2MODL**	–	–	–	–	P2MOD1		P2MOD0	
94h	0000-0000	**OPTION**	TKBUFS	TM3CKS	WDTPSC		ADCKS		TKOFC	
95h	0x00-x000	**INTFLG**	LVDIF	–	TKIF	ADIF	–	IE2	PCIF	TF3
96h	0000-0000	**P1WKUP**	P1WKUP							
97h	xxxx-xx00	**SWCMD**	SWRST / IAPALL / WDTO							
98h	0000-0000	**SCON**	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99h	xxxx-xxxx	**SBUF**	SBUF							
9Ah	0000-0000	**SCON2**	SM	–	–	REN2	TB82	RB82	TI2	RI2
9Bh	xxxx-xxxx	**SBUF2**	SBUF2							
9Ch	0000-0000	**P0WKUP**	P0WKUP							
9Dh	xxxx-xx00	**P2WKUP**	–	–	–	–	–	–	P2WKUP	
9Eh	0000-0000	**P3WKUP**	P3WKUP							
A0h	1111-1111	**P2**	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
A1h	0000-0000	**PWMCON**	PWM1CKS		PWM1EN	PWM0EN	PWM0CKS		PWM0NMSK	PWM0PMSK
A2h	0101-0101	**P1MODL**	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
A3h	0101-0101	**P1MODH**	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
A4h	0101-0101	**P3MODL**	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
A5h	0101-0101	**P3MODH**	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
A6h	0000-0000	**PINMOD**	PSEUDOEN	MSI2CPS	UART2PS	UART1PS	TCOE	T2OE	T1OE	T0OE
A7h	xxx1-1111	**TKCHS**	–	–	–	TKCHS				
A8h	0x00-0000	**IE**	EA	–	ET2	ES	ET1	EX1	ET0	EX0
A9h	0000-0000	**INTE1**	PWMIE	ES2	LVDIE	SPI2CIE	ADTKIE	EX2	PCIE	TM3IE
AAh	xxxx-xxxx	**ADCDL**	ADCDL				–	–	–	PWRDEC
ABh	xxxx-xxxx	**ADCDH**	ADCDH							
ACh	0000-0000	**P1LOE**	P1LOE7	P1LOE6	P1LOE5	P1LOE4	P1LOE3	P1LOE2	P1LOE1	P1LOE0
ADh	1101-0000	**TKCON**	TKPD	TKEOC	TMRADJ	TKIVCS	SPREAD	MCHS	ATKMODE	
AEh	1110-0000	**ADCHSEL**	ADCHS					ADCVREFS	VBGSEL	
AFh	0000-0000	**PWMCON2**	PWM0MOD	PWM0MSKE	PWM0OM		PWM0DZ			
B0h	1111-1111	**P3**	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B1h	0000-0111	**LXDCON**	LXDON	LEDDUTY			LEDBRITM	LEDBRIT		
B2h	x000-xx00	**LXDCON2**	–	LEDPSC		SELLED	–	–	LEDMODE	
B3h	0000-0000	**P3LOE**	P3LOE7	P3LOE6	P3LOE5	P3LOE4	P3LOE3	P3LOE2	P3LOE1	P3LOE0
B4h	1111-1111	**TKTMRL**	TKTMRL							
B5h	0000-0000	**TKCON2**	TKFJMP	JMPVH			TKTMRH			
B6h	0000-0000	**PWMOE0**	PWM2OE1	PWM2OE0	PWM1OE1	PWM1OE0	PWM0NOE1	PWM0POE1	PWM0NOE0	PWM0POE0
B7h	0000-0000	**PWMOE1**	PWM6OE1	PWM6OE0	PWM5OE1	PWM5OE0	PWM4OE1	PWM4OE0	PWM3OE1	PWM3OE0
B8h	xx00-0000	**IP**	–	–	PT2	PS	PT1	PX1	PT0	PX0
B9h	xx00-0000	**IPH**	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
BAh	0000-0000	**IP1**	PPWM	PS2	PLVD	PSPI2C	PADTKI	PX2	PPC	PT3
BBh	0000-0000	**IP1H**	PPWMH	PS2H	PLVDH	PSPI2CH	PADTKIH	PX2H	PPCH	PT3H
BCh	0000-x000	**SPCON**	SPEN	MSTR	CPOL	CPHA	–	LSBF	SPCR	
BDh	00x0-00xx	**SPSTA**	SPIF	WCOL	–	RCVOVF	RCVBF	SPBSY	–	–
BEh	0000-0000	**SPDAT**	SPDAT							
C1h	0000-0000	**SIADR**	SA							SIEN
C2h	0000-x000	**SICON**	MIIE	TXDIE	RCD2IE	RCD1IE	–	TXDF	RCD2F	RCD1F
C3h	xxxx-xxxx	**SIRCD1**	SIRCD1							
C4h	xxxx-xxxx	**SITXRCD2**	SITXRCD2							
C5h	0000-0000	**ATKCH0**	ATKCH0							
C6h	0000-0000	**ATKCH1**	ATKCH1							
C7h	0000-0000	**ATKCH2**	ATKCH2							
C8h	0000-0000	**T2CON**	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
C9h	0000-xxxx	**IAPCON**	IAPCON / IAPWE / EEPWE / INFOWE / IAPTO							
CAh	0000-0000	**RCP2L**	RCP2L							
CBh	0000-0000	**RCP2H**	RCP2H							
CCh	0000-0000	**TL2**	TL2							
CDh	0000-0000	**TH2**	TH2							
CEh	0000-0000	**EXA2**	EXA2							
CFh	0000-0000	**EXA3**	EXA3							
D0h	0000-0000	**PSW**	CY	AC	F0	RS1	RS0	OV	F1	P
D1h	0000-0000	**PWM0DH**	PWM0DH							
D2h	0000-0000	**PWM0DL**	PWM0DL							
D3h	0000-0000	**PWM1DH**	PWM1DH							
D4h	0000-0000	**PWM1DL**	PWM1DL							
D5h	0000-0000	**PWM2DH**	PWM2DH							
D6h	0000-0000	**PWM2DL**	PWM2DL							
D7h	xxxx-x000	**TKCON3**	–	–	–	–	–	JMPVL		
D8h	0010-0011	**CLKCON**	SCKTYPE	FCKTYPE	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
D9h	1111-1111	**PWM0PRDH**	PWM0PRDH							
DAh	1111-1111	**PWM0PRDL**	PWM0PRDL							
DBh	1111-1111	**PWM1PRDH**	PWM1PRDH							
DCh	1111-1111	**PWM1PRDL**	PWM1PRDL							
DDh	0000-0000	**PWM3DH**	PWM3DH							
DEh	0000-0000	**PWM3DL**	PWM3DL							
DFh	0000-0000	**UART1CON**	UART1BRS	UART1BRP						
E0h	0000-0000	**ACC**	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
E1h	000x-0100	**MICON**	MIEN	MIACKO	MIIF	MIACKI	MISTART	MISTOP	MICR	
E2h	0000-0000	**MIDAT**	MIDAT							
E3h	xx00-0000	**LVRCON**	–	–	PORPD	LVRPD	LVRSEL			

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E4h	0000-0000	**LVDCON**	LVDM	LVDO	LVDHYS	LVDPD	LVDSEL			
E5h	0000-0000	**EFTCON**	EFT2CS	EFT1CS	EFT1S		EFTSLOW	–	EFTWOUT	CKHLDE
E6h	0000-0000	**EXA**	EXA							
E7h	0000-0000	**EXB**	EXB							
E9h	0000-0000	**PWM4DH**	PWM4DH							
EAh	0000-0000	**PWM4DL**	PWM4DL							
EBh	0000-0000	**PWM5DH**	PWM5DH							
ECh	0000-0000	**PWM5DL**	PWM5DL							
EDh	0000-0000	**PWM6DH**	PWM6DH							
EEh	0000-0000	**PWM6DL**	PWM6DL							
EFh	x000-0x00	**AUX3**	–	HSNK2EN	HSNK1EN	HSNK0EN	WARMTIME	–	FJMPE	FJMPS
F0h	0000-0000	**B**	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
F1h	1111-1111	**CRCDL**	CRCDL							
F2h	1111-1111	**CRCDH**	CRCDH							
F3h	0000-0000	**CRCIN**	CRCIN							
F5h	xxxx-xxxx	**CFGBG**	–	–	–	BGTRIM				
F6h	xxxx-xxxx	**CFGWL**	–	FRCF						
F7h	0000-0110	**AUX2**	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
F8h	0000-11x0	**AUX1**	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL

Flash Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FFBh	**CFGBG**	–	–	–	BGTRIM				
3FFDh	**CFGWL**	–	FRCF						
3FFFh	**CFGWH**	PROT	XRSTE	PORSEL	HVS	–	–	–	–

SFR & CFGW DESCRIPTION

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
80h	**P0**	7~0	P0	R/W	FFh	Port0 data
81h	**SP**	7~0	SP	R/W	07h	Stack Point
82h	**DPL**	7~0	DPL	R/W	00h	Data Point low byte
83h	**DPH**	7~0	DPH	R/W	00h	Data Point high byte
84h	**INTE2**	6	PWM1IE	R/W	0	PWM1~PWM6 interrupt enable 0: Disable PWM1~PWM6 interrupt 1: Enable PWM1~PWM6 interrupt
		5	PWM0IE	R/W	0	PWM0 interrupt enable 0: Disable PWM0 interrupt 1: Enable PWM0 interrupt
85h	**INTFLG2**	6	PWM1IF	R/W	0	PWM1~PWM6 interrupt flag Set by H/W at the end of PWM1 period, S/W writes BFh to INTFLG2 to clear this flag.
		5	PWM0IF	R/W	0	PWM0 interrupt enable Set by H/W at the end of PWM0 period, S/W writes DFh to INTFLG2 to clear this flag.
86h	**P0LOE**	7	P0LOE7	R/W	0	LCDC07 / LED SEG6 (P0.7) enable control 0: Disable 1: Enable
		6	P0LOE6	R/W	0	LCDC06 / LED SEG7 (P0.6) enable control 0: Disable 1: Enable
		5	P0LOE5	R/W	0	LCDC05 (P0.5) enable control 0: Disable 1: Enable
		4	P0LOE4	R/W	0	LCDC04 (P0.4) enable control 0: Disable 1: Enable
		3	P0LOE3	R/W	0	LCDC03 / LED COM3 / LED3 (P0.3) enable control 0: Disable 1: Enable
		2	P0LOE2	R/W	0	LCDC02 / LED COM2 / LED2 (P0.2) enable control 0: Disable 1: Enable
		1	P0LOE1	R/W	0	LCDC01 / LED COM1 / LED1 (P0.1) enable control 0: Disable 1: Enable
		0	P0LOE0	R/W	0	LCDC00 / LED COM0 / LED0 (P0.0) enable control 0: Disable 1: Enable
87h	**PCON**	7	SMOD	R/W	0	Set 1 to enable UART1 double Baud Rate
		3	GF1	R/W	0	General purpose flag bit
		2	GF0	R/W	0	General purpose flag bit
		1	PD	R/W	0	Power down control bit, set 1 to enter Halt/Stop mode
		0	IDL	R/W	0	Idle control bit, set 1 to enter Idle mode
88h	**TCON**	7	TF1	R/W	0	Timer1 overflow flag Set by H/W when Timer/Counter 1 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		6	TR1	R/W	0	Timer1 run control. 1: timer runs; 0: timer stops
		5	TF0	R/W	0	Timer0 overflow flag Set by H/W when Timer/Counter 0 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		4	TR0	R/W	0	Timer0 run control. 1:timer runs; 0:timer stops
		3	IE1	R/W	0	External Interrupt 1 (INT1 pin) edge flag Set by H/W when an INT1 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		2	IT1	R/W	0	External Interrupt 1 control bit 0: Low level active (level triggered) for INT1 pin 1: Falling edge active (edge triggered) for INT1 pin
		1	IE0	R/W	0	External Interrupt 0 (INT0 pin) edge flag Set by H/W when an INT0 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		0	IT0	R/W	0	External Interrupt 0 control bit 0: Low level active (level triggered) for INT0 pin 1: Falling edge active (edge triggered) for INT0 pin
89h	**TMOD**	7	GATE1	R/W	0	Timer1 gating control bit 0: Timer1 enable when TR1 bit is set 1: Timer1 enable only while the INT1 pin is high and TR1 bit is set
		6	CT1N	R/W	0	Timer1 Counter/Timer select bit 0: Timer mode, Timer1 data increases at 2 System clock cycle rate 1: Counter mode, Timer1 data increases at T1 pin's negative edge
		5~4	TMOD1	R/W	00	Timer1 mode select 00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 11: Timer1 stops
		3	GATE0	R/W	0	Timer0 gating control bit 0: Timer0 enable when TR0 bit is set 1: Timer0 enable only while the INT0 pin is high and TR0 bit is set
		2	CT0N	R/W	0	Timer0 Counter/Timer select bit 0: Timer mode, Timer0 data increases at 2 System clock cycle rate 1: Counter mode, Timer0 data increases at T0 pin's negative edge
		1~0	TMOD0	R/W	00	Timer0 mode select 00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.
8Ah	**TL0**	7~0	TL0	R/W	00h	Timer0 data low byte
8Bh	**TL1**	7~0	TL1	R/W	00h	Timer1 data low byte
8Ch	**TH0**	7~0	TH0	R/W	00h	Timer0 data high byte
8Dh	**TH1**	7~0	TH1	R/W	00h	Timer1 data high byte
8Eh	**P2LOE**	1	P2LOE1	R/W	0	LCDC21 / LED COM5 or SEG9 (P2.1) enable control 0: Disable 1: Enable
		0	P2LOE0	R/W	0	LCDC20 / LED COM4 or SEG8 (P2.0) enable control 0: Disable 1: Enable
8Fh	**UART2CON**	6~0	UART2BRP	R/W	00h	Define UART2 Baud Rate prescaler UART2 Baud Rate = F_{SYSCLK}/32/UART2BRP
90h	**P1**	7~0	P1	R/W	FFh	Port1 data
91h	**P0MODL**	7~6	P0MOD3	R/W	01	P0.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P0.3 is ADC input
		5~4	P0MOD2	R/W	01	P0.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P0.2 is ADC input
		3~2	P0MOD1	R/W	01	P0.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P0.1 is ADC input
		1~0	P0MOD0	R/W	01	P0.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P0.0 is ADC input

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
92h	**P0MODH**	7~6	P0MOD7	R/W	01	P0.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P0.7 is ADC input
		5~4	P0MOD6	R/W	01	P0.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P0.6 is ADC input
		3~2	P0MOD5	R/W	01	P0.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P0.5 is ADC input
		1~0	P0MOD4	R/W	01	P0.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P0.4 is ADC input
93h	**P2MODL**	3~2	P2MOD1	R/W	01	P2.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P2.1 is ADC input
		1~0	P2MOD0	R/W	01	P2.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P2.0 is ADC input
94h	**OPTION**	7	TKBUFS	R/W	0	TKRAM Ping-Pong buffer select 0: HW stored TKDATA to TKRAM's 1st half (E100h~E17Fh) 1: HW stored TKDATA to TKRAM's 2nd half (E180h~E1FFh)
		6	TM3CKS	R/W	0	Timer3 clock source select. 0: Slow clock (SXT/SRC) 1: FRC/512
		5~4	WDTPSC	R/W	00	Watchdog Timer prescaler time select 00: 400ms WDT overflow rate 01: 200ms WDT overflow rate 10: 100ms WDT overflow rate 11: 50ms WDT overflow rate
		3~2	ADCKS	R/W	00	ADC clock rate select 00: F_{SYSCLK}/32 01: F_{SYSCLK}/16 10: F_{SYSCLK}/8 11: F_{SYSCLK}/4
		1~0	TKOFC	R/W	00	Touch Key ICLD capacitor select. 00: the smallest 11: the biggest
95h	**INTFLG**	7	LVDIF	R/W	0	LVD interrupt flag Set by H/W when V_{CC} less than the LVD voltage. S/W writes 7Fh to INTFLG to clear this flag.
		5	TKIF	R/W	0	Touch Key interrupt flag Set by H/W at the end of TK conversion. S/W writes DFh to INTFLG or sets the TKSOC bit to clear this flag.
		4	ADIF	R/W	0	ADC interrupt flag Set by H/W at the end of ADC conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.
		2	IE2	R/W	0	External Interrupt 2 (INT2 pin) edge flag Set by H/W when a falling edge is detected on the INT2 pin, no matter the EX2 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine. S/W can write FBh to INTFLG to clear this bit.
		1	PCIF	R/W	0	Port0~3 pin change Interrupt flag Set by H/W when a Port0~3 pin state change is detected and its interrupt enable bit is set (P0WKUP/P1WKUP/P2WKUP/P3WKUP). PCIE does not affect this flag's setting. It is cleared automatically when the program performs the interrupt service routine. S/W can write FDh to INTFLG to clear this bit.
		0	TF3	R/W	0	Timer3 interrupt flag. Set by H/W when Timer3 counts to FFFFFFh. It is cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
96h	**P1WKUP**	7~0	P1WKUP	R/W	00h	P1.7~P1.0 pin individual Wake-up/Interrupt enable control 0: Disable; 1: Enable.
97h	**SWCMD**	7~0	SWRST	W		Write 56h to generate S/W Reset
		7~0	IAPALL	W		Write 65h to set IAPALL flag. Write other value to clear IAPALL flag.
		1	WDTO	R	0	Watchdog Time-Out flag
		0	IAPALL	R	0	Flag indicates Flash can be written by IAP or not 0: Flash IAP only can write IAP-free area. 1: Flash IAP can write IAP-all area.
98h	**SCON**	7	SM0	R/W	0	UART1 Serial port mode select bit 0, 1 (SM0, SM1) = 00: Mode0: 8 bit shift register, Baud Rate=F_{SYSCLK}/2 01: Mode1: 8 bit UART1, Baud Rate is variable 10: Mode2: 9 bit UART1, Baud Rate=F_{SYSCLK}/32 or /64 11: Mode3: 9 bit UART1, Baud Rate is variable
		6	SM1	R/W	0	
		5	SM2	R/W	0	Serial port mode select bit 2 SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.
		4	REN	R/W	0	Set 1 to enable UART1 Reception
		3	TB8	R/W	0	Transmitter bit 8, ninth bit to transmit in Modes 2 and 3
		2	RB8	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit is Mode 1 if SM2=0
		1	TI	R/W	0	Transmit Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W
		0	RI	R/W	0	Receive Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.
99h	**SBUF**	7~0	SBUF	R/W	–	UART1 transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
9Ah	**SCON2**	7	SM	R/W	0	UART2 Serial port mode select bit 0: Mode1: 8 bit UART2, Baud Rate is variable 1: Mode3: 9 bit UART2, Baud Rate is variable
		4	REN2	R/W	0	UART2 reception enable 0: Disable reception 1: Enable reception
		3	TB82	R/W	0	Transmit Bit 8, the ninth bit to be transmitted in Mode3
		2	RB82	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode3
		1	TI2	R/W	0	Transmit interrupt flag Set by H/W at the beginning of the stop bit in Mode 1 & 3. Must be cleared by S/W.
		0	RI2	R/W	0	Receive interrupt flag Set by H/W at the sampling point of the stop bit in Mode 1 & 3. Must be cleared by S/W.
9Bh	**SBUF2**	7~0	SBUF	R/W	–	UART2 transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
9Ch	**P0WKUP**	7~0	P0WKUP	R/W	00h	P0.7~P0.0 pin individual Wake-up/Interrupt enable control 0: Disable; 1: Enable.
9Dh	**P2WKUP**	5~0	P2WKUP	R/W	00h	P2.1~P2.0 pin individual Wake-up/Interrupt enable control 0: Disable; 1: Enable.
9Eh	**P3WKUP**	7~0	P3WKUP	R/W	00h	P3.7~P3.0 pin individual Wake-up/Interrupt enable control 0: Disable; 1: Enable.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
A0h	**P2**	7~2	P2.7~P2.2	R/W	3Fh	P2.7~P2.2 have no pin out, so these bits are used as general purpose register
		1~0	P2.1~P2.0	R/W	11	P2.1~P2.0 data
A1h	**PWMCON**	7~6	PWM1CKS	R/W	00	PWM1 clock source 00: F_{SYSCLK} 01: F_{SYSCLK} 10: FRC 11: FRCx2 (V_{CC}>2.7V)
		5	PWM1EN	R/W	0	PWM1~6 enable control 0: PWM1~6 Disable 1: PWM1~6 Enable
		4	PWM0EN	R/W	0	PWM0 enable control 0: PWM0 Disable 1: PWM0 Enable
		3~2	PWM0CKS	R/W	00	PWM0 clock source 00: F_{SYSCLK} 01: F_{SYSCLK} 10: FRC 11: FRCx2 (V_{CC}>2.7V)
		1	PWM0NMSK	R/W	0	PWM0N mask data. If CLRPWM0=1 and PMW0MSKE=1, PWM0N will output this mask data.
		0	PWM0PMSK	R/W	0	PWM0P mask data. If CLRPWM0=1 and PMW0MSKE=1, PWM0P will output this mask data.
A2h	**P1MODL**	7~6	P1MOD3	R/W	01	P1.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.3 is ADC input
		5~4	P1MOD2	R/W	01	P1.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.2 is ADC input
		3~2	P1MOD1	R/W	01	P1.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.1 is ADC input
		1~0	P1MOD0	R/W	01	P1.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.0 is ADC input
A3h	**P1MODH**	7~6	P1MOD7	R/W	01	P1.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.7 is ADC input
		5~4	P1MOD6	R/W	01	P1.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.6 is ADC input
		3~2	P1MOD5	R/W	01	P1.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.5 is ADC input
		1~0	P1MOD4	R/W	01	P1.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.4 is ADC input
A4h	**P3MODL**	7~6	P3MOD3	R/W	01	P3.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.3 is ADC input
		5~4	P3MOD2	R/W	01	P3.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.2 is ADC input
		3~2	P3MOD1	R/W	01	P3.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.1 is ADC input
		1~0	P3MOD0	R/W	01	P3.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.0 is ADC input

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
A5h	**P3MODH**	7~6	P3MOD7	R/W	01	P3.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.7 is ADC input
		5~4	P3MOD6	R/W	01	P3.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.6 is ADC input
		3~2	P3MOD5	R/W	01	P3.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.5 is ADC input
		1~0	P3MOD4	R/W	01	P3.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.4 is ADC input
A6h	**PINMOD**	7	PSEUDOEN	R/W	0	P3.2~P3.0 pseudo open-drain control 0: Disable 1: Enable
		6	MSI2CPS	R/W	0	Master/Slave I^2C pin select (SCL/SDA) 0: P3.0/P3.1 1: P0.1/P0.2
		5	UART2PS	R/W	0	UART2 Pin select (TX/RX) 0: P1.7/P3.6 1: P0.3/P0.2
		4	UART1PS	R/W	0	UART1 Pin select (TX/RX) 0: P3.1/P3.0 1: P0.0/P0.1
		3	TCOE	R/W	0	System clock signal output (CKO) control 0: Disable "System clock divided by 2" output to P1.4 pin 1: Enable "System clock divided by 2" output to P1.4 pin
		2	T2OE	R/W	0	Timer2 signal output (T2O) control 0: Disable "Timer2 overflow divided by 2" output to P1.0 pin 1: Enable "Timer2 overflow divided by 2" output to P1.0 pin
		1	T1OE	R/W	0	Timer1 signal output (T1O) control 0: Disable "Timer1 overflow divided by 2" output to P3.5 pin 1: Enable "Timer1 overflow divided by 2" output to P3.5 pin
		0	T0OE	R/W	0	Timer0 signal output (T0O) control 0: Disable "Timer0 overflow divided by 64" output to P3.4 pin 1: Enable "Timer0 overflow divided by 64" output to P3.4 pin
A7h	**TKCHS**	4~0	TKCHS	R/W	1Fh	Touch Key channel select 00000: TK0 (P3.3) 00001: TK1 (P3.2) 00010: TK2 (P3.1) 00011: TK3 (P3.0) 00100: TK4 (P1.0) 00101: TK5 (P1.1) 00110: TK6 (P1.2) 00111: TK7 (P1.3) 01000: TK8 (P1.4) 01001: TK9 (P1.5) 01010: TK10 (P1.6) 01011: TK11 (P1.7) 01100: TK12 (P3.6) 01101: TK13 (P3.5) 01110: TK14 (P3.4) 01111: TK15 (P3.7) 10000: TK16 (P2.0) 10001: TK17 (P2.1) 10010: TK18 (P0.3) 10011: TK19 (P0.7) 10100: TK20 (P0.6) 10101: TK21 (P0.5) 10110: TK22 (P0.4) 10111: TK reference capacitor others: Reserved

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
A8h	**IE**	7	EA	R/W	0	Global interrupt enable control. 0: Disable all Interrupts. 1: Each interrupt is enabled or disabled by its own interrupt control bit.
		5	ET2	R/W	0	Set 1 to enable Timer2 interrupt
		4	ES	R/W	0	Set 1 to enable Serial Port (UART1) Interrupt
		3	ET1	R/W	0	Set 1 to enable Timer1 Interrupt
		2	EX1	R/W	0	Set 1 to enable external INT1 pin Interrupt & Halt/Stop mode wake up capability
		1	ET0	R/W	0	Set 1 to enable Timer0 Interrupt
		0	EX0	R/W	0	Set 1 to enable external INT0 pin Interrupt & Halt/Stop mode wake up capability
A9h	**INTE1**	7	PWMIE	R/W	0	Set 1 to enable PWM0/PWM1~PWM6 interrupt
		6	ES2	R/W	0	Set 1 to enable Serial Port (UART2) Interrupt
		5	LVDIE	R/W	0	Set 1 to enable LVD interrupt
		4	SPI2CE	R/W	0	Set 1 to enable SPI/I^2C interrupt
		3	ADTKIE	R/W	0	Set 1 to enable ADC/TK Interrupt
		2	EX2	R/W	0	Set 1 to enable external INT2 pin Interrupt & Halt/Stop mode wake up capability
		1	PCIE	R/W	0	Set 1 to enable Port0/Port1/Port2/Port3 Pin Change Interrupt
		0	TM3IE	R/W	0	Set 1 to enable Timer3 Interrupt
AAh	**ADCDL**	7~4	ADCDL	R	–	ADC data bit 3~0
		0	PWRDEC	W	0	ROM parameter settings for high temperature writing.
ABh	**ADCDH**	7~0	ADCDH	R	–	ADC data bit 11~4
ACh	**P1LOE**	7	P1LOE7	R/W	0	LCDC17 / LED SEG2 (P1.7) enable control 0: Disable 1: Enable
		6	P1LOE6	R/W	0	LCDC16 / LED SEG3 (P1.6) enable control 0: Disable 1: Enable
		5	P1LOE5	R/W	0	LCDC15 / LED SEG4 (P1.5) enable control 0: Disable 1: Enable
		4	P1LOE4	R/W	0	LCDC14 / LED SEG5 (P1.4) enable control 0: Disable 1: Enable
		3	P1LOE3	R/W	0	LCDC13 (P1.3) enable control 0: Disable 1: Enable
		2	P1LOE2	R/W	0	LCDC12 (P1.2) enable control 0: Disable 1: Enable
		1	P1LOE1	R/W	0	LCDC11 (P1.1) enable control 0: Disable 1: Enable
		0	P1LOE0	R/W	0	LCDC10 (P1.0) enable control 0: Disable 1: Enable
ADh	**TKCON**	7	TKPD	R/W	1	Touch Key power down (Auto disable in Idle/Halt/Stop mode when Touch Key end of conversion) 0: Touch Key enable 1: Touch Key disable
		6	TKEOC	R	1	Touch Key end of conversion flag, TKEOC may have 3 us delay after TKSOC=1, so F/W must wait enough time before polling this Flag. 0: Indicates conversion is in progress 1: Indicates conversion is finished
		5	TMRADJ	R/W	0	Touch Key scan length auto-adjustment selection 0: TK scan length define by TKTMR[11:0] 1: TK scan length auto-adjustment

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		4	TKIVCS	R/W	1	Touch Key internal voltage control select 0: V_{CHG}=2.8V; V_{INT}=1.4V 1: V_{CHG}=3.6V; V_{INT}=1.8V
		3	SPREAD	R/W	0	Touch Key spread spectrum 0: Disable 1: Enable
		2	MCHS	R/W	0	Scan channel select 0: select channel as ATK Scan 1: select channel as Bundle Scan
		1~0	ATKMODE	R/W	00	Touch Key scan mode 00: each channel scan 1 time, max 23 TK channels + TK reference key 01: each channel scan 2 times, max 23 TK channels + TK reference key 10: each channel scan 4 times, max 16 TK channels 11: each channel scan 8 times, max 8 TK channels
AEh	**ADCHSEL**	7~3	ADCHS	R/W	1Ch	ADC channel select. 00000: AD0 (P3.3) 00001: AD1 (P3.2) 00010: AD2 (P3.1) 00011: AD3 (P3.0) 00100: AD4 (P1.0) 00101: AD5 (P1.1) 00110: AD6 (P1.2) 00111: AD7 (P1.3) 01000: AD8 (P1.4) 01001: AD9 (P1.5) 01010: AD10 (P1.6) 01011: AD11 (P1.7) 01100: V_{BG} 01101: V_{SS} 01110: AD14 (P3.6) 01111: AD15 (P3.5) 10000: AD16 (P3.4) 10001: AD17 (P3.7) 10010: AD18 (P2.0) 10011: AD19 (P2.1) 10100: AD20 (P0.3) 10101: AD21 (P0.2) 10110: AD22 (P0.1) 10111: AD23 (P0.0) 11000: AD24 (P0.7) 11001: AD25 (P0.6) 11010: AD26 (P0.5) 11011: AD27 (P0.4) others: Reserved 11111: V_{CC}/4
		2	ADCVREFS	R/W	0	ADC reference voltage 0: V_{CC} 1: V_{BG}
		1~0	VBGSEL	R/W	00	V_{BG} voltage select, When ADCVREF is selected as V_{BG}; VBGSEL is prohibited from using 1.18V. 00: 1.18V 01: 2.5V (need V_{CC}>2.8V) 10: Reserved 11: Reserved

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
AFh	**PWMCON2**	7	PWM0MOD	R/W	0	PWM0 mode select 0: Normal mode 1: Half-bridge mode
		6	PWM0MSKE	R/W	0	PWM0 mask output enable 0: Disable 1: Enable, PWM0P/PWM0N output data by PWM0PMSK/PWM0NMSK while CLRPWM0=1
		5~4	PWM0OM	R/W	00	PWM0 output mode select 00: Mode0 01: Mode1 10: Mode2 11: Mode3
		3~0	PWM0DZ	R/W	0000	PWM0 dead zone (Dead zone is prohibited in half-bridge mode) 0000: 0 x T_{PWMCLK} 0001: 1 x T_{PWMCLK} … 1111: 15 x T_{PWMCLK}
B0h	**P3**	7~0	P3	R/W	FFh	Port3 data
B1h	**LXDCON**	7	LXDON	R/W	0	LCD/LED enable 0: LCD/LED disable 1: LCD/LED enable
		6~4	LEDDUTY	R/W	000	LED duty select LED select: Matrix mode (SELLED=1, LEDMODE=00b) 000: 1/2 Duty, COM0~COM1 001: 1/3 Duty, COM0~COM2 010: 1/4 Duty, COM0~COM3 011: 1/5 Duty, COM0~COM4 100: 1/6 Duty, COM0~COM5 101: 1/7 Duty, COM0~COM6 110: 1/8 Duty, COM0~COM7 111: 1/8 Duty, COM0~COM7 LED select: Dot Matrix mode (SELLED=1, LEDMODE=10b) 000: 4x4, LED0~LED4 001: 5x5, LED0~LED5 010: 6x6, LED0~LED6 011: 6x7, LED0~LED6 100: 7x7, LED0~LED7 101: 7x8, LED0~LED7 110: Reserved 111: Reserved
		3	LEDBRITM	R/W	0	LED Brightness Mode 0: Uniform brightness mode 1: Brightness enhancement mode
		2~0	LEDBRIT	R/W	111	LCD/LED Brightness control 000: Level 0 (Darkest) … 111: Level 7 (Brightest)
B2h	**LXDCON2**	6~5	LEDPSC	R/W	00	LED clock prescaler select 00: LED clock is FRC divided by 64 01: LED clock is FRC divided by 32 10: LED clock is FRC divided by 16 11: LED clock is FRC divided by 8
		4	SELLED	R/W	0	LCD/LED function select 0: LCD 1: LED
		1~0	LEDMODE	R/W	00	LED Mode select 00: Matrix scan mode 01: Reserved 10: Dot Matrix scan mode 11: Reserved

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
B3h	**P3LOE**	7	P3LOE7	R/W	0	LCDC37 / LED COM6 or SEG10 / LED6 (P3.7) enable control 0: Disable 1: Enable
		6	P3LOE6	R/W	0	LCDC36 / LED SEG1 (P3.6) enable control 0: Disable 1: Enable
		5	P3LOE5	R/W	0	LCDC35 / LED SEG0 (P3.5) enable control 0: Disable 1: Enable
		4	P3LOE4	R/W	0	LCDC34 / LED COM7 or SEG11 / LED7 (P3.4) enable control 0: Disable 1: Enable
		3	P3LOE3	R/W	0	LCDC33 (P3.3) enable control 0: Disable 1: Enable
		2	P3LOE2	R/W	0	LCDC32 (P3.2) enable control 0: Disable 1: Enable
		1	P3LOE1	R/W	0	LCDC31 (P3.1) enable control 0: Disable 1: Enable
		0	P3LOE0	R/W	0	LCDC30 (P3.0) enable control 0: Disable 1: Enable
B4h	**TKTMRL**	7~0	TKTMRL	R/W	FFh	Touch Key scan length bit 7~0 adjustment 00: shortest FF: longest
B5h	**TKCON2**	7	TKFJMP	R/W	0	Internal Touch Key clock frequency auto adjust option 0: Disable 1: Enable (Available in ATKMODE=1 or 2)
		6~4	JMPVH	R/W	000	Touch Key clock frequency MSB 3bit (Coarse tune) select, only available in TKFJMP=0 [JMPVH, JMPVL]=000_000=frequency slowest [JMPVH, JMPVL]=111_111=frequency fastest
		3~0	TKTMRH	R/W	0000	Touch Key scan length 11~8 adjustment. 0000: shortest 1111: longest
B6h	**PWMOE0**	7	PWM2OE1	R/W	0	PWM2 output control 0: Disable 1: PWM2 enable and output to P3.3
		6	PWM2OE0	R/W	0	PWM2 output control 0: Disable 1: PWM2 enable and output to P1.5
		5	PWM1OE1	R/W	0	PWM1 output control 0: Disable 1: PWM1 enable and output to P3.2
		4	PWM1OE0	R/W	0	PWM1 output control 0: Disable 1: PWM1 enable and output to P1.4
		3	PWM0NOE1	R/W	0	PWM0N output control 0: Disable 1: PWM0N enable and output to P2.0
		2	PWM0POE1	R/W	0	PWM0P output control 0: Disable 1: PWM0P enable and output to P2.1
		1	PWM0NOE0	R/W	0	PWM0N output control 0: Disable 1: PWM0N enable and output to P1.3
		0	PWM0POE0	R/W	0	PWM0P output control 0: Disable 1: PWM0P enable and output to P1.2

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
B7h	**PWMOE1**	7	PWM6OE1	R/W	0	PWM6 output control 0: Disable 1: PWM6 enable and output to P0.7
		6	PWM6OE0	R/W	0	PWM6 output control 0: Disable 1: PWM6 enable and output to P3.7
		5	PWM5OE1	R/W	0	PWM5 output control 0: Disable 1: PWM5 enable and output to P0.6
		4	PWM5OE0	R/W	0	PWM5 output control 0: Disable 1: PWM5 enable and output to P3.4
		3	PWM4OE1	R/W	0	PWM4 output control 0: Disable 1: PWM4 enable and output to P0.5
		2	PWM4OE0	R/W	0	PWM4 output control 0: Disable 1: PWM4 enable and output to P3.5
		1	PWM3OE1	R/W	0	PWM3 output control 0: Disable 1: PWM3 enable and output to P0.4
		0	PWM3OE0	R/W	0	PWM3 output control 0: Disable 1: PWM3 enable and output to P1.6
B8h	**IP**	5	PT2	R/W	0	Timer2 Interrupt Priority Low bit
		4	PS	R/W	0	Serial Port (UART1) Interrupt Priority Low bit
		3	PT1	R/W	0	Timer1 Interrupt Priority Low bit
		2	PX1	R/W	0	External INT1 Pin Interrupt Priority Low bit
		1	PT0	R/W	0	Timer0 Interrupt Priority Low bit
		0	PX0	R/W	0	External INT0 Pin Interrupt Priority Low bit
B9h	**IPH**	5	PT2H	R/W	0	Timer2 Interrupt Priority High bit
		4	PSH	R/W	0	Serial Port (UART1) Interrupt Priority High bit
		3	PT1H	R/W	0	Timer1 Interrupt Priority High bit
		2	PX1H	R/W	0	External INT1 Pin Interrupt Priority High bit
		1	PT0H	R/W	0	Timer0 Interrupt Priority High bit
		0	PX0H	R/W	0	External INT0 Pin Interrupt Priority High bit
BAh	**IP1**	7	PPWM	R/W	0	PWM0/PWM1 Interrupt Priority Low bit
		6	PS2	R/W	0	Serial Port (UART2) Interrupt Priority Low bit
		5	PLVD	R/W	0	LVD Interrupt Priority Low bit
		4	PSPI2C	R/W	0	SPI/I^2C Interrupt Priority Low bit
		3	PADTKI	R/W	0	ADC/TK Interrupt Priority Low bit
		2	PX2	R/W	0	External INT2 Pin Interrupt Priority Low bit
		1	PPC	R/W	0	Port0~Port3 pin change Interrupt Priority Low bit
		0	PT3	R/W	0	Timer3 Interrupt Priority Low bit
BBh	**IP1H**	7	PPWMH	R/W	0	PWM0/PWM1 Interrupt Priority High bit
		6	PS2H	R/W	0	Serial Port (UART2) Interrupt Priority High bit
		5	PLVDH	R/W	0	LVD Interrupt Priority High bit
		4	PI2CH	R/W	0	SPI/I^2C Interrupt Priority High bit
		3	PADTKIH	R/W	0	ADC/TK Interrupt Priority High bit
		2	PX2H	R/W	0	External INT2 Pin Interrupt Priority High bit
		1	PPCH	R/W	0	Port0~Port3 Interrupt Priority High bit
		0	PT3H	R/W	0	Timer3 Interrupt Priority High bit

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
BCh	**SPCON**	7	SPEN	R/W	0	SPI enable 0: SPI disable 1: SPI enable
		6	MSTR	R/W	0	Master mode enable 0: Slave mode 1: Master mode
		5	CPOL	R/W	0	SPI clock polarity 0: SCK is low in idle state 1: SCK is high in idle state
		4	CPHA	R/W	0	SPI clock phase 0: Data sample on first edge of SCK period 1: Data sample on second edge of SCK period
		2	LSBF	R/W	0	LSB first 0: MSB first 1: LSB first
		1~0	SPCR	R/W	00	SPI clock rate 00: $F_{SYSCLK}/2$ 01: $F_{SYSCLK}/4$ 10: $F_{SYSCLK}/8$ 11: $F_{SYSCLK}/16$
BDh	**SPSTA**	7	SPIF	R/W	0	SPI interrupt flag This is set by H/W at the end of a data transfer. Cleared by H/W when an interrupt is vectored into. Writing 0 to this bit will clear this flag.
		6	WCOL	R/W	0	Write collision interrupt flag Set by H/W if write data to SPDAT when SPBSY is set. Write 0 to this bit or rewrite data to SPDAT when SPBSY is cleared will clear this flag.
		4	RCVOVF	R/W	0	Received buffer overrun flag Set by H/W at the end of a data transfer and RCVBF is set. Write 0 to this bit or read SPDAT register will clear this flag.
		3	RCVBF	R/W	0	Receive buffer full flag Set by H/W at the end of a data transfer. Write 0 to this bit or read SPDAT register will clear this flag.
		2	SPBSY	R	0	SPI busy flag Set by H/W when a SPI transfer is in progress.
BEh	**SPDAT**	7~0	SPDAT	R/W	00h	SPI transmit and receive data The SPDAT register is used to transmit and receive data. Writing data to SPDAT place the data into shift register and start a transfer when in master mode. Reading SPDAT returns the contents of the receive buffer.
C1h	**SIADR**	7~1	SA	R/W	64h	Slave I²C address assigned
		0	SIEN	R/W	0	Slave I²C enable 0: disable 1: enable
C2h	**SICON**	7	MIIE	R/W	0	I^2C Master interrupt enable 0: disable 1: enable
		6	TXDIE	R/W	0	Slave I²C transmission completed interrupt enable 0: disable 1: enable
		5	RCD2IE	R/W	0	Slave I²C DATA2(SITXRCD2) reception completed interrupt enable 0: disable 1: enable
		4	RCD1IE	R/W	0	Slave I²C DATA1(SIRCD1) reception completed interrupt enable 0: disable 1: enable
		2	TXDF	R/W	1	Slave I²C transmission completed interrupt flag 0: write 0 to clear it 1: Set by H/W when Slave I²C transmission complete
		1	RCD2F	R/W	0	Slave I²C DATA2 (SITXRCD2) reception completed interrupt flag 0: write 0 to clear it 1: Set by H/W when Slave I²C DATA2 (SITXRCD2) reception complete

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		0	RCD1F	R/W	0	Slave I²C DATA1 (SIRCD1) reception completed interrupt flag 0: write 0 to clear it 1: Set by H/W when Slave I²C DATA1 (SIRCD1) reception complete
C3h	**SIRCD1**	7~0	SIRCD1	R	–	Slave I²C data receive register1 (DATA1)
C4h	**SITXRCD2**	7~0	SITXRCD2	R/W	–	Slave I²C transmit and receive data register Read: Slave I²C data receive register2 (DATA2) Write: Slave I²C data transmission register (TXD)
C5h	**ATKCH0**	7~0	ATKCH0	R/W	00h	TK7~TK0 channel scan enable: 0: disable 1: enable (if MCHS=0, Select ATK Scan ; if MCHS=1, Select Bundle Scan)
C6h	**ATKCH1**	7~0	ATKCH1	R/W	00h	TK15~TK8 channel scan enable: 0: disable 1: enable (if MCHS=0, Select ATK Scan ; if MCHS=1, Select Bundle Scan)
C7h	**ATKCH2**	7~0	ATKCH2	R/W	00h	TK23 (TKCAP) ~TK16 channel scan enable: 0: disable 1: enable (if MCHS=0, Select ATK Scan ; if MCHS=1, Select Bundle Scan)
C8h	**T2CON**	7	TF2	R/W	0	Timer2 overflow flag Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.
		6	EXF2	R/W	0	T2EX interrupt pin falling edge flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.
		5	RCLK	R/W	0	UART receive clock control bit 0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3 1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3
		4	TCLK	R/W	0	UART transmit clock control bit 0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3 1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3
		3	EXEN2	R/W	0	T2EX pin enable 0: T2EX pin disable 1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0
		2	TR2	R/W	0	Timer2 run control 0:timer stops 1:timer runs
		1	CT2N	R/W	0	Timer2 Counter/Timer select bit 0: Timer mode, Timer2 data increases at 2 System clock cycle rate 1: Counter mode, Timer2 data increases at T2 pin's negative edge
		0	CPRL2N	R/W	0	Timer2 Capture/Reload control bit 0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1. 1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1. If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.
C9h	**IAPCON**	7~0	IAPCON	W	–	Write 47h or 74h to set IAPWE flag; Write 47h can write 1 byte at once, write 74h can write 2 bytes at once. Write other value to clear IAPWE flag. It is recommended to clear it immediately after IAP write. Write A1h to set INFOWE flag; write other value to clear INFOWE flag. It is recommended to clear it immediately after IAP write. Write E2h to set EEPWE flag; write other value to clear EEPWE flag. It is recommended to clear it immediately after EEPROM write.
		7	IAPWE	R	0	Flag indicates Flash memory can be written by IAP or not 0: IAP Write disable 1: IAP Write enable
		6	IAPTO	R	0	Time-Out flag of IAP write/EEPROM write/INFO write. Set by H/W when IAP or EEPROM or INFO write Time-out occurs. Cleared this flag by H/W when IAPWE=0 or EEPWE=0 or INFOWE=0.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		5	EEPWE	R	0	Flag indicates EEPROM memory can be written or not 0: EEPROM Write disable 1: EEPROM Write enable
		4	INFOWE	R	0	Flag indicates INFO memory can be written or not 0: INFO IAP Write disable 1: INFO IAP Write enable
CAh	**RCP2L**	7~0	RCP2L	R/W	00h	Timer2 reload/capture data low byte
CBh	**RCP2H**	7~0	RCP2H	R/W	00h	Timer2 reload/capture data high byte
CCh	**TL2**	7~0	TL2	R/W	00h	Timer2 data low byte
CDh	**TH2**	7~0	TH2	R/W	00h	Timer2 data high byte
CEh	**EXA2**	7~0	EXA2	R/W	00h	Expansion accumulator 2
CFh	**EXA3**	7~0	EXA3	R/W	00h	Expansion accumulator 3
D0h	**PSW**	7	CY	R/W	0	ALU carry flag
		6	AC	R/W	0	ALU auxiliary carry flag
		5	F0	R/W	0	General purpose user-definable flag
		4	RS1	R/W	0	Register Bank Select bit 1
		3	RS0	R/W	0	Register Bank Select bit 0
		2	OV	R/W	0	ALU overflow flag
		1	F1	R/W	0	General purpose user-definable flag
		0	P	R/W	0	Parity flag
D1h	**PWM0DH**	7~0	PWM0DH	R/W	00h	PWM0 duty high byte write sequence: PWM0DL then PWM0DH read sequence: PWM0DH then PWM0DL
D2h	**PWM0DL**	7~0	PWM0DL	R/W	00h	PWM0 duty low byte write sequence: PWM0DL then PWM0DH read sequence: PWM0DH then PWM0DL
D3h	**PWM1DH**	7~0	PWM1DH	R/W	00h	PWM1 duty high byte write sequence: PWM1DL then PWM1DH read sequence: PWM1DH then PWM1DL
D4h	**PWM1DL**	7~0	PWM1DL	R/W	00h	PWM1 duty low byte write sequence: PWM1DL then PWM1DH read sequence: PWM1DH then PWM1DL
D5h	**PWM2DH**	7~0	PWM2DH	R/W	00h	PWM2 duty high byte write sequence: PWM2DL then PWM2DH read sequence: PWM2DH then PWM2DL
D6h	**PWM2DL**	7~0	PWM2DL	R/W	00h	PWM2 duty low byte write sequence: PWM2DL then PWM2DH read sequence: PWM2DH then PWM2DL
D7h	**TKCON3**	2~0	JMPVL	R/W	000	Touch Key clock frequency LSB 3bit (Fine tune) select, only available in TKFJMP=0 [JMPVH, JMPVL]=000_000=frequency slowest [JMPVH, JMPVL]=111_111=frequency fastest
D8h	**CLKCON**	7	SCKTYPE	R/W	0	Slow clock Type. This bit can be changed only in Fast mode (SELFCK=1) 0: SRC 1: SXT, P2.0 and P2.1 are crystal pins
		6	FCKTYPE	R/W	0	Fast clock type. This bit can be changed only in Slow mode (SELFCK=0). 0: FRC 1: FXT, P2.0 and P2.1 are crystal pins, oscillator gain is high for FXT
		5	STPSCK	R/W	1	Set 1 to stop SRC clock in PDOWN mode
		4	STPPCK	R/W	0	Set 1 to stop UART/Timer0/1/2 clock in Idle mode for current reducing.
		3	STPFCK	R/W	0	Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.
		2	SELFCK	R/W	0	System clock select. This bit can be changed only when STPFCK=0. 0: Slow clock 1: Fast clock

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		1~0	CLKPSC	R/W	11	System clock prescaler. Effective after 16 clock cycles (Max.) delay. 00: System clock is Fast/Slow clock divided by 16 01: System clock is Fast/Slow clock divided by 4 10: System clock is Fast/Slow clock divided by 2 11: System clock is Fast/Slow clock divided by 1
D9h	**PWM0PRDH**	7~0	PWM0PRDH	R/W	FFh	PWM0 period high byte write sequence: PWM0PRDL then PWM0PRDH read sequence: PWM0PRDH then PWM0PRDL
DAh	**PWM0PRDL**	7~0	PWM0PRDL	R/W	FFh	PWM0 period low byte write sequence: PWM0PRDL then PWM0PRDH read sequence: PWM0PRDH then PWM0PRDL
DBh	**PWM1PRDH**	7~0	PWM1PRDH	R/W	FFh	PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 period high byte write sequence: PWM1PRDL then PWM1PRDH read sequence: PWM1PRDH then PWM1PRDL
DCh	**PWM1PRDL**	7~0	PWM1PRDL	R/W	FFh	PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 period low byte write sequence: PWM1PRDL then PWM1PRDH read sequence: PWM1PRDH then PWM1PRDL
DDh	**PWM3DH**	7~0	PWM3DH	R/W	00h	PWM3 duty high byte write sequence: PWM3DL then PWM3DH read sequence: PWM3DH then PWM3DL
DEh	**PWM3DL**	7~0	PWM3DL	R/W	00h	PWM3 duty low byte write sequence: PWM3DL then PWM3DH read sequence: PWM3DH then PWM3DL
DFh	**UART1CON**	7	UART1BRS	R/W	0	UART1 Baud Rate source select 0: 8051 default Baud Rate source select 1: UART1 Baud Rate select as UART1BRP
		6~0	UART1BRP	R/W	00h	Define UART1 Baud Rate prescaler UART1 Baud Rate = F_{SYSCLK}/32/UART1BRP
E0h	**ACC**	7~0	ACC	R/W	00h	Accumulator
E1h	**MICON**	7	MIEN	R/W	0	Master I^2C enable 0: disable 1: enable
		6	MIACKO	R/W	0	When Master I^2C receive data, send acknowledge to I^2C bus 0: ACK to slave device 1: NACK to slave device
		5	MIIF	R/W	0	Master I^2C Interrupt flag 0: write 0 to clear it 1: Master I^2C transfer one byte complete
		4	MIACKI	R	–	When Master I^2C transfer, acknowledgement form I^2C bus (read only) 0: ACK received 1: NACK received
		3	MISTART	R/W	0	Master I^2C Start bit 1: start I^2C bus transfer
		2	MISTOP	R/W	1	Master I^2C Stop bit 1: send STOP signal to stop I^2C bus
		1~0	MICR	R/W	00	Master I^2C (SCL) clock frequency selection 00: F_{SYSCLK}/4 (ex. If F_{SYSCLK}=16MHz, I^2C clock is 4M Hz) 01: F_{SYSCLK}/16 (ex. If F_{SYSCLK}=16MHz, I^2C clock is 1M Hz) 10: F_{SYSCLK}/64 (ex. If F_{SYSCLK}=16MHz, I^2C clock is 250K Hz) 11: F_{SYSCLK}/256 (ex. If F_{SYSCLK}=16MHz, I^2C clock is 62.5K Hz)
E2h	**MIDAT**	7~0	MIDAT	R/W	00h	Master I^2C data shift register (W): After Start and before Stop condition, write this register will resume transmission to I^2C bus (R): After Start and before Stop condition, read this register will resume receiving from I^2C bus

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
E3h	**LVRCON**	5	PORPD	R/W	0	POR power down 0: POR enable 1: POR disable
		4	LVRPD	R/W	0	LVR power down 0: LVR enable 1: LVR disable
		3~0	LVRSEL	R/W	0000	Low Voltage Reset (LVR) select. (step=0.14V) 0000: Set LVR at 2.05V 0001: Set LVR at 2.19V 0010: Set LVR at 2.33V 0011: Set LVR at 2.47V 0100: Set LVR at 2.61V 0101: Set LVR at 2.75V 0110: Set LVR at 2.89V 0111: Set LVR at 3.03V 1000: Set LVR at 3.17V 1001: Set LVR at 3.31V 1010: Set LVR at 3.45V 1011: Set LVR at 3.59V 1100: Set LVR at 3.73V 1101: Set LVR at 3.87V 1110: Set LVR at 4.01V 1111: Set LVR at 4.15V
E4h	**LVDCON**	7	LVDM	R/W	0	Low Voltage Detect interrupt enable 0: LVDIF =1 and LVDO =1 while $V_{CC} < V_{LVD}$ 1: LVDIF =1 and LVDO =1 while $V_{CC} > V_{LVD}$
		6	LVDO	R	0	Low Voltage Detect output
		5	LVDHYS	R/W	0	LVD Hysteresis Enable 0: LVD Hysteresis disable 1: LVD Hysteresis enable
		4	LVDPD	R/W	0	LVD power down 0: LVD enable 1: LVD disable
		3~0	LVDSEL	R/W	0000	Low Voltage Detect (LVD) select. (step=0.14V) 0000: Set LVD at 2.05V 0001: Set LVD at 2.19V 0010: Set LVD at 2.33V 0011: Set LVD at 2.47V 0100: Set LVD at 2.61V 0101: Set LVD at 2.75V 0110: Set LVD at 2.89V 0111: Set LVD at 3.03V 1000: Set LVD at 3.17V 1001: Set LVD at 3.31V 1010: Set LVD at 3.45V 1011: Set LVD at 3.59V 1100: Set LVD at 3.73V 1101: Set LVD at 3.87V 1110: Set LVD at 4.01V 1111: Set LVD at 4.15V

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
E5h	**EFTCON**	7	EFT2CS	R/W	0	EFT2 Detector enable 0: Disable EFT2 1: Enable EFT2
		6	EFT1CS	R/W	0	EFT1 Detector enable 0: Disable EFT1 1: Enable EFT1
		5~4	EFT1S	R/W	00	EFT1 Detector sensitivity adjustment
		3	EFTSLOW	R/W	0	Force System clock to Slow clock while EFT detected 0: Disable 1: Enable
		1	EFTWOUT	R/W	0	EFTWAIT output to pin 0: P3.6 = normal I/O 1: P3.6 = EFTWAIT
		0	CKHLDE	R/W	0	clock hold enable 0: Disable 1: Enable
E6h	**EXA**	7~0	EXA	R/W	00h	Expansion accumulator
E7h	**EXB**	7~0	EXB	R/W	00h	Expansion B register
E9h	**PWM4DH**	7~0	PWM4DH	R/W	00h	PWM4 duty high byte write sequence: PWM4DL then PWM4DH read sequence: PWM4DH then PWM4DL
EAh	**PWM4DL**	7~0	PWM4DL	R/W	00h	PWM4 duty low byte write sequence: PWM4DL then PWM4DH read sequence: PWM4DH then PWM4DL
EBh	**PWM5DH**	7~0	PWM5DH	R/W	00h	PWM5 duty high byte write sequence: PWM5DL then PWM5DH read sequence: PWM5DH then PWM5DL
ECh	**PWM5DL**	7~0	PWM5DL	R/W	00h	PWM5 duty low byte write sequence: PWM5DL then PWM5DH read sequence: PWM5DH then PWM5DL
EDh	**PWM6DH**	7~0	PWM6DH	R/W	00h	PWM6 duty high byte write sequence: PWM6DL then PWM6DH read sequence: PWM6DH then PWM6DL
EEh	**PWM6DL**	7~0	PWM6DL	R/W	00h	PWM6 duty low byte write sequence: PWM6DL then PWM6DH read sequence: PWM6DH then PWM6DL
EFh	**AUX3**	6	HSNK2EN	R/W	0	Pin high sink enable (Group 2 = P04, P05, P10~P13, P30~P33) 0: Group 2 high sink disable 1: Group 2 high sink enable
		5	HSNK1EN	R/W	0	Pin high sink enable (Group 1 = P06, P07, P14~P17, P35, P36) 0: Group 1 high sink disable 1: Group 1 high sink enable
		4	HSNK0EN	R/W	0	Pin high sink enable (Group 0 = P00~P03, P20, P21, P34, P37) 0: Group 0 high sink disable 1: Group 0 high sink enable
		3	WARMTIME	R/W	0	Warm-up time for wake-up from Halt/Stop mode 0: 128 Clock 1: 64 Clock
		1	FJMPE	R/W	0	FRC frequency auto-change enable 0: FRC frequency define by CFGWL 1: FRC frequency auto-change enable
		0	FJMPS	R/W	0	FRC frequency auto-change selection 0: ±1% frequency change 1: ±2% frequency change
F0h	**B**	7~0	B	R/W	00h	B register
F1h	**CRCDL**	7~0	CRCDL	R/W	FFh	16-bit CRC data bit 7~0
F2h	**CRCDH**	7~0	CRCDH	R/W	FFh	16-bit CRC data bit 15~8
F3h	**CRCIN**	7~0	CRCIN	W	–	CRC input data
F5h	**CFGBG**	4~0	BGTRIM	R/W	–	VBG trimming value

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
F6h	**CFGWL**	6~0	FRCF	R/W	–	FRC frequency adjustment 00h: lowest frequency 7Fh: highest frequency
F7h	**AUX2**	7~6	WDTE	R/W	–	Watchdog Timer Reset control 0x: WDT disable 10: WDT enable in Fast/Slow mode, disable in Idle/Halt/Stop mode 11: WDT always enable
		5	PWRSAV	R/W	–	Set 1 to reduce the chip's power consumption at Idle/Halt/Stop Mode.
		4	VBGOUT	R/W	0	Bandgap voltage output control 0: P3.2 as normal I/O 1: Bandgap voltage output to P3.2 pin
		3	DIV32	R/W	0	only active when MULDVI16 =1 0: instruction DIV as 16/16 bit division operation 1: instruction DIV as 32/16 bit division operation
		2~1	IAPTE	R/W	11	IAP write/EEPROM write/INFO write watchdog timer enable 00: Disable 01: wait 3ms trigger watchdog time-out flag 10: wait 6ms trigger watchdog time-out flag 11: wait 25ms trigger watchdog time-out flag
		0	MULDIV16	R/W	0	0: instruction MUL/DIV as 8*8, 8/8 operation 1: instruction MUL/DIV as 16*16, 16/16 or 32/16 operation
F8h	**AUX1**	7	CLRWDT	R/W	0	Set 1 to clear WDT, H/W auto clear it at next clock cycle
		6	CLRTM3	R/W	0	Set 1 to clear and hold Timer3, need S/W clear.
		5	TKSOC	R/W	0	Touch Key Start of Conversion Set 1 to start Touch Key conversion, and S/W need to write 0 to clear this flag
		4	ADSOC	R/W	0	ADC Start of Conversion Set 1 to start ADC conversion. Cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
		3	CLRPWM0	R/W	1	PWM0 clear enable 0: PWM0 is running 1: PWM0 is cleared and held or set PWM0 stop status by PWM0PMSK/PWM0NMSK & PWM0MSK=1
		2	CLRPWM1	R/W	1	PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 clear enable 0: PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 is running 1: PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 is cleared and held
		0	DPSEL	R/W	0	Active DPTR Select

Adr	Flash	Bit#	Bit Name	Description
3FFBh	**CFGBG**	4~0	BGTRIM	VBG adjustment. V_{BG} is trimmed to 1.18V in chip manufacturing.
3FFDh	**CFGWL**	6~0	FRCF	FRC frequency adjustment. FRC is trimmed to 18.432 MHz in chip manufacturing.
3FFFh	**CFGWH**	7	PROT	Flash Code Protect, 1=Protect
		6	XRSTE	External Pin Reset Enable, 1=Enable.
		5	PORSEL	POR enable selection 0: POR always on (when PORPD=0) 1: POR turn on 2ms (1/8duty when PORPD=0)
		4	HVS	High voltage switch for ROM write.
		3~0	-	Reserved

INSTRUCTION SET

Instructions are 1, 2 or 3 bytes long as listed in the 'byte' column below. Each instruction takes 1~8 System clock cycles to execute as listed in the 'cycle' column below.

ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ADD A,Rn	Add register to A	1	2	28-2F
ADD A,dir	Add direct byte to A	2	2	25
ADD A,@Ri	Add indirect memory to A	1	2	26-27
ADD A,#data	Add immediate to A	2	2	24
ADDC A,Rn	Add register to A with carry	1	2	38-3F
ADDC A,dir	Add direct byte to A with carry	2	2	35
ADDC A,@Ri	Add indirect memory to A with carry	1	2	36-37
ADDC A,#data	Add immediate to A with carry	2	2	34
SUBB A,Rn	Subtract register from A with borrow	1	2	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	2	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	2	04
INC Rn	Increment register	1	2	08-0F
INC dir	Increment direct byte	2	2	05
INC @Ri	Increment indirect memory	1	2	06-07
DEC A	Decrement A	1	2	14
DEC Rn	Decrement register	1	2	18-1F
DEC dir	Decrement direct byte	2	2	15
DEC @Ri	Decrement indirect memory	1	2	16-17
INC DPTR	Increment data pointer	1	4	A3
MUL AB	Multiply A by B	1	8/16	A4
DIV AB	Divide A by B	1	8/16/32	84
DA A	Decimal Adjust A	1	2	D4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ANL A,Rn	AND register to A	1	2	58-5F
ANL A,dir	AND direct byte to A	2	2	55
ANL A,@Ri	AND indirect memory to A	1	2	56-57
ANL A,#data	AND immediate to A	2	2	54
ANL dir,A	AND A to direct byte	2	2	52
ANL dir,#data	AND immediate to direct byte	3	4	53
ORL A,Rn	OR register to A	1	2	48-4F
ORL A,dir	OR direct byte to A	2	2	45
ORL A,@Ri	OR indirect memory to A	1	2	46-47
ORL A,#data	OR immediate to A	2	2	44
ORL dir,A	OR A to direct byte	2	2	42
ORL dir,#data	OR immediate to direct byte	3	4	43
XRL A,Rn	Exclusive-OR register to A	1	2	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	2	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	2	66-67
XRL A,#data	Exclusive-OR immediate to A	2	2	64
XRL dir,A	Exclusive-OR A to direct byte	2	2	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	4	63
CLR A	Clear A	1	2	E4
CPL A	Complement A	1	2	F4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
SWAP A	Swap Nibbles of A	1	2	C4
RL A	Rotate A left	1	2	23
RLC A	Rotate A left through carry	1	2	33
RR A	Rotate A right	1	2	03
RRC A	Rotate A right through carry	1	2	13

DATA TRANSFER				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MOV A,Rn	Move register to A	1	2	E8-EF
MOV A,dir	Move direct byte to A	2	2	E5
MOV A,@Ri	Move indirect memory to A	1	2	E6-E7
MOV A,#data	Move immediate to A	2	2	74
MOV Rn,A	Move A to register	1	2	F8-FF
MOV Rn,dir	Move direct byte to register	2	4	A8-AF
MOV Rn,#data	Move immediate to register	2	2	78-7F
MOV dir,A	Move A to direct byte	2	2	F5
MOV dir,Rn	Move register to direct byte	2	4	88-8F
MOV dir,dir	Move direct byte to direct byte	3	4	85
MOV dir,@Ri	Move indirect memory to direct byte	2	4	86-87
MOV dir,#data	Move immediate to direct byte	3	4	75
MOV @Ri,A	Move A to indirect memory	1	2	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	4	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	2	76-77
MOV DPTR,#data	Move immediate to data pointer	3	4	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	8	93
MOVC A,@A+PC	Move code byte relative PC to A	1	8	83
MOVX A,@Ri	Move external data(A8) to A	1	8	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	8	E0
MOVX @Ri,A	Move A to external data(A8)	1	8	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	8	F0
PUSH dir	Push direct byte onto stack	2	4	C0
POP dir	Pop direct byte from stack	2	4	D0
XCH A,Rn	Exchange A and register	1	2	C8-CF
XCH A,dir	Exchange A and direct byte	2	2	C5
XCH A,@Ri	Exchange A and indirect memory	1	2	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2	D6-D7

BOOLEAN				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
CLR C	Clear carry	1	2	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	2	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	2	B3
CPL bit	Complement direct bit	2	2	B2
ANL C,bit	AND direct bit to carry	2	4	82
ANL C,/bit	AND direct bit inverse to carry	2	4	B0
ORL C,bit	OR direct bit to carry	2	4	72
ORL C,/bit	OR direct bit inverse to carry	2	4	A0
MOV C,bit	Move direct bit to carry	2	2	A2
MOV bit,C	Move carry to direct bit	2	4	92

BRANCHING				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ACALL addr 11	Absolute jump to subroutine	2	6	11-F1
LCALL addr 16	Long jump to subroutine	3	6	12
RET	Return from subroutine	1	6	22
RETI	Return from interrupt	1	6	32
AJMP addr 11	Absolute jump unconditional	2	6	01-E1
LJMP addr 16	Long jump unconditional	3	6	02
SJMP rel	Short jump (relative address)	2	6	80
JC rel	Jump on carry = 1	2	4 (or 6)	40
JNC rel	Jump on carry = 0	2	4 (or 6)	50
JB bit,rel	Jump on direct bit = 1	3	4 (or 6)	20
JNB bit,rel	Jump on direct bit = 0	3	4 (or 6)	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	4 (or 6)	10
JMP @A+DPTR	Jump indirect relative DPTR	1	6	73
JZ rel	Jump on accumulator = 0	2	4 (or 6)	60
JNZ rel	Jump on accumulator ≠ 0	2	4 (or 6)	70
CJNE A,dir,rel	Compare A,direct, jump not equal relative	3	4 (or 6)	B5
CJNE A,#data,rel	Compare A,immediate, jump not equal relative	3	4 (or 6)	B4
CJNE Rn,#data,rel	Compare register,immediate, jump not equal relative	3	4 (or 6)	B8-BF
CJNE @Ri,#data,rel	Compare indirect,immediate, jump not equal relative	3	4 (or 6)	B6-B7
DJNZ Rn,rel	Decrement register, jump not zero relative	2	4 (or 6)	D8-DF
DJNZ dir,rel	Decrement direct byte, jump not zero relative	3	4 (or 6)	D5

MISCELLANEOUS				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
NOP	No operation	1	2	00

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11-F1 (for example), are used for absolute jumps and calls with the top 3 bits of the code being used to store the top three bits of the destination address.

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (T_A=25℃)

Parameter	Rating	Unit
Supply voltage	V_{SS} –0.3 ~ V_{SS} +5.5	V
Input voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
All pins output current high	–80	mA
All pins output current low	+150	
Maximum Operating Voltage	5.5	V
Operating temperature	–40 ~ +105	℃
Storage temperature	–65 ~ +150	

2. DC Characteristics (T_A=25 ℃, V_{CC}=2.2V ~ 5.5V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Operating Voltage	V_{CC}	F_{SYSCLK}=18.432 MHz		2.2	–	5.5	V
Input High Voltage	V_{IH}	All Input	V_{CC}=5V	0.6V_{CC}	–	–	V
			V_{CC}=3V	0.6V_{CC}	–	–	V
Input Low Voltage	V_{IL}	All Input	V_{CC}=5V	–	–	0.2V_{CC}	V
			V_{CC}=3V	–	–	0.2V_{CC}	V
I/O Port Source Current	I_{OH}	All Output LEDBRITM=1	V_{CC}=5V, V_{OH}=0.9V_{CC}	6	12	–	mA
			V_{CC}=5V, V_{OH}=0.6V_{CC}	20	40	–	
			V_{CC}=3V, V_{OH}=0.9V_{CC}	2.5	5	–	
			V_{CC}=3V, V_{OH}=0.66V_{CC}	7.5	15	–	
		LED Pins (P0.0~P0.3, P0.6~P0.7, P1.4~P1.7, P2.0~P2.1, P3.4~P3.7) LEDBRITM=0	V_{CC}=5V, V_{OH}=0.9V_{CC}	6	12	–	
			V_{CC}=5V, V_{OH}=0.6V_{CC}	10	20	–	
			V_{CC}=3V, V_{OH}=0.9V_{CC}	2.5	5	–	
			V_{CC}=3V, V_{OH}=0.66V_{CC}	5	10	–	
I/O Port Sink Current	I_{OL}	All Output,	V_{CC}=5V, V_{OL}=0.1V_{CC} HSNKxEN=1	72	90	–	mA
			V_{CC}=5V, V_{OL}=0.1V_{CC} HSNKxEN=0	23	46	–	
			V_{CC}=3V, V_{OL}=0.1V_{CC} HSNKxEN=1	20	40	–	
			V_{CC}=3V, V_{OL}=0.1V_{CC} HSNKxEN=0	10	20	–	

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Supply Current	I_{DD}	Fast mode V_{CC}=5V	FRC=18.432 MHz	–	8.1	–	mA
			FRC=9.216 MHz	–	5.5	–	
		Fast mode V_{CC}=3V	FRC=18.432 MHz	–	4.6	–	
			FRC=9.216 MHz	–	3.2	–	
		Slow mode	V_{CC}=5V	–	2.1	–	
			V_{CC}=3V	–	1.4	–	
		Idle mode PWRSAV=0	SRC, V_{CC}=5V	–	75	–	µA
			SRC, V_{CC}=3V	–	50	–	
		Idle mode PWRSAV=1	SRC, V_{CC}=5V	–	16.5	–	
			SRC, V_{CC}=3V	–	7.2	–	
		Idle mode PWRSAV=1 PORPD=1	SRC, V_{CC}=5V	–	9.7	–	
			SRC, V_{CC}=3V	–	3.6	–	
		Stop mode PWRSAV=1	V_{CC}=5V	–	0.4	–	
			V_{CC}=3V	–	0.2	–	
		Halt mode PWRSAV=1	V_{CC}=5V	–	7.2	–	
			V_{CC}=3V	–	2.4	–	
Pull-Up Resistor	R_{PU}	V_{IN}=V_{CC}	V_{CC}=5V	–	32	–	KΩ
			V_{CC}=3V	–	54	–	

3. Clock Timing

Parameter	Condition	Min	Typ	Max	Unit
FRC Frequency	25℃, V_{CC}=4.5V	–1%	18.432	+1%	MHz
	0℃ ~ 105℃, V_{CC}=4.5V	–1.5%	18.432	+1.5%	
	-40℃ ~ 105℃, V_{CC}=3.0 ~ 5.5V	–3.5%	18.432	+3.5%	
SRC Frequency	V_{CC}=5V	–	41	–	KHz
	V_{CC}=3V	–	37	–	

4. Reset Timing Characteristics (T_A= –40°C ~ +105°C)

Parameter	Conditions	Min	Typ	Max	Unit
RESET Input Low width	Input V_{CC}=5V ± 10 %	30	–	–	µs
WDT wake up time	V_{CC}=5V, WDTPSC=11	–	50	–	ms
	V_{CC}=3V, WDTPSC=11	–	55	–	
CPU start up time	V_{CC} = 5 V	–	22	–	ms

5. LVR Circuit Characteristics (T_A = 25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVR Reference Voltage	V_{LVR}	T_A=25°C	–	4.15	–	V
			–	4.01	–	
			–	3.87	–	
			–	3.73	–	
			–	3.59	–	
			–	3.45	–	
			–	3.31	–	
			–	3.17	–	
			–	3.03	–	
			–	2.89	–	
			–	2.75	–	
			–	2.61	–	
			–	2.47	–	
			–	2.33	–	
			–	2.19	–	
			–	2.05	–	
LVR Hysteresis Window	V_{HYS_LVR}	T_A = 25℃	–	20	–	mV
Low Voltage Detection time	t_{LVR}	T_A=25°C	100	–	–	μs

6. LVD Circuit Characteristics (T_A = 25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVD Reference Voltage	V_{LVD}	T_A=25°C	–	4.15	–	V
			–	4.01	–	
			–	3.87	–	
			–	3.73	–	
			–	3.59	–	
			–	3.45	–	
			–	3.31	–	
			–	3.17	–	
			–	3.03	–	
			–	2.89	–	
			–	2.75	–	
			–	2.61	–	
			–	2.47	–	
			–	2.33	–	
			–	2.19	–	
			–	2.05	–	
LVD Hysteresis Window	V_{HYS_LVD}	LVDHYS = 0	–	20	–	mV
		LVDHYS = 1	–	60	–	
Low Voltage Detection time	t_{LVR}	T_A=25°C	100	–	–	μs

7. ADC Electrical Characteristics (T_A= 25°C, V_{CC}= 3.0V ~ 5.5V, V_{SS}= 0V)

Parameter	Conditions		Min	Typ	Max	Unit
Total Accuracy	V_{CC}=5.12 V, V_{SS}=0V		–	±2.5	±4	LSB
Integral Non-Linearity			–	±3.2	±5	
Max Input Clock (f_{ADC})	Source impedance (Rs < 5KΩ)		–	–	4.2	MHz
	Source impedance (Rs < 10KΩ)		–	–	2.1	
	Source impedance (Rs < 25KΩ)		–	–	1.1	
	Source is V_{BG} (ADCHS=01100b)		–	–	4.2	
Conversion Time	F_{ADC} = 1MHz		–	50	–	μs
Conversion Current	V_{CC}=5V, ADCVREFS=0		–	0.45	–	mA
	V_{CC}=4V, ADCVREFS=1		–	0.6	–	
BandGap Voltage Reference (V_{BG})	–	V_{CC}=2.5V~5.5V 25℃	-1.5%	1.18	+1.5%	V
		V_{CC}=2.5V~5.5V -40℃~105℃	-1.8%	1.18	+1.8%	
ADC Reference Voltage (V_{ADC})	ADCVREFS=1	V_{CC}=3V~5.5V 25℃	-1.7%	2.49	+1.7%	
		V_{CC}=2.8V~5.5V -40℃~105℃	-2.3%	2.49	+2.3%	
V_{CC}/4 Reference Voltage ($V_{1/4}$)	–	V_{CC}=5V, 25°C	-0.8%	1.252	+0.8%	
		V_{CC}=3.6V, 25°C	-0.8%	0.902	+0.8%	
Input Voltage	–		V_{SS}	–	V_{CC}	

8. TK Electrical Characteristics (T_A= 25°C, V_{CC}= 3.0V ~ 5.5V, V_{SS}= 0V)

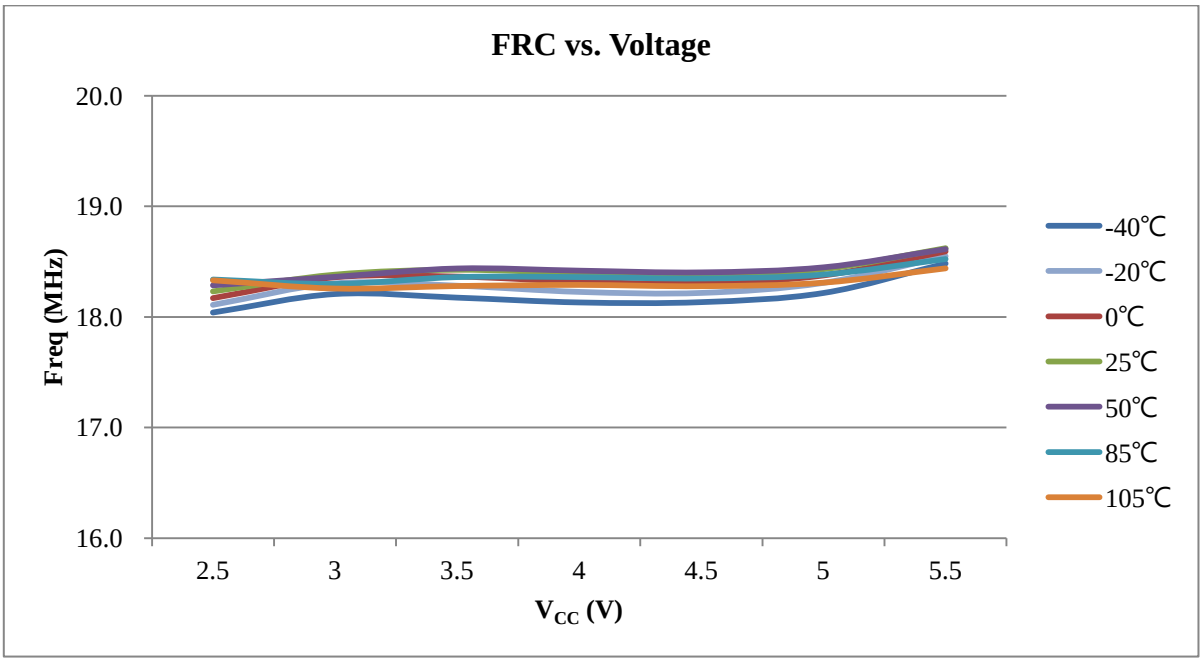
Parameter	Conditions	Min	Typ	Max	Unit
Conversion Current	V_{CC}=5.0V	–	2.5	–	mA

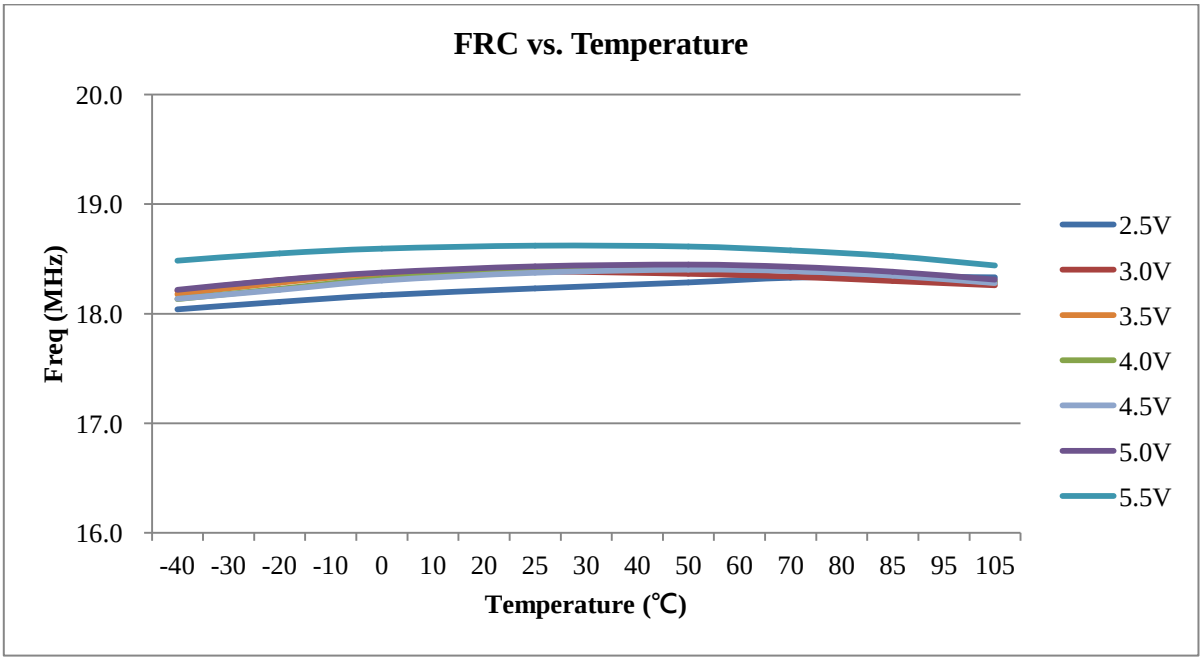
9. EEPROM Characteristics

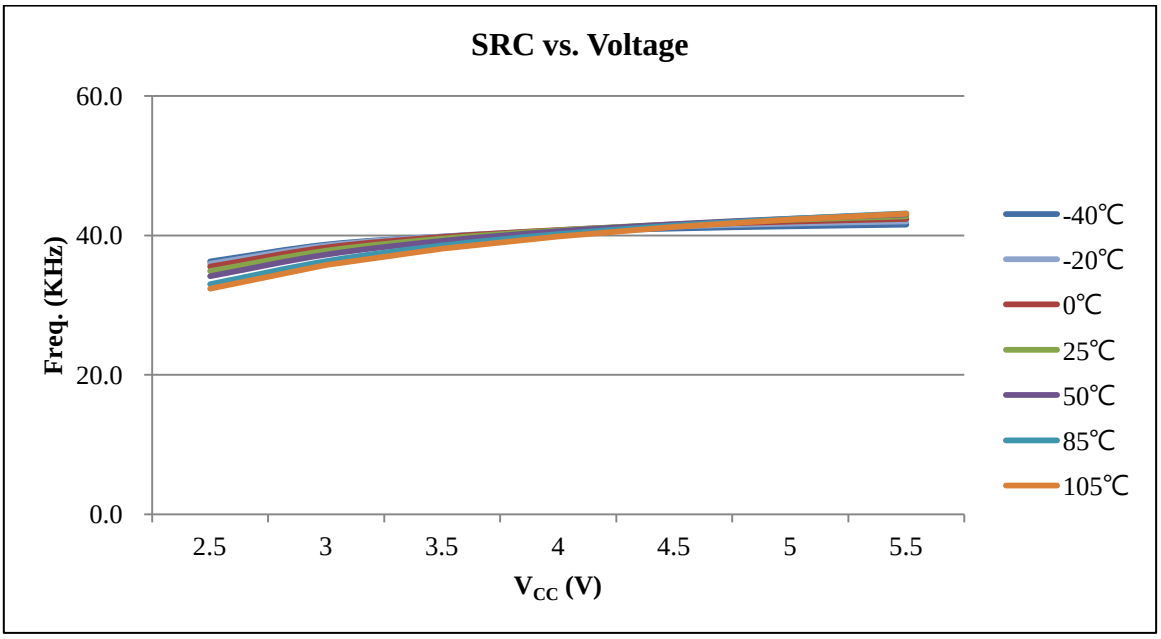
Parameter	Conditions	Min	Typ	Max	Unit
Write Voltage	-20°C ~ 85°C	3.5	5.0	5.5	V
	0°C ~ 105°C	4.5	5.0	5.5	
Write Endurance*	V_{CC} = 5V, -20°C	30K	–	–	cycles
	V_{CC} = 5V, -10°C	50K	–	–	
	V_{CC} = 3.5~5V, 85°C	50K	–	–	
	V_{CC} = 4.5 V, 0°C~105°C	50K	–	–	

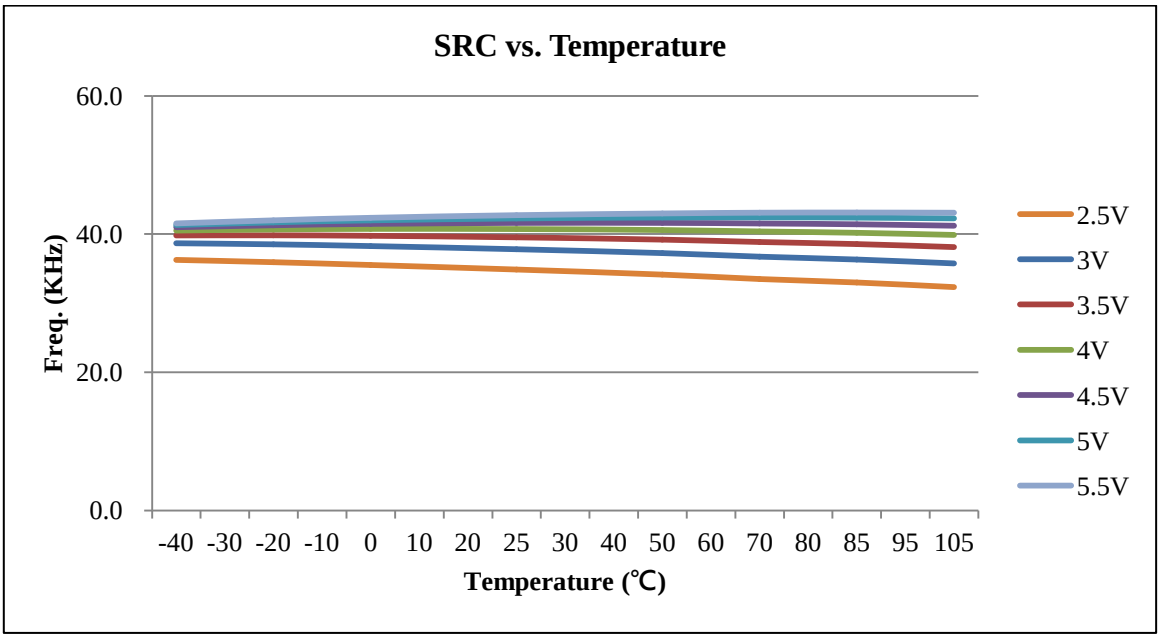
Note: *The value of this parameter is based on the characteristics of tested samples.*

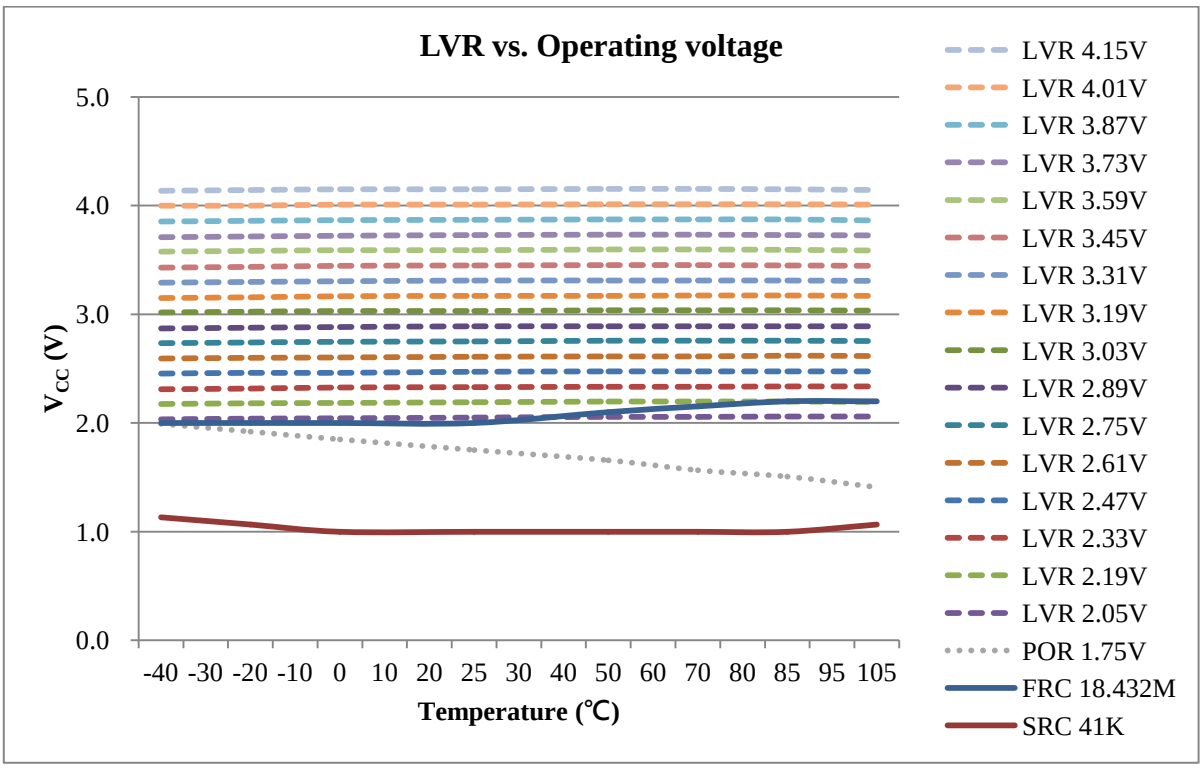
10. Characteristic Graphs



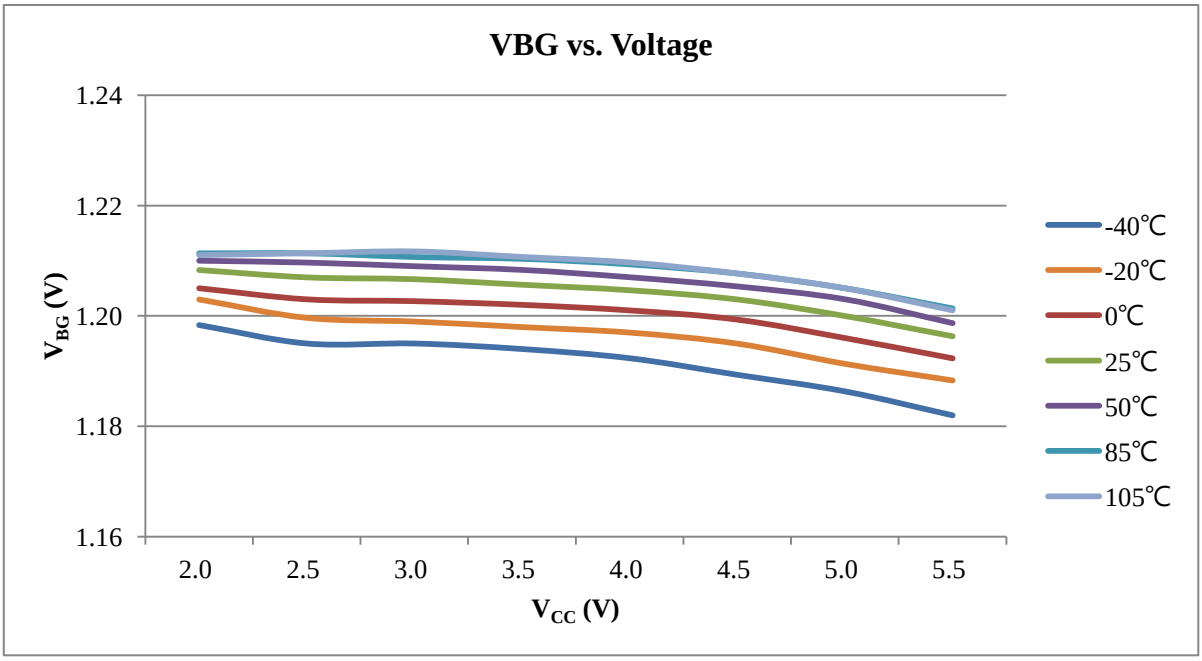



SRC vs. Voltage
60.0
40.0
20.0
0.0
Freq. (KHz)
2.5
3
3.5
4
4.5
5
5.5
VCC (V)
-40℃
-20℃
0℃
25℃
50℃
85℃
105℃


SRC vs. Temperature
60.0
40.0
20.0
0.0
Freq. (KHz)
-40 -30 -20 -10 0 10 20 25 30 40 50 60 70 80 85 95 105
Temperature (℃)
2.5V
3V
3.5V
4V
4.5V
5V
5.5V



Note: *POR: Power on reset. VCC should greater than POR when power on. Due to the variation of the manufacturing process, the POR value will be slightly different between different chips.*



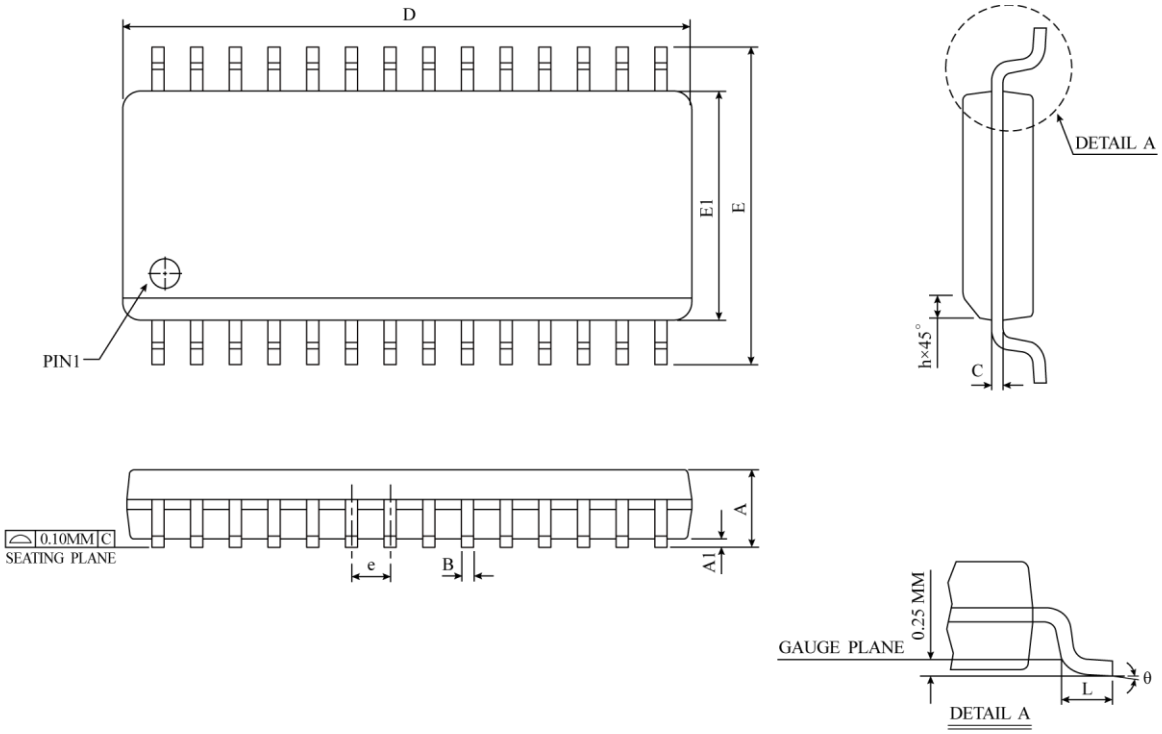
Package and Dice Information

Please note that the package information provided is for reference only. Since this information is frequently updated, users can contact Sales to consult the latest package information and stocks.

Ordering information

Ordering number	Package
TM52F4974-MTP	Wafer/Dice blank chip
TM52F4974-COD	Wafer/Dice with code
TM52F49745S-MTP-23	SOP 28-pin (300 mil)
TM52F49745E-MTP-29	SSOP 28-pin (150 mil)
TM52F49743S-MTP-21	SOP 20-pin (300 mil)
TM52F49742S-MTP-16	SOP 16-pin (150 mil)

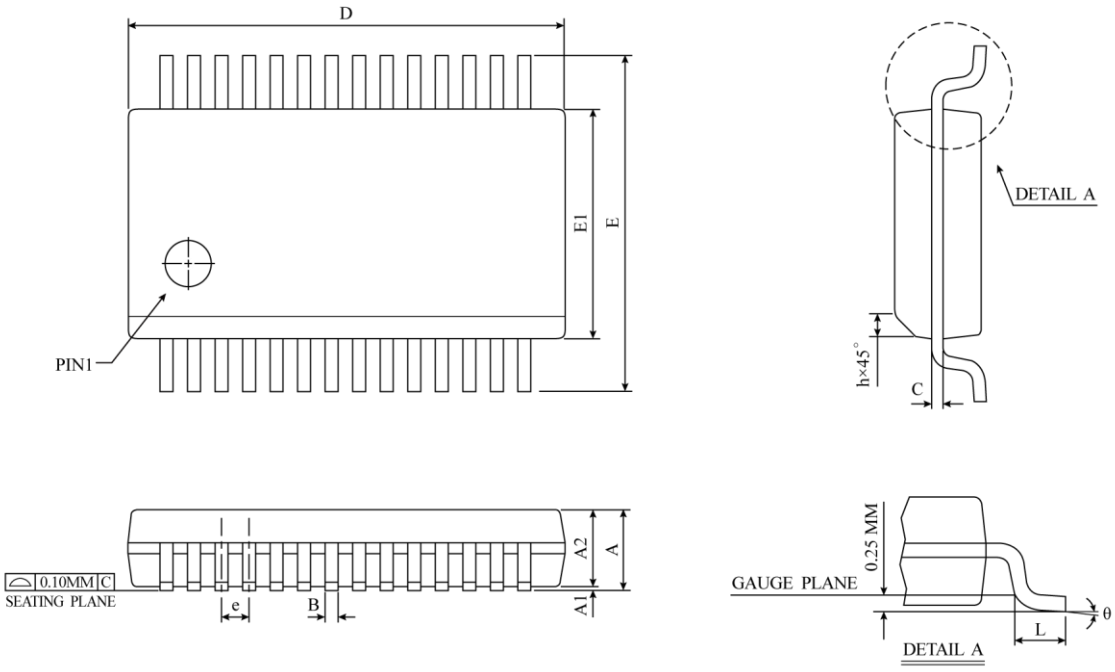
SOP-28 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	17.70	17.90	18.10	0.6969	0.7047	0.7125
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AE)					

⚠ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

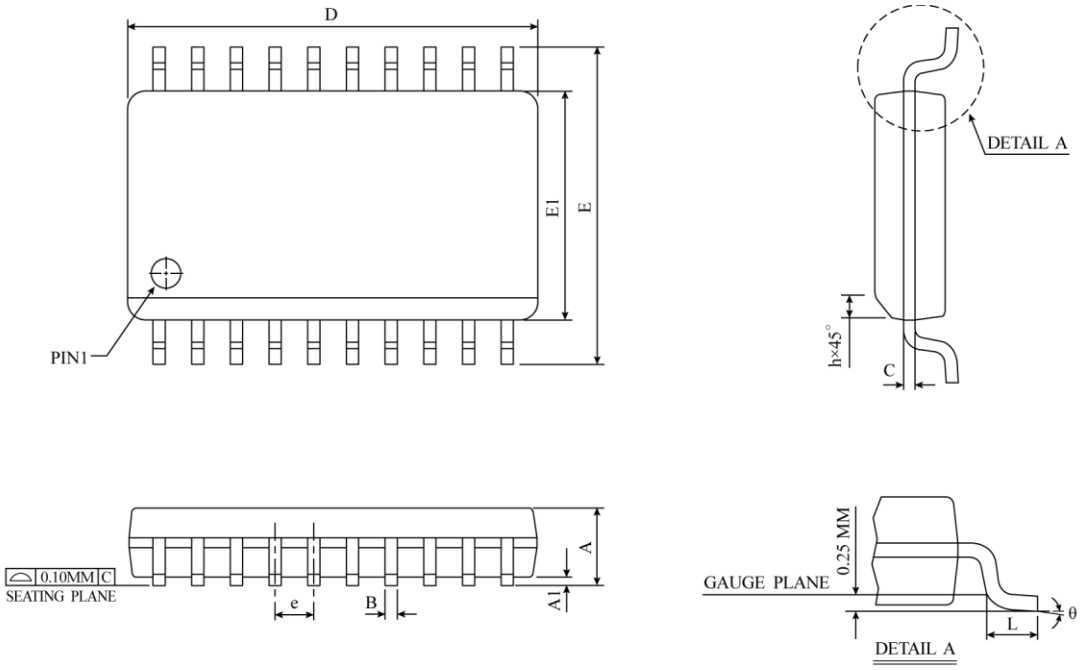
SSOP-28 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.65	1.80	0.06	0.06	0.07
A1	0.102	0.176	0.249	0.004	0.007	0.010
A2	1.40	1.475	1.55	0.06	0.06	0.06
B	0.20	0.25	0.30	0.01	0.01	0.01
C	0.2TYP			0.008TYP		
e	0.635TYP			0.025TYP		
D	9.804	9.881	9.957	0.386	0.389	0.392
E	5.842	6.020	6.198	0.230	0.237	0.244
E1	3.86	3.929	3.998	0.152	0.155	0.157
L	0.406	0.648	0.889	0.016	0.026	0.035
θ	0°	4°	8°	0°	4°	8°
JEDEC	M0-137(AF)					

*NOTES：DIMENSION “D” DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE.

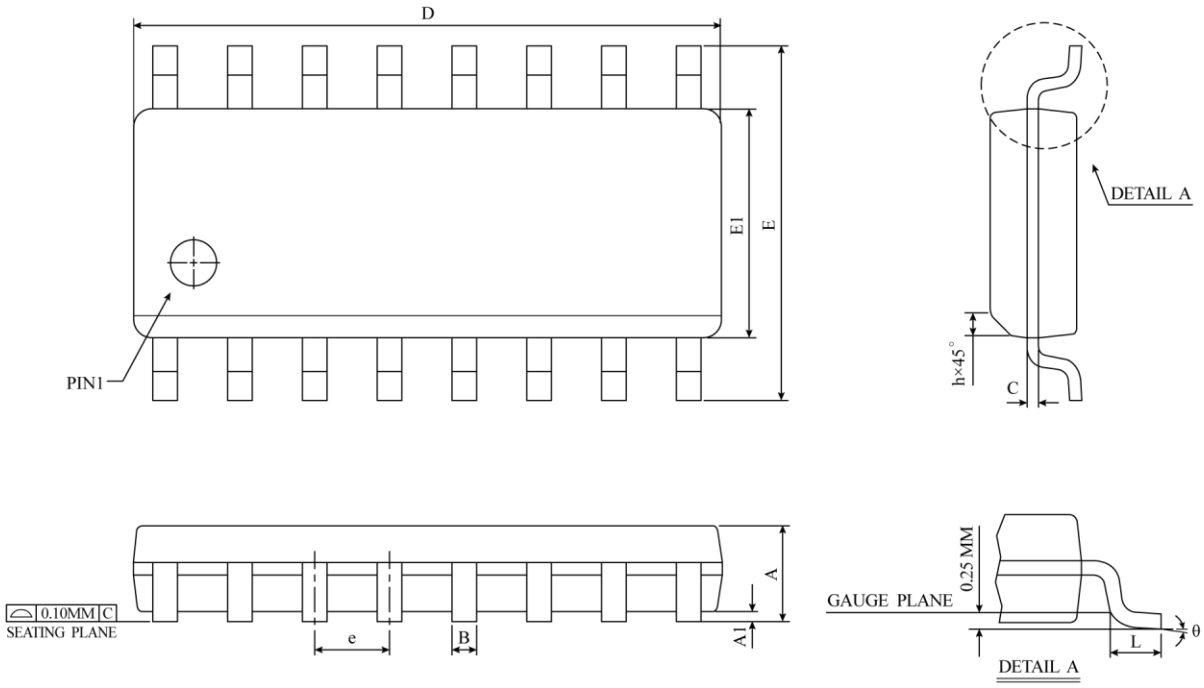
SOP-20 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	12.60	12.80	13.00	0.4961	0.5040	0.5118
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AC)					

△ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

SOP-16 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	9.80	9.90	10.00	0.3859	0.3898	0.3937
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AC)					

⚠ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.