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TM8727

with LCD Driver

User Manual

Rev 1.4

AMENDMENT HISTORY

Version	Date	Description
V1.0	Aug, 2004	New release
V1.1	Sep, 2006	Modify the contents in “PAD COORDINATE” table.
V1.2	Mar, 2011	Modify TMR2 to TMR1.
V1.3	Dec, 2011	Add Ordering Information table.
V1.4	Dec, 2016	Modify Segment Driver Output Characteristics Voh1d,Voh1e Value

CONTENTS

1. GENERAL DESCRIPTION

1.1 GENERAL DESCRIPTION

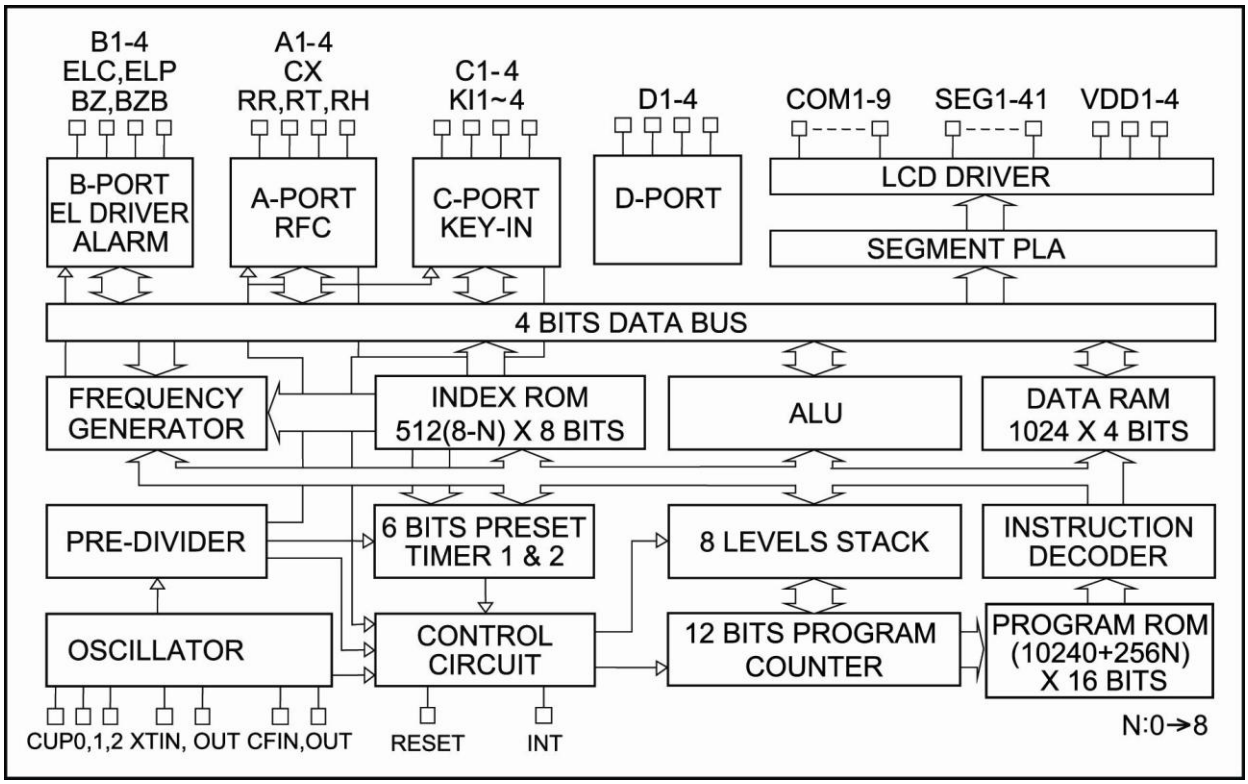
The TM8727 is an embedded high-performance 4-bit microcomputer with LCD driver. It contains all of the following functions in a single chip: 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock operation, Resistance to Frequency Converter (RFC), EL panel driver, LCD driver, look-up table, watchdog timer and key matrix scanning circuitry.

1.2 FEATURES

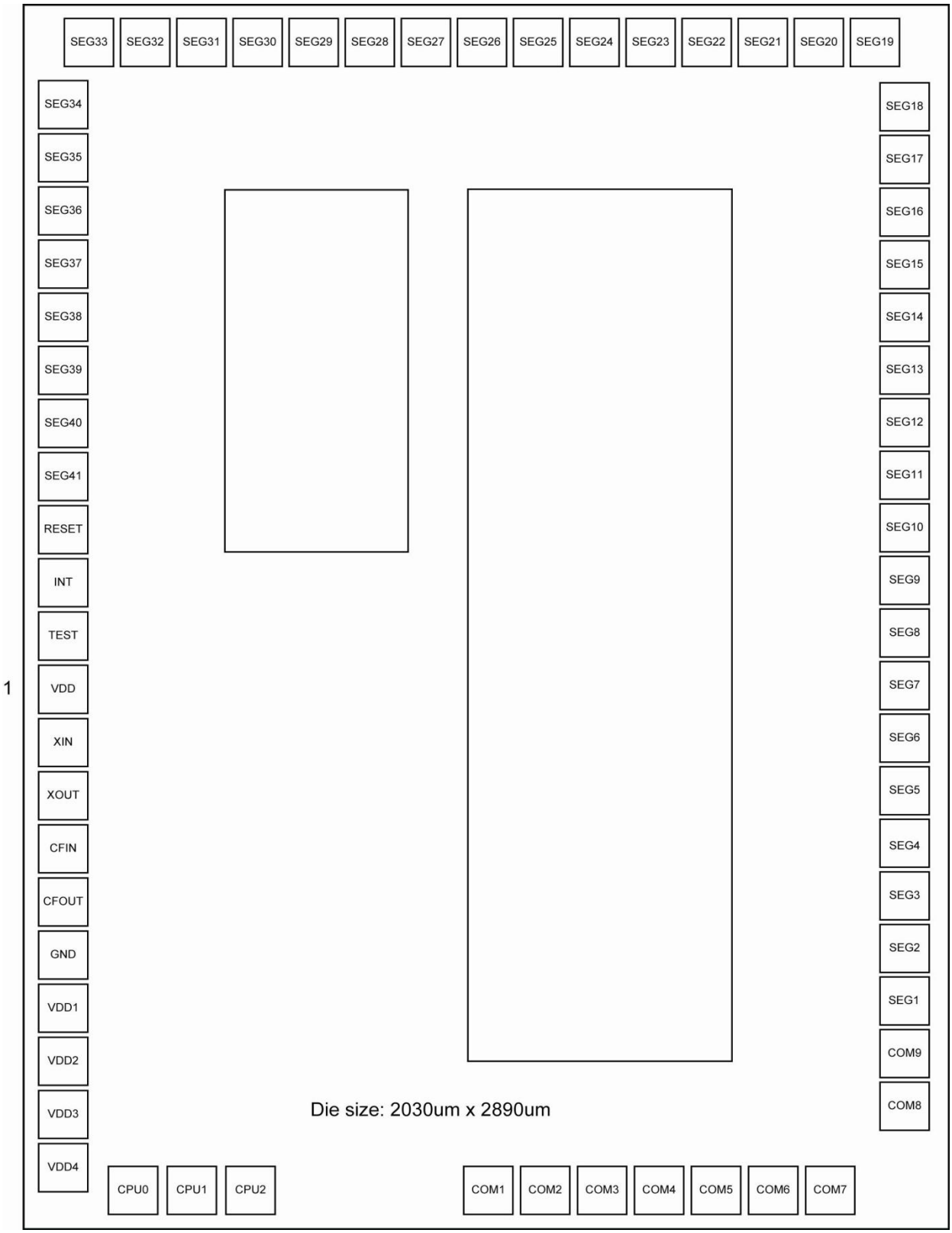
1. Low power dissipation.
2. Powerful instruction set (178 instructions).
   - Binary addition, subtraction, BCD adjusts, logical operation in direct and index addressing mode.
   - Single-bit manipulation (set, reset, decision for branch).
   - Various conditional branches.
   - 16 working registers and manipulation.
   - Table look-up.
   - LCD driver data transfer.
3. Memory capacity.
   - ROM capacity 12288 x 16 bits.
   - Program Address X100~X1FFh reversed for Bank Convert Area.
   - RAM capacity 1024 x 4 bits.
4. LCD driver output.
   - 9 common outputs and 41 segment outputs (up to drive 369 LCD segments).
   - 1/2 Duty, 1/3 Duty, 1/4 Duty, 1/5 Duty, 1/6 Duty, 1/7 Duty, 1/8 Duty or 1/9 Duty is selected by MASK option.
   - 1/2 Bias, 1/3 Bias or 1/4 Bias is selected by MASK option.
   - Single instruction to turn off all segments.
   - COM5~9, SEG1~41 could be defined as CMOS or P_open drain type output by mask option.
5. Input/output ports.
   - Port IOA 4 pins (with internal pull-low), muxed with SEG24~SEG27.
   - Port IOB 4 pins (with internal pull-low), muxed with SEG28~SEG31.
   - Port IOC 4 pins (with internal pull-low, low-level-hold), muxed with SEG32~SEG35. IOC port has built in the input signal chattering prevention circuitry.
   - Port IOD 4 pins (with internal pull-low), muxed with SEG36 ~ SEG39. IOD port has built in the input signal chattering prevention circuitry.

6. 8-level subroutine nesting.
7. Interrupt function.
   - External factors 4 (INT pin, Port IOC, IOD & KI input).
   - Internal factors 4 (Pre-Divider, Timer1, Timer2 & RFC).
8. Built-in EL-light driver.
   - ELC, ELP (Muxed with SEG28, SEG29).
9. Built-in Alarm, clock or single tone melody generator.
   - BZB, BZ (Muxed with SEG30, SEG31).
10. Built-in resistance to frequency converter.
    - CX, RR, RT, RH (Muxed with SEG24~SEG27).
11. Built-in key matrix scanning function.
    - K1~K16 (Shared with SEG1~SEG16).
    - KI1~KI4 (Muxed with SEG32 ~ SEG35).
12. Two 6-bit programmable timers with programmable clock source.
13. Watch dog timer.
14. Built-in Voltage doubler, halver, tripler, quartic charge pump circuit.
15. Dual clock operation.
    - Slow clock oscillation can be defined as X'tal or external RC type oscillator by mask option.
    - Fast clock oscillation can be defined as 3.58 MHz ceramic resonator, internal R or external R type oscillator by mask option.
16. HALT function.
17. STOP function

1.3 BLOCK DIAGRAM



1.4 PAD DIAGRAM



The substrate of the chip should be connected to the GND.

1.5 PAD COORDINATE

No	Name	X	Y	No	Name	X	Y
1	BAK	83.00	1229.20	34	SEG12(K12)	1957.50	1913.10
2	XIN	72.50	1090.30	35	SEG13(K13)	1957.50	2040.10
3	XOUT	72.50	965.40	36	SEG14(K14)	1957.50	2167.10
4	CFIN	72.50	835.40	37	SEG15(K15)	1957.50	2294.10
5	CFOUT	72.50	699.80	38	SEG16(K16)	1957.50	2421.10
6	GND	72.50	577.80	39	SEG17	1957.50	2548.10
7	VDD1	72.50	459.80	40	SEG18	1957.50	2675.10
8	VDD2	72.50	344.80	41	SEG19	1907.50	2817.50
9	VDD3	72.50	229.80	42	SEG20	1787.50	2817.50
10	VDD4	72.50	114.80	43	SEG21	1667.50	2817.50
11	CUP0	197.50	72.50	44	SEG22	1547.50	2817.50
12	CUP1	312.50	72.50	45	SEG23	1427.50	2817.50
13	CUP2	427.50	72.50	46	SEG24/IOA1/CX	1281.00	2817.50
14	COM1	988.80	72.50	47	SEG25/IOA2/RR	1135.00	2817.50
15	COM2	1128.80	72.50	48	SEG26/IOA3/RT	989.00	2817.50
16	COM3	1268.80	72.50	49	SEG27/IOA4/RH	843.00	2817.50
17	COM4	1408.80	72.50	50	SEG28/IOB1/ELC	722.50	2817.50
18	COM5	1548.80	72.50	51	SEG29/IOB2/ELP	602.50	2817.50
19	COM6	1688.80	72.50	52	SEG30/IOB3/BZB	482.50	2817.50
20	COM7	1828.80	72.50	53	SEG31/IOB4/BZ	362.50	2817.50
21	COM8	1957.50	263.10	54	SEG32/IOC1/KI1	242.50	2817.50
22	COM9	1957.50	388.10	55	SEG33/IOC2/KI2	122.50	2817.50
23	SEG1(K1)	1957.50	516.10	56	SEG34/IOC3/KI3	72.50	2675.40
24	SEG2(K2)	1957.50	643.10	57	SEG35/IOC4/KI4	72.50	2539.40
25	SEG3(K3)	1957.50	770.10	58	SEG36/IOD1	72.50	2403.40
26	SEG4(K4)	1957.50	897.10	59	SEG37/IOD2	72.50	2267.40
27	SEG5(K5)	1957.50	1024.10	60	SEG38/IOD3	72.50	2131.40
28	SEG6(K6)	1957.50	1151.10	61	SEG39/IOD4	72.50	1995.40
29	SEG7(K7)	1957.50	1278.10	62	SEG40	72.50	1859.40
30	SEG8(K8)	1957.50	1405.10	63	SEG41	72.50	1723.40
31	SEG9(K9)	1957.50	1532.10	64	RESET	72.50	1600.70
32	SEG10(K10)	1957.50	1659.10	65	INT	72.50	1475.70
33	SEG11(K11)	1957.50	1786.10	66	TEST	72.50	1350.70

1.6 PIN DESCRIPTION

Name	I/O	Description
BAK	P	Positive Back-up voltage. When using the Li power mode, connect a 0.1u capacitor to GND.
VDD1,2,3,4	P	LCD supply voltage, and positive supply voltage. When using the Ag mode, connect positive power to VDD1. When using the Li or ExtV power mode, connect positive power to VDD2.
RESET	I	Input pin for external reset request signal, built-in internal pull-down resistor.
INT	I	Input pin for external INT request signal. • Falling edge or rising edge triggers are defined by mask option. • Internal pull-down or pull-up resistor is defined by mask option.
TEST		Test signal input pin.
CUP0,1,2	O	Switching pins for supplying LCD driving voltage to the VDD1, VDD2, VDD3 and VDD4 pins. • Connect the CUP0, CUP1 and CUP2 pins with non-polarized electrolytic capacitors when the chip is operated in the 1/2, 1/3 or 1/4 bias mode. • When there is no BIAS mode application, leave these pins open.
XIN XOUT	I O	Time based counter frequency (Clock specified, LCD alternating frequency, Alarm signal frequency) or system clock oscillation. • The use of either the 32 KHz Crystal oscillator or the external RC oscillator is defined by mask option.
CFIN CFOUT	I O	System clock oscillation for the FAST clock alone or during DUAL clock operation. • The use of either the 3.58 MHz ceramic/resonator oscillator or the external R type oscillator is defined by mask option.
COM1~9	O	Output pins for driving the common pins of the LCD panel. COM5~9 can be defined as either COMS or Open Drain type output (mask option).
SEG1-41	O	Output pins for driving the LCD panel segment.
IOA1-4	I/O	Input/Output port A (muxed with SEG24~27 by mask option).
IOB1-4	I/O	Input/Output port B (muxed with SEG28~31 by mask option).
IOC1-4	I/O	Input/Output port C (muxed with SEG32~35 by mask option).
IOD1~4	I/O	Input/Output port D (muxed with SEG36~39 by mask option).
CX RR/RT/RH	I O	1 input pin and 3 output pins for RFC application (muxed with SEG24~27 by mask option).
ELC/ELP	O	Output port for El panel driver (muxed with SEG28~29 by mask option).
BZB/BZ	O	Output port for alarm, clock or single tone melody generator (muxed with SEG30~31 by mask option).
K1~K16	O	Output port for key matrix scanning (shared with SEG1~SEG16).
KI1~4	I	Input port for key matrix scanning (muxed with SEG32~SEG35 by mask option).
GND	P	Negative supply voltage.

1.7 CHARACTERIZATION

ABSOLUTE MAXIMUM RATINGS

GND=0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD1	-0.3 to 5.5	V
	VDD2	-0.3 to 5.5	
	VDD3	-0.3 to 8.5	
	VDD4	-0.3 to 8.5	
Maximum Input Voltage	Vin	-0.3 to VDD1/2+0.3	
Maximum output Voltage	Vout1	-0.3 to VDD1/2+0.3	
	Vout2	-0.3 to VDD3+0.3	
	Vout3	-0.3 to VDD4+0.3	
Maximum Operating Temperature	Topg	-20 to +70	°C
Maximum Storage Temperature	Tstg	-40 to +125	

POWER CONSUMPTION

At Ta = –20°C to 70°C, GND=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
HALT mode	IHALT1	Only 32.768 KHz Crystal Oscillator operating, without loading. Ag mode, VDD1=1.5V, BCF = 0		2		uA
	IHALT2	Only 32.768 KHz Crystal Oscillator operating, without loading. Li mode, VDD2=3.0V, BCF = 0		2		
STOP mode	ISTOP				1	

Note: When RC oscillator function is operating, the current consumption will depend on the frequency of oscillation.

ALLOWABLE OPERATING CONDITIONS

At Ta = –20°C to 70°C, GND=0V

Name	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	VDD1		1.2	5.4	V
	VDD2		2.4	5.4	
	VDD3		2.4	8.0	
	VDD4		2.4	8.0	
Oscillator Start-Up Voltage	VDDB	Crystal Mode	1.3		
Oscillator Sustain Voltage	VDDB	Crystal Mode	1.2		
Supply Voltage	VDD1	Ag Mode	1.2	1.8	
Supply Voltage	VDD2	EXT-V, Li Mode	2.4	5.4	
Input “H” Voltage	Vih1	Ag Battery Mode	VDD1-0.7	VDD1+0.7	
Input “L” Voltage	Vil1		-0.7	0.7	
Input “H” Voltage	Vih2	Li Battery Mode	VDD2-0.7	VDD2+0.7	
Input “L” Voltage	Vil2		-0.7	0.7	
Input “H” Voltage	Vih3	OSCIN at Ag Battery Mode	0.8xVDD1	VDD1	
Input “L” Voltage	Vil3		0	0.2xVDD1	
Input “H” Voltage	Vih4	OSCIN at Li Battery Mode	0.8xVDD2	VDD2	
Input “L” Voltage	Vil4		0	0.2xVDD2	
Input “H” Voltage	Vih5	CFIN at Li Battery or EXT-V Mode	0.8xVDD2	VDD2	
Input “L” Voltage	Vil5		0	0.2xVDD2	
Input “H” Voltage	Vih6	RC Mode	0.8xVDDO	VDDO	
Input “L” Voltage	Vil6		0	0.2xVDDO	
Operating Freq	Fopg1	Crystal Mode	32		KHz
	Fopg2	RC Mode	10	1000	
	Fopg3	CF Mode	1000	3580	

ALLOWABLE OPERATING FREQUENCY

At Ta = –20°C to 70°C, GND=0V

Condition	Max. Operating Frequency
BAK=1.5V (VDD1)	800 KHz
BAK=3V (VDD2)	4 MHz

INTERNAL RC FREQUENCY RANGE

Option Mode	BAK	Min.	Typ.	Max.
250 KHz	1.5V	200 KHz	300 KHz	400 KHz
	3.0V	200 KHz	250 KHz	300 KHz
500 KHz	1.5V	400 KHz	500 KHz	600 KHz
	3.0V	400 KHz	500 KHz	600 KHz

ELECTRICAL CHARACTERISTICS

at #1: VDD1=1.2V (Ag) ;

at #2: VDD2=2.4V (Li) :

at #3: VDD2=4V (Ext-V) ;

Input Resistance

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
"L" Level Hold Tr(IOC)	Rllh1	Vi=0.2VDD1,#1	10	40	100	KΩ
	Rllh2	Vi=0.2VDD2,#2	10	40	100	
	Rllh3	Vi=0.2VDD2,#3	5	20	50	
IOC Pull-Down Tr	Rmad1	Vi=VDD1,#1	200	500	1000	
	Rmad2	Vi=VDD2,#2	200	500	1000	
	Rmad3	Vi=VDD2,#3	100	250	500	
INT Pull-up Tr	Rintu1	Vi=VDD1,#1	200	500	1000	
	Rintu2	Vi=VDD2,#2	200	500	1000	
	Rintu3	Vi=VDD2,#3	100	250	500	
INT Pull-Down Tr	Rintd1	Vi=GND,#1	200	500	1000	
	Rintd2	Vi=GND,#2	200	500	1000	
	Rintd3	Vi=GND,#3	100	250	500	
RES Pull-Down R	Rres1	Vi=GND or VDD1,#1	10	1. 40	100	
	Rres2	Vi=GND or VDD2,#2	10	40	100	
	Rres3	Vi=GND or VDD2,#3	10	40	100	

DC Output Characteristics

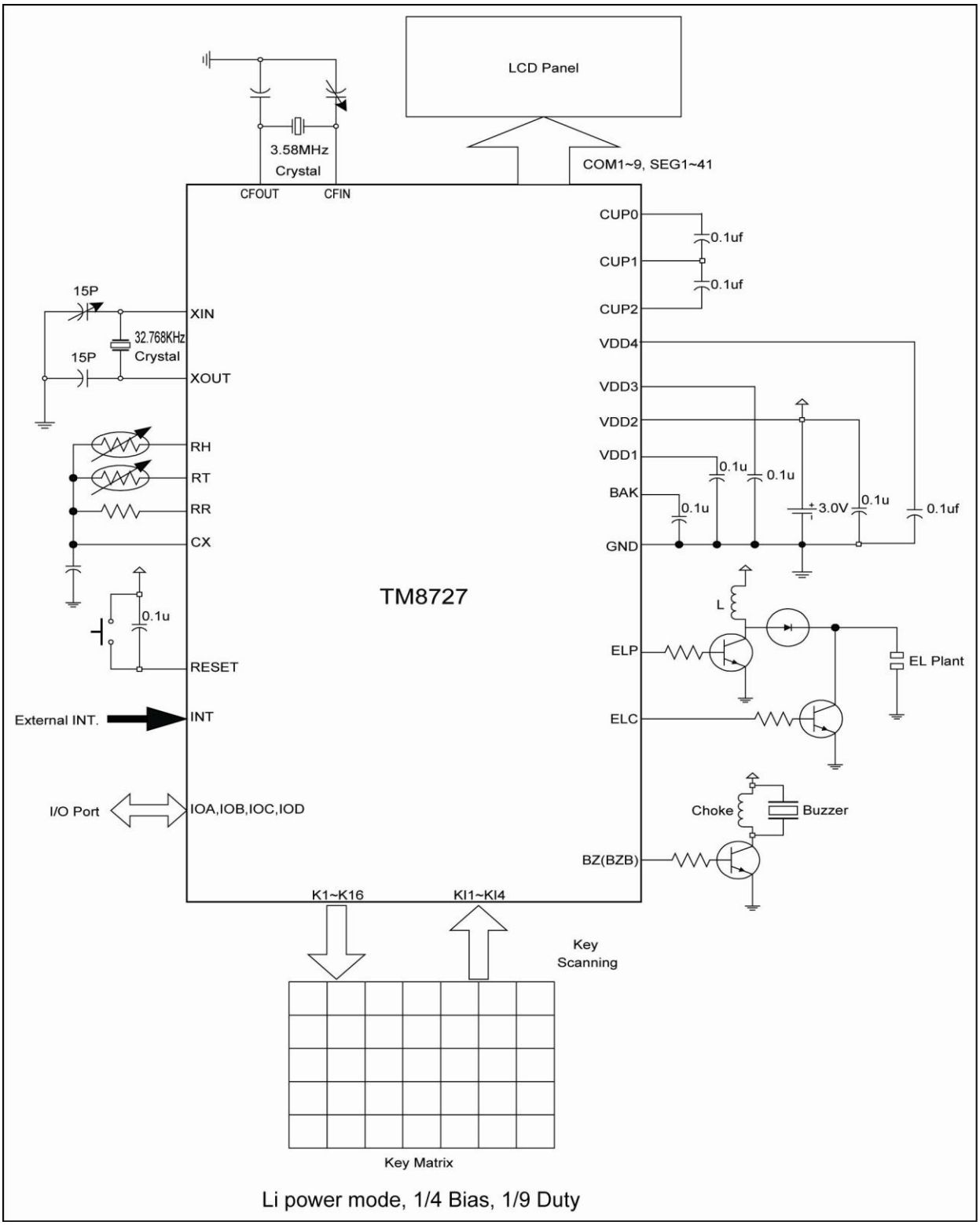
Name	Symbol	Condition	Port	Min.	Typ.	Max.	Unit
Output "H" Voltage	Voh1c	Ioh=-200 uA,#1	COM5~9 SEG1~ 41	0.8	0.9	1.0	V
	Voh2c	Ioh=-1 mA,#2		1.5	1.8	2.1	
	Voh3c	Ioh=-3 mA,#3		2.5	3.0	3.5	
Output "L" Voltage	Vol1c	Iol=400 uA,#1		0.2	0.3	0.4	
	Vol2c	Iol=2 mA,#2		0.3	0.6	0.9	
	Vol3c	Iol=6 mA,#3		0.5	1.0	1.5	

Segment Driver Output Characteristics

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit.
1/2 Bias Display Mode							
Output “H” Voltage	Voh12f	Ioh=-1 uA, #1, #2	SEG-n	2.2			V
	Voh3f	Ioh=-1 uA, #3		3.8			
Output “L” Voltage	Vol12f	Iol=1 uA, #1, #2				0.2	
	Vol3f	Iol=1 uA, #3				0.2	
Output “H” Voltage	Voh12g	Ioh=-10 uA, #1, #2	COM-n	2.2			
	Voh3g	Ioh=-10 uA, #3		3.8			
Output “M” Voltage	Vom12g	Iol/h=+/-10 uA, #1, #2		1.0		1.4	
	Vom3g	Iol/h=+/-10 uA, #3		1.8		2.2	
1/3 Bias display Mode							
Output “H” Voltage	Voh12h	Ioh=-1 uA, #1, #2	SEG-n	3.4			V
	Voh3h	Ioh=-1 uA, #3		5.8			
Output “M1” Voltage	Vom1h	Iol/h=+/-10 uA, #1, #2		1.0		1.4	
	Vom13h	Iol/h=+/-10 uA, #3		1.8		2.2	
Output “M2” Voltage	Vom22h	Iol/h=+/-10 uA, #1, #2		2.2		2.6	
	Vom23h	Iol/h=+/-10 uA, #3		3.8		4.2	
Output “L” Voltage	Vol12h	Iol=1 uA, #1, #2				0.2	
	Vol3h	Iol=1 uA, #3				0.2	
Output “H” Voltage	Voh12i	Ioh=-10 uA, #1, #2	COM-n	3.4			
	Voh3i	Ioh=-10 uA, #3		5.8			
Output “M1” Voltage	Vom12i	Iol/h=+/-10 uA, #1, #2		1.0		1.4	
	Vom13i	Iol/h=+/-10 uA, #3		1.8		2.2	
Output “M2” Voltage	Vom22i	Iol/h=+/-10 uA, #1, #2		2.2		2.6	
	Vom23i	Iol/h=+/-10 uA, #3		3.8		4.2	
Output “L” Voltage	Vol12i	Iol=10 uA, #1, #2				0.2	
	Vol3i	Iol=10 uA, #3				0.2	
1/4 Bias display Mode							
Output “H” Voltage	Voh12j	Ioh=-1 uA, #1, #2	SEG-n	4.6			V
Output “M2” Voltage	Vom22j	Iol/h=+/-10 uA, #1, #2		2.2		2.6	
Output “L” Voltage	Vol12j	Iol=1 uA, #1, #2				0.2	
Output “H” Voltage	Voh12k	Ioh=-10 uA, #1, #2	COM-n	4.6			
Output “M1” Voltage	Vom12k	Iol/h=+/-10 uA, #1, #2		1.0		1.4	
Output “M3” Voltage	Vom22k	Iol/h=+/-10 uA, #1, #2		3.4		3.8	
Output “L” Voltage	Vol12k	Iol=10 uA, #1, #2				0.2	

1.8 TYPICAL APPLICATION CIRCUIT

This application circuit is simply an example, and is not guaranteed to work.



2. TM8727 INTERNAL SYSTEM ARCHITECTURE

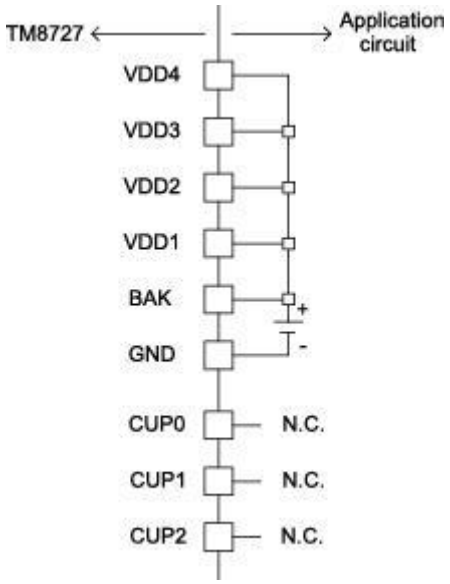
2.1 POWER SUPPLY

TM8727 can operate with 3 types voltage supplies, Ag, Li, and EXT-V, all of these operating types are defined by the mask option. The power supply circuitry also generates the necessary voltage level for driving the LCD panel with a different bias. Shown below are the connection diagrams for 1/2 bias, 1/3 bias, 1/4 bias, and no bias applications.

2.1.1 Ag BATTERY POWER SUPPLY

Operating voltage range: 1.2V ~ 1.8V.

2.1.1.1 NO LCD BIAS NEED AT Ag BATTERY POWER SUPPLY



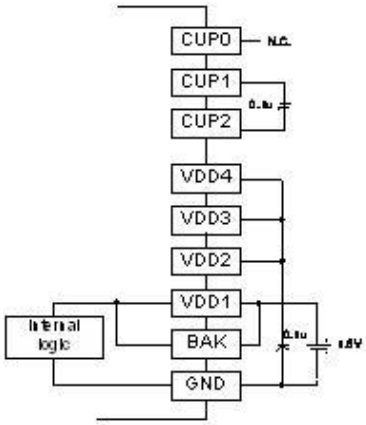
MASK OPTION table:

Mask Option name	Selected item
POWER SOURCE	(3) 1.5V BATTERY
BIAS	(1) NO BIAS

Note:

1. **The input/output ports operate between GND and VDD1.**
2. **The backup flag (BCF) is set in the initial clear mode. When the backup flag is set, the oscillator circuit uses a larger driving force to operate and the oscillation conditions are improved, but the operating current is also increased. Therefore, the backup flag should be reset unless otherwise required. *For information on the backup flag, refer to 3-5*.**

2.1.1.2 1/2 BIAS & STATIC AT Ag BATTERY POWER SUPPLY



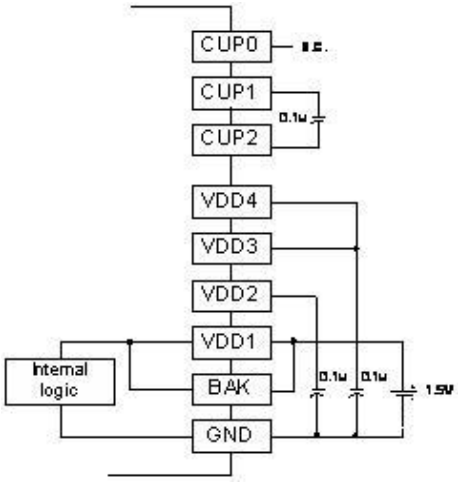
MASK OPTION table:

Mask Option name	Selected item
POWER SOURCE	(3) 1.5V BATTERY
BIAS	(2) 1/2 BIAS

Note:

1. **The input/output ports operate between GND and VDD1.**
2. **The backup flag (BCF) is set in the initial clear mode. When the backup flag is set, the oscillator circuit uses a larger driving force to operate and the oscillation conditions are improved, but the operating current is also increased. Therefore, the backup flag should be reset unless otherwise required. *For information on the backup flag, refer to 3-5.***

2.1.1.3 1/3 BIAS AT Ag BATTERY POWER SUPPLY



MASK OPTION table:

Mask Option name	Selected item
POWER SOURCE	(3) 1.5V BATTERY
BIAS	(3) 1/3 BIAS

Note:

1. **The input/output ports operate between GND and VDD1.**
2. **The backup flag (BCF) is set in the initial clear mode. When the backup flag is set, the oscillator circuit uses a larger driving force to operate and the oscillation conditions are improved, but the operating current is also increased. Therefore, the backup flag should be reset unless otherwise required. *For information on the backup flag, refer to 3-5.***

2.1.1.4 1/4 BIAS AT Ag BATTERY POWER SUPPLY

It is recommanded that the option "LCD reset OFF" is not used in this power mode, as the LCD segments cannot be turned off completely in the RESET cycle.

MASK OPTION table:

Mask Option name	Selected item
POWER SOURCE	(3) 1.5V BATTERY
BIAS	(4) 1/4 BIAS

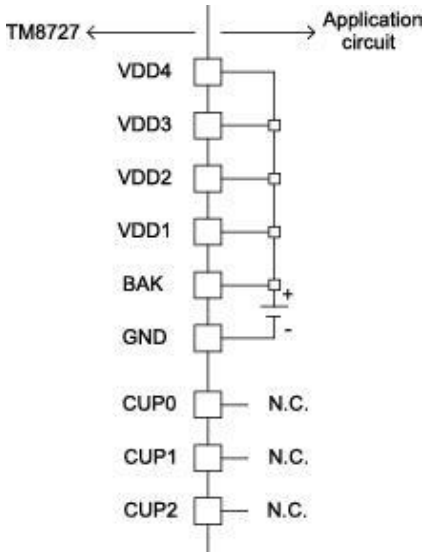
Note:

1. **The input/output ports operate between GND and VDD1.**
2. **The backup flag (BCF) is set in the initial clear mode. When the backup flag is set, the oscillator circuit uses a larger driving force to operate and the oscillation conditions are improved, but the operating current is also increased. Therefore, the backup flag should be reset unless otherwise required. *For information on the backup flag, refer to 3-5.***

2.1.2 Li BATTERY POWER SUPPLY

Operating voltage range: 2.4V ~ 3.6V.

2.1.2.1 NO BIAS AT Li BATTERY POWER SUPPLY



MASK OPTION table:

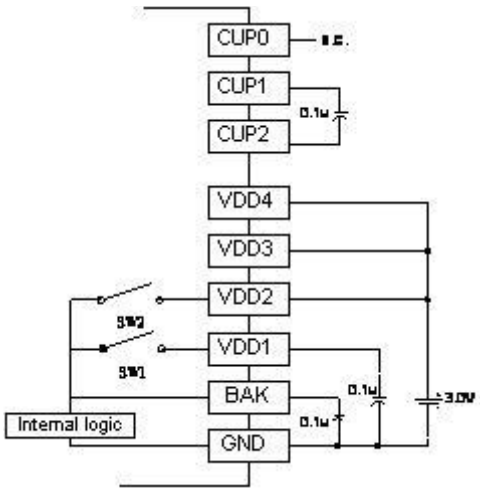
Mask Option name	Selected item
POWER SOURCE	(2) 3V BATTERY OR HIGHER
BIAS	(1) NO BIAS

Note: The input/output ports operate between GND and VDD2.

2.1.2.2 1/2 BIAS AT Li BATTERY POWER SUPPLY

The backup flag (BCF) must be reset after the operation of the halver circuit is fully stabilized and a voltage of approximately 1/2 * VDD2 appears on the VDD1 pin.

Backup flag(BCF)	SW1	SW2
BCF=0	ON	OFF
BCF=1	OFF	ON



MASK OPTION table:

Mask Option name	Selected item
POWER SOURCE	(2) 3V BATTERY OR HIGHER
BIAS	(2) 1/2 BIAS

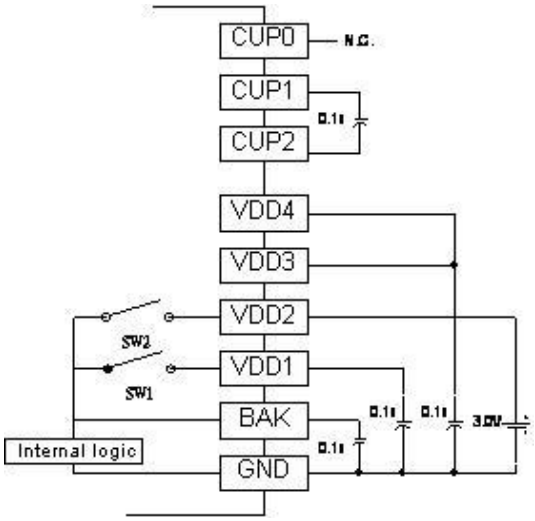
Note:

1. **The input/output ports operate between GND and VDD2.**
2. **The backup flag (BCF) is set in the initial clear mode. When the backup flag is set, the internal logic operated on VDD2 and the oscillator circuit becomes large in driver size. When the backup flag is set, the operating current is increased. Therefore, the backup flag should be reset unless otherwise required. *For information on the backup flag, refer to 3-5.***
3. **The VDD1 level (≈1/2 * VDD2) at the off-state of SW1 is used as an intermediate voltage level for the LCD driver.**

2.1.2.3 1/3 BIAS AT Li BATTERY POWER SUPPLY

The backup flag (BCF) must be reset after the operation of the halver circuit is fully stabilized and a voltage of approximately 1/2 * VDD2 appears on the VDD1 pin.

Backup flag(BCF)	SW1	SW2
BCF=0	ON	OFF
BCF=1	OFF	ON



MASK OPTION table:

Mask Option name	Selected item
POWER SOURCE	(2) 3V BATTERY OR HIGHER
BIAS	(3) 1/3 BIAS

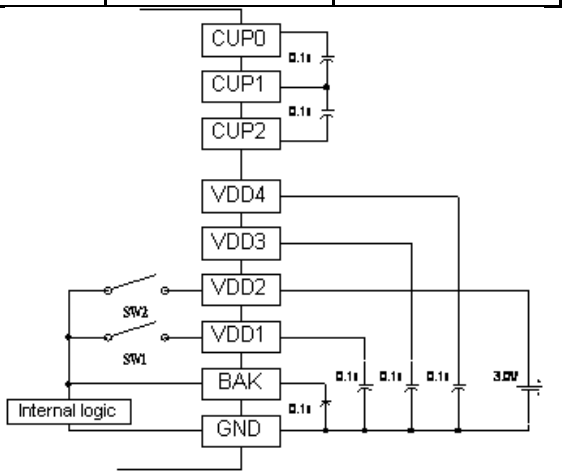
Note:

1. **The input/output ports operate between GND and VDD2.**
2. **The backup flag (BCF) is set in the initial clear mode. When the backup flag is set, the internal logic operated on VDD2 and the oscillator circuit becomes large in driver size. When the backup flag is set, the operating current is increased. Therefore, the backup flag should be reset unless otherwise required. *For information on the backup flag, refer to 3-5.***
3. **The VDD1 level (≈□ 1/2 * VDD) at the offstate of SW1 is used as an intermediate voltage level for LCD driver.**

2.1.2.4 1/4 BIAS AT Li BATTERY POWER SUPPLY

The backup flag (BCF) must be reset after the operation of the halver circuit is fully stabilized and a voltage of approximately 1/2 * VDD2 appears on the VDD1 pin.

Backup flag(BCF)	SW1	SW2
BCF=0	ON	OFF
BCF=1	OFF	ON



It is recommanded that the option "LCD reset OFF" is not used in this power mode, as the LCD segments cannot be turned off completely in the RESET cycle.

MASK OPTION table:

Mask Option name	Selected item
POWER SOURCE	(2) 3V BATTERY OR HIGHER
BIAS	(4) 1/4 BIAS

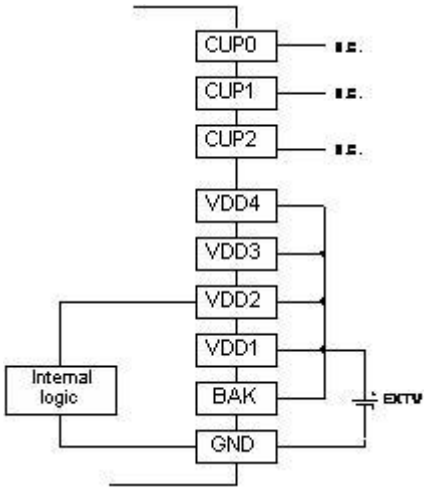
Note:

1. **The input/output ports operate between GND and VDD2.**
2. **The backup flag (BCF) is set in the initial clear mode. When the backup flag is set, the internal logic operated on VDD2 and the oscillator circuit becomes large in driver size. When the backup flag is set, the operating current is increased. Therefore, the backup flag must be reset unless otherwise required. *For information on the backup flag, refer to 3-5.***
3. **The VDD1 level (≈ 1/2 * VDD) at the offstate of SW1 is used as an intermediate voltage level for LCD driver.**

2.1.3 EXT-V POWER SUPPLY

Operating voltage range: 3.6V ~ 5.4V.

2.1.3.1 NO BIAS AT EXT-V BATTERY POWER SUPPLY



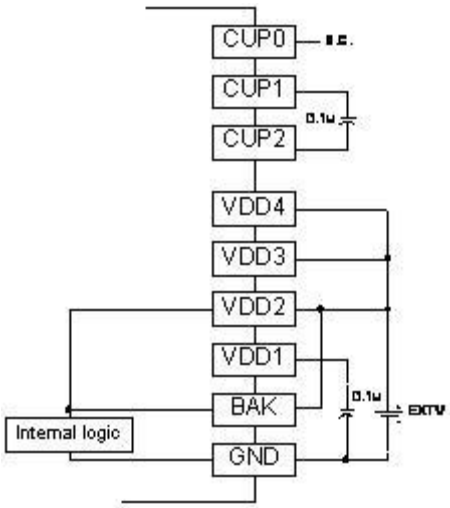
MASK OPTION table:

Mask Option name	Selected item
POWER SOURCE	(1) EXT-V
BIAS	(1) NO BIAS

Note:

1. The input/output ports operate between GND and VDD2.
2. At the initial clear mode the backup flag (BCF) is reset.
3. At the backup flag set mode the operating current is increased.

2.1.3.2 1/2 BIAS AT EXT-V POWER SUPPLY



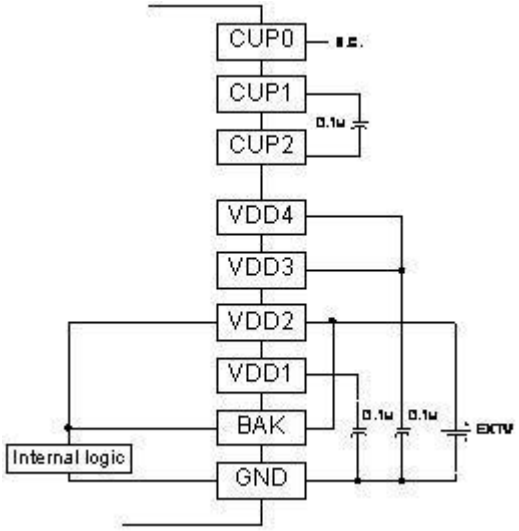
MASK OPTION table:

Mask Option name	Selected item
POWER SOURCE	(1) EXT-V
BIAS	(2) 1/2 BIAS

Note:

1. **The input/output ports operate between GND and VDD2.**
2. **At the initial clear mode the backup flag (BCF) is reset.**
3. **At the backup flag set mode the operating current is increased. Therefore, the backup flag must be reset unless otherwise required.**

2.1.3.3 1/3 BIAS AT EXT-V POWER SUPPLY



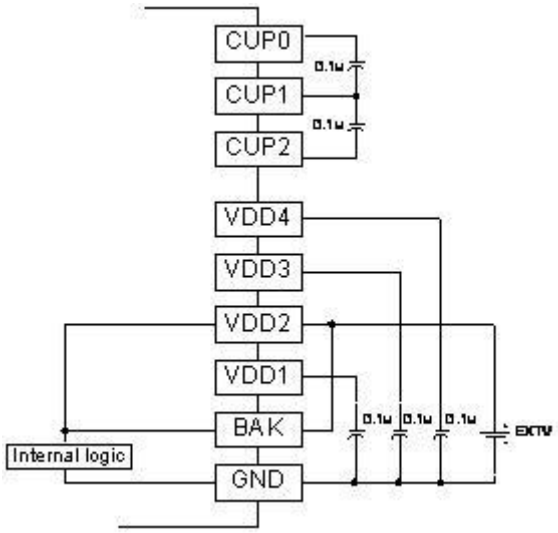
MASK OPTION table:

Mask Option name	Selected item
POWER SOURCE	(1) EXT-V
BIAS	(3) 1/3 BIAS

Note:

1. **The input/output ports operate between GND and VDD2.**
2. **At the initial clear mode the backup flag (BCF) is reset.**
3. **At the backup flag set mode the operating current is increased. Therefore, the backup flag must be reset unless otherwise required.**

2.1.3.4 1/4 BIAS AT EXT-V POWER SUPPLY



MASK OPTION table:

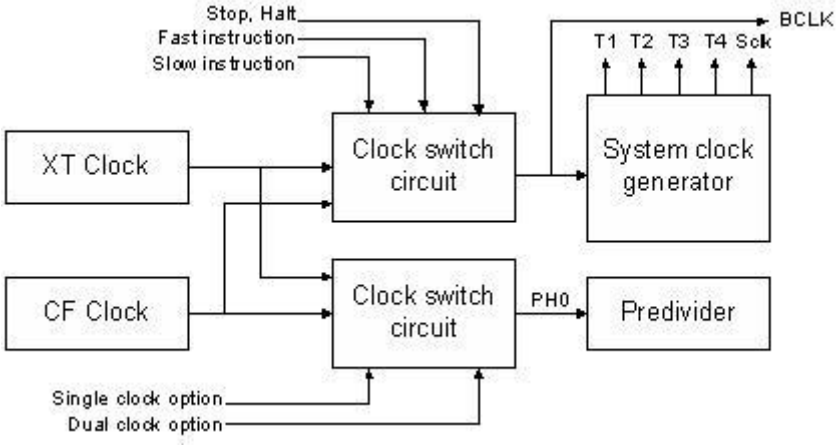
Mask Option name	Selected item
POWER SOURCE	(1) EXT-V
BIAS	(4) 1/4 BIAS

Note:

1. **The input/output ports operate between GND and VDD2.**
2. **At the initial clear mode the backup flag (BCF) is reset.**
3. **At the backup flag set mode the operating current is increased. Therefore, the backup flag must be reset unless otherwise required.**

2.2 SYSTEM CLOCK

The XT clock (slow clock oscillator) and CF clock (fast clock oscillator) compose the clock oscillation circuitry and the block diagram is shown below.



The system clock generator provides the necessary clocks for execution of instruction. The pre-divider generates several clocks with different frequencies for the LCD driver, frequency generator, etc... to use.

The following table shows the clock sources of system clock generators and pre-divider under different conditions.

	PH0	BCLK
Slow clock only option	XT clock	XT clock
fast clock only option	CF clock	CF clock
Initial state (dual clock option)	XT clock	XT clock
Halt mode (dual clock option)	XT clock	XT clock
Slow mode (dual clock option)	XT clock	XT clock
Fast mode (dual clock option)	XT clock	CF clock

2.2.1 CONNECTION DIAGRAM OF SLOW CLOCK OSCILLATOR (XT CLOCK)

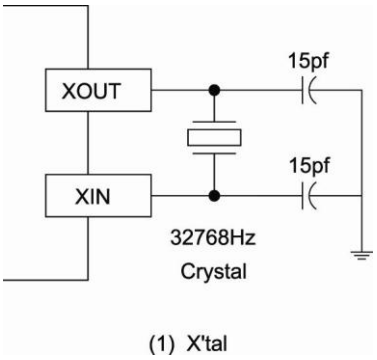
This clock oscillation circuitry provides the lower-speed clock to the system clock generator, pre-divider, timer, chattering prevention of IO port and LCD circuitry. This oscillator will be disabled when the fast clock only option is selected by mask option, otherwise it will be active all the time after the initial reset. In stop mode, the oscillator will be stopped.

There are 2 type oscillators which can be used in slow clock oscillators, select with the mask option.

2.2.1.1 External 32.768 KHz Crystal Oscillator

MASK OPTION table:

Mask Option name	Selected item
SLOW CLOCK TYPE FOR SLOW ONLY OR DUAL	(1) X’tal



(1) X'tal

When backup flag (BCF) is set to 1, the oscillator operates with an extra buffer in parallel in order to shorten the oscillator start-up time. This increases the power consumption. Therefore, the backup flag should be reset unless otherwise required.

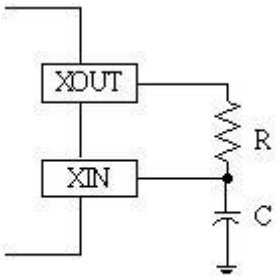
The following table shows the power consumption of Crystal oscillator under different conditions:

	Ag power option	Li power option	EXT-V option
BCF=1	Increased	Increased	Increased
BCF=0	Normal	Normal	Increased
Initial reset	Increased	Increased	Increased
After reset	Normal	Normal	Increased

2.2.1.2 External RC oscillator

MASK OPTION table:

Mask Option name	Selected item
SLOW CLOCK TYPE FOR SLOW ONLY OR DUAL	(2) RC



(2) RC

2.2.2 CONNECTION DIAGRAM OF FAST CLOCK OSCILLATOR (CF CLOCK)

The CF clock is a multiple type oscillator (mask option) which provides a faster clock source to system. In single clock operation (fast only), this oscillator will provide the clock to the system clock generator,

pre-divider, timer, I/O port chattering prevention clock and LCD circuitry. In dual clock operation, CF clock provides the clock to the system clock generator only.

When the dual clock option is selected by mask option, this oscillator will be inactive most of the time except when the FAST instruction is executed. After the FAST instruction is executed, the clock source (BCLK) of the system clock generator will be switched to CF clock, and the clock source for other functions will continue to come from XT clock.

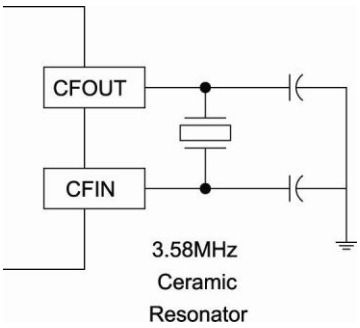
Halt mode, stop mode or SLOW instruction execution will stop this oscillator, after which the system clock (BCLK) will be switched to XT clock.

There are 3 type oscillators that can be used in the slow clock oscillator, select by mask option.

2.2.2.1 External 3.58 MHz Ceramic Resonator Oscillator

MASK OPTION table:

Mask Option name	Selected item
FAST CLOCK TYPE FOR FAST ONLY OR DUAL	(4) 3.58 MHz Ceramic Resonator



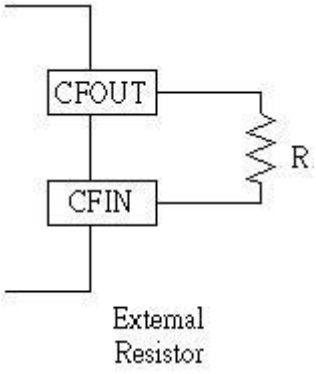
Note:

1. **Don't use 3.58 MHz Ceramic Resonator as the oscillator when the Ag battery option is used.**
2. **When the program has to reset the BCF flag to 0 in Li battery power mode, don't use a 3.58 MHz Ceramic Resonator as the oscillator.**

2.2.2.2 RC oscillator with External Resistor

MASK OPTION table:

Mask Option name	Selected item
FAST CLOCK TYPE FOR FAST ONLY OR DUAL	(3) EXTERNAL RESISTOR



2.2.2.3 Internal RC Oscillator

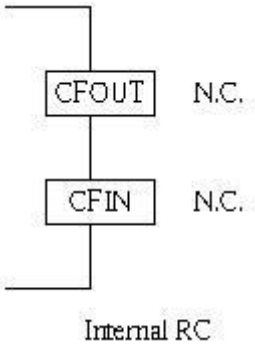
MASK OPTION table:

For 250 KHz output frequency:

Mask Option name	Selected item
FAST CLOCK TYPE FOR FAST ONLY OR DUAL	(1) INTERNAL RESISTOR FOR 250 KHz

For 250 KHz output frequency:

Mask Option name	Selected item
FAST CLOCK TYPE FOR FAST ONLY OR DUAL	(2) INTERNAL RESISTOR FOR 500 KHz



FREQUENCY RANGE OF INTERNAL RC OSCILLATOR:

Option Mode	BAK	Min.	Typ.	Max.
250 KHz	1.5V	200 KHz	300 KHz	400 KHz
	3.0V	200 KHz	250 KHz	300 KHz
500 KHz	1.5V	400 KHz	500 KHz	600 KHz
	3.0V	400 KHz	500 KHz	600 KHz

2.2.3 COMBINATION OF THE CLOCK SOURCES

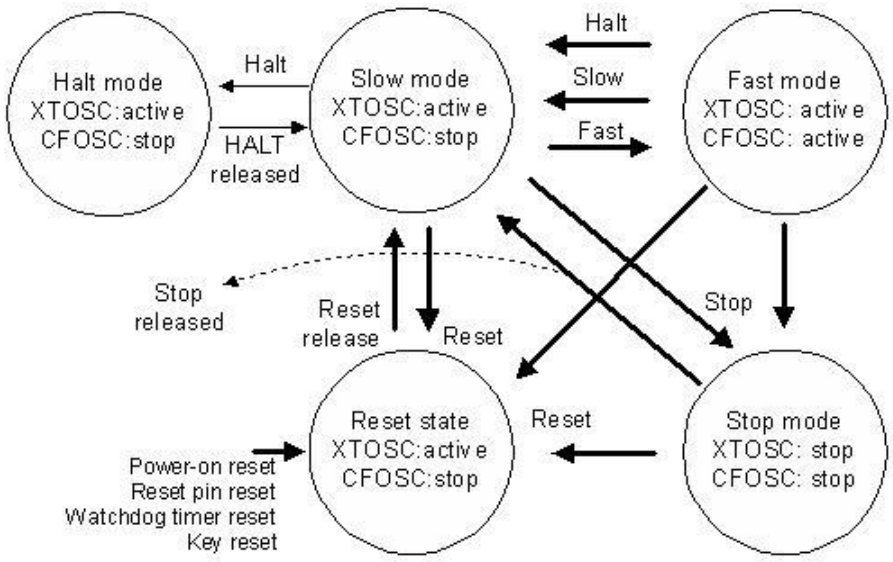
There are three combinations of clock sources that can be selected by mask option.

2.2.3.1 Dual Clock

MASK OPTION table:

Mask Option name	Selected item
CLOCK SOURCE	(3) DUAL

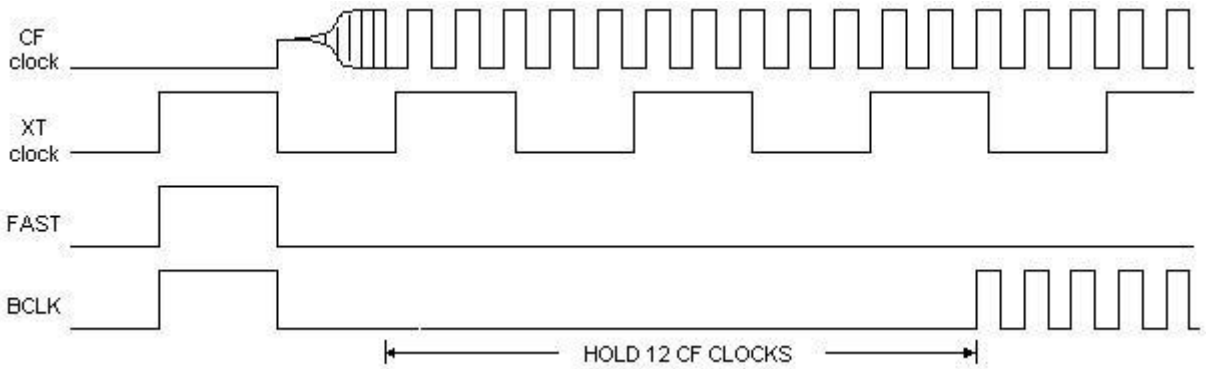
The operation of the dual clock option is shown in the following figure.



When this option is selected by mask option, the clock source (BCLK) of system clock generator will switch between the XT clock and the CF clock according to the user's program. When the halt and stop instructions are executed, the clock source (BCLK) will switch to XT clock automatically.

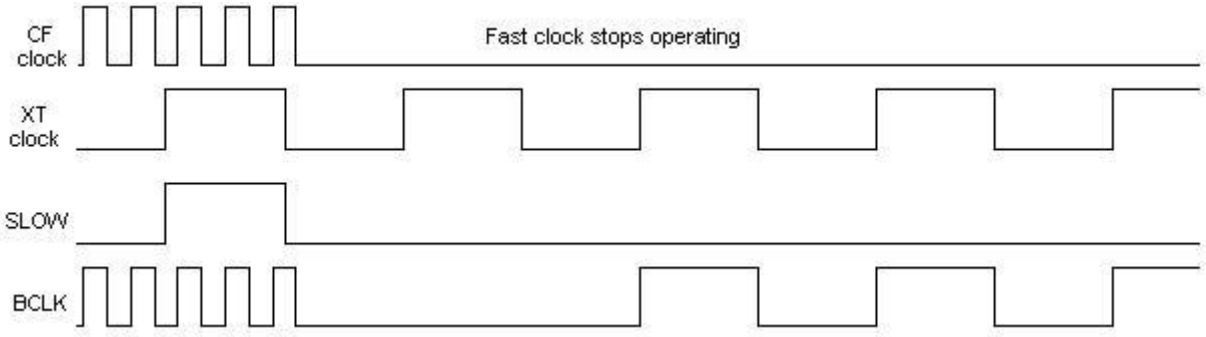
In this option, the XT clock provides the clock to the pre-divider, timer, I/O port chattering prevention and LCD circuitry.

After executing FAST instructions, the CF clock oscillator will start up and switch CF clock to BCLK, after which the system clock generator will hold 12 CF clocks. This will prevent the incorrect clock from reaching the system clock in the start-up duration of the fast clock oscillator.



This figure shows the System Clock Switching from Slow to FAST.

After executing SLOW instruction, the system clock generator will hold for 2 XT clock cycles, and then switch XT clock to BCLK.



This figure shows the System Clock Switching from FAST to Slow.

2.2.3.2 Single Clock

MASK OPTION table:

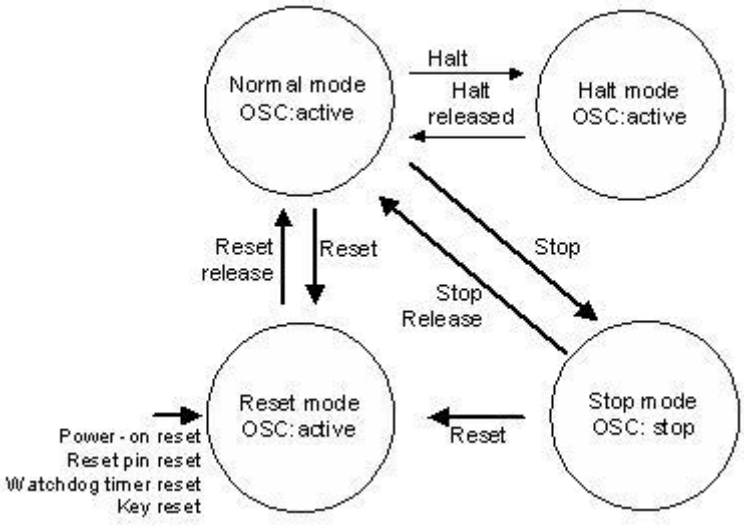
For Fast clock oscillator only

Mask Option name	Selected item
CLOCK SOURCE	(1) FAST ONLY

For slow clock oscillator only

Mask Option name	Selected item
CLOCK SOURCE	(2) SLOW ONLY

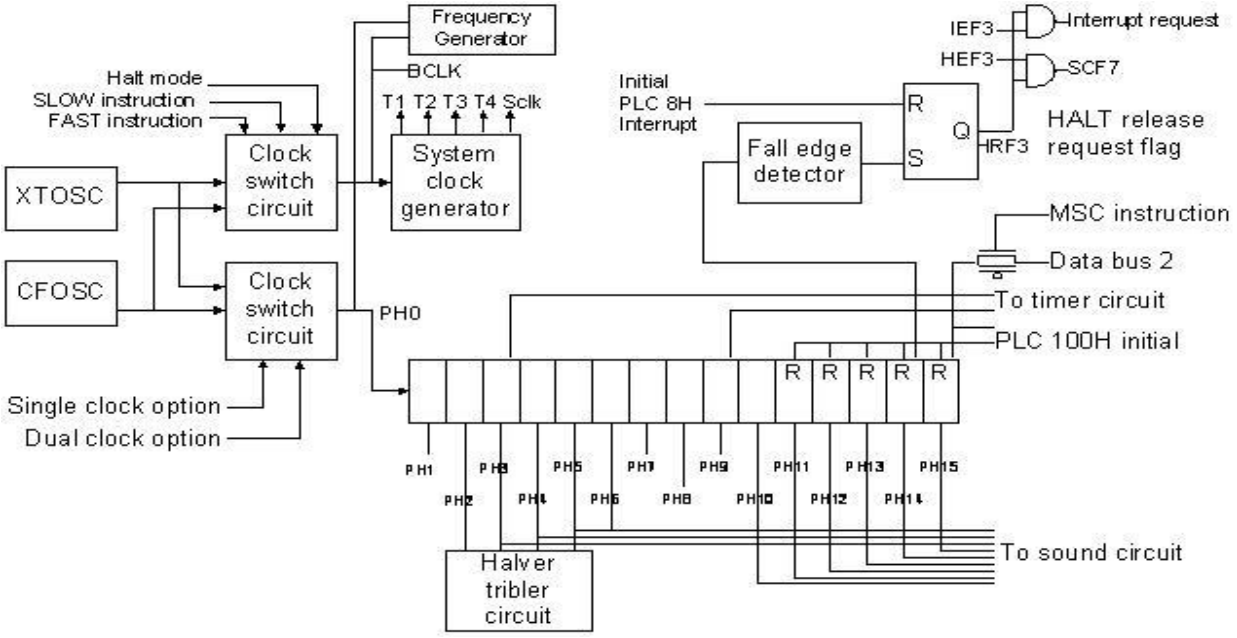
The operation of the single clock option is shown in the following figure. Either the XT or the CF clock may be selected by mask option in this mode. The FAST and SLOW instructions will perform as the NOP instruction in this option. The backup flag (BCF) will be set to 1 automatically before the program enters the stop mode.



This figure shows the State Diagram of Single Clock Option

2.2.4 PREDIVIDER

The pre-divider is a 15-stage counter that receives the clock from the output of clock switch circuitry (PH0) as input. When PH0 changes from "H" level to "L" level, the contents of this counter changes. The PH11 to PH15 of the pre-divider are reset to "0" when the PLC 100H instruction is executed or during the initial reset mode. The pre-divider delivers the signal to the halver/tripler circuit, alternating frequency for LCD display, system clock, sound generator and halt release request signal (I/O port chattering prevention clock).



This figure shows the Pre-divider and its Peripherals

The PH14 delivers the halt mode release request signal, setting the halt mode release request flag (HRF3). In this case, if the pre-divider interrupt enable mode (IEF3) is provided, the interrupt is accepted; and if the halt release enable mode (HEF3) is provided, the halt release request signal is delivered, setting the start condition flag 7 (SCF7) in status register 3 (STS3).

The clock source of the pre-divider is PH0; 4 kinds of frequencies of PH0 can be selected by mask option:

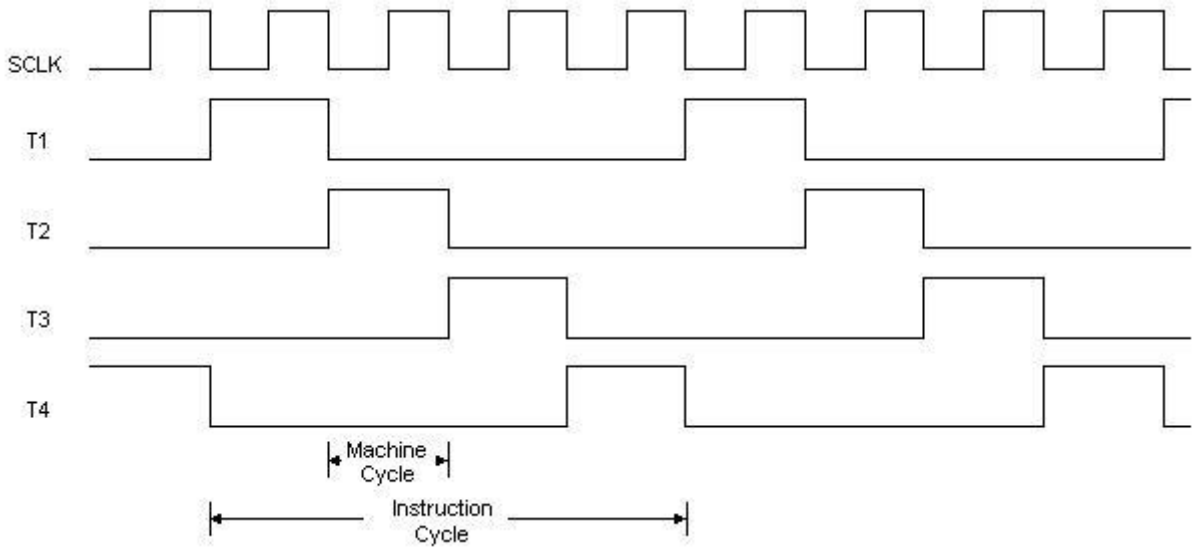
MASK OPTION table:

Mask Option name	Selected item
PH0 <-> BCLK FOR FAST ONLY	(1) PH0 = BCLK
PH0 <-> BCLK FOR FAST ONLY	(2) PH0 = BCLK/4
PH0 <-> BCLK FOR FAST ONLY	(3) PH0 = BCLK/8
PH0 <-> BCLK FOR FAST ONLY	(4) PH0 = BCLK/16

2.2.5 SYSTEM CLOCK GENERATOR

For the system clock, the clock switch circuit permits different clock inputs from XTOSC and CFOSC to be selected. The FAST and SLOW instructions can switch the clock input of the system clock generator (SGC).

The basic system clock is shown below:



2.3 PROGRAM COUNTER (PC)

This is a 14-bit counter, which addresses the program memory (ROM) for up to 12288 addresses. Program counter (PC11) is a page register. Only CALL and JMP instructions can address the whole address range (0000h ~ 2FFFh), the rest jump relative instructions can only address within a page (page x_0 (X000h ~ X7FFh) or page x_1 (X800h ~ XFFFh)). The MSB of program counter (PC13 and PC12) is a bank register. When CALL&JMP has to jump to the address which located in another bank, compile will insert "SF2 1xx0000b"&"JMP X" instructions in bank convert area (X100~X1FFh) to accomplish the bank jump operation automatically.

Example:

Source file =>

```
        org     1300h
        CALL    level1          ;Bank1
                :
                :
        org      0745h
        level1:                 ;Bank0
                :
                :
```

Compile to =>

```
        CAL     130h
                ↓
        SF2     40h             ;Insert to address 1130h by compiler , and jump to 0131h.
                ↓
        JMP     745h            ;Insert to address  0131h by compiler, and jump to 0745h.
```

- For ICE compatibility and bank jump operation, it is strongly recommended don't execute "CPHL X" instruction in following address:
  00FFh, 10FFh, 20FFh, 0FFEh, 1FFEh, and 2FFEh.
- The program counter (PC) is normally increased by one (+1) with every instruction execution, and it will not be limited by bank and page range.
  PC ← PC + 1
- When executing JMP instructions, subroutine call instructions (CALL), interrupt service routines or if reset occurs, the program counter (PC) loads the specified address corresponding to table 2-3-(1).
  PC ← specified address shows in Table 2-3-(1).
- When executing any jump instruction except JMP and CALL, the program counter (PC) loads the specified address in the operand of instruction. All of these jump relative instructions can only address the current page. That means when the current page is page x_0 (PC11=0), only the range X000h ~ X7FFh can be addressed; when the current page is page x_1 (PC11=1), only the range X800h ~ XFFFh is addressed.
  PC ← current page (PC11) + specified address in operand
- Return instruction (RTS)
  PC ← content of stack specified by the stack pointer
  Stack pointer ← stack pointer – 1

Table 2-3-(1)

	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Initial reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Interrupt 2 (INT pin)	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Interrupt 0 (input port C or D)	0	0	0	0	0	0	0	0	0	1	0	1	0	0
Interrupt 1 (timer 1 interrupt)	0	0	0	0	0	0	0	0	0	1	1	0	0	0
Interrupt 3 (pre-divider interrupt)	0	0	0	0	0	0	0	0	0	1	1	1	0	0
Interrupt 4 (timer 2 interrupt)	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Interrupt 5 (Key Scanning interrupt)	0	0	0	0	0	0	0	0	1	**0**	0	1	0	0
Interrupt 6 (RFC counter interrupt)	0	0	0	0	0	0	0	0	1	0	1	0	0	0
CALL,JMP	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
Other jump instructions	-	-	-	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

P10 to P0: Low-order 11 bits of instruction operand;

P11: page register;

P31, P12: Bank registers.

When executing subroutine call instructions or interrupt service routines, the contents of the program counter (PC) are automatically saved to the stack register (STACK).

2.4 PROGRAM/TABLE MEMORY

BANK0	BANK1	BANK2
0000H	1000H	2000H
BANK CONVERT AREA (X100~X1FFH)		
PAGE0_0 07FFH	PAGE1_0 17FFH	PAGE2_0 27FFH
0800H PAGE0_1 0FFFH	1800H PAGE1_1 1FFFH	2800H PAGE2_1 (Mask Option with Table ROM) 2FFFH

The built-in mask ROM is organized with 12288 x 16 bits. There are 6 pages of memory space in this mask ROM. Page x_0 covers the address range from X000h to X7FFh and page x_1 covers X800h to XFFFh.

Both instruction ROM (PROM) and table ROM (TROM) share this memory space. The partition formula for PROM and TROM is shown below:

Instruction ROM memory space = 10240 + (256 * N) words,
Table ROM memory space = 512(8 - N) bytes (N = 0 ~ 8).

Note: The data width of table ROM is 8-bit.

The partition of memory space is defined by mask option, as shown in the table below:

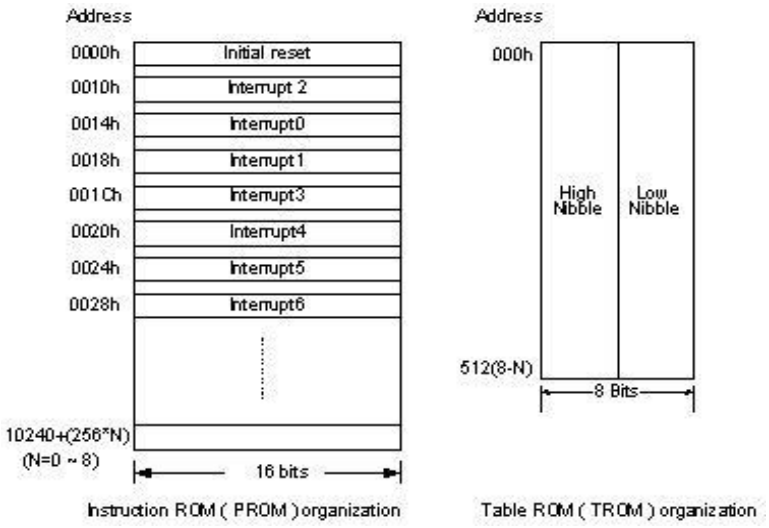
MASK OPTION table:

Mask Option name	Selected item	Instruction ROM memory space (Words)	Table ROM memory space(Bytes)
INSTRUCTION ROM <-> TABLE ROM	1 (N=0)	10240	4096
INSTRUCTION ROM <-> TABLE ROM	2 (N=1)	10496	3584
INSTRUCTION ROM <-> TABLE ROM	3 (N=2)	10752	3072
INSTRUCTION ROM <-> TABLE ROM	4 (N=3)	11008	2560
INSTRUCTION ROM <-> TABLE ROM	5 (N=4)	11264	2048
INSTRUCTION ROM <-> TABLE ROM	6 (N=5)	11520	1536
INSTRUCTION ROM <-> TABLE ROM	7 (N=6)	11776	1024
INSTRUCTION ROM <-> TABLE ROM	8 (N=7)	12032	512
INSTRUCTION ROM <-> TABLE ROM	9 (N=8)	12288	0

2.4.1 NSTRUCTION ROM (PROM)

There are some special locations that serve as interrupt service routines, such as reset address (000H), interrupt 0 address (014H), interrupt 1 address (018H), interrupt 2 address (010H), interrupt 3 address (01CH), interrupt 4 address (020H), interrupt 5 address (024H), and interrupt 6 address (028H), in the program memory.

When the useful address range of PROM exceeds 2048/4096 addresses, the memory space of PROM will automatically be defined as 6 pages/3 banks. *Refer to section 2-3.*



This figure shows the Organization of ROM

2.4.2 TABLE ROM (TROM)

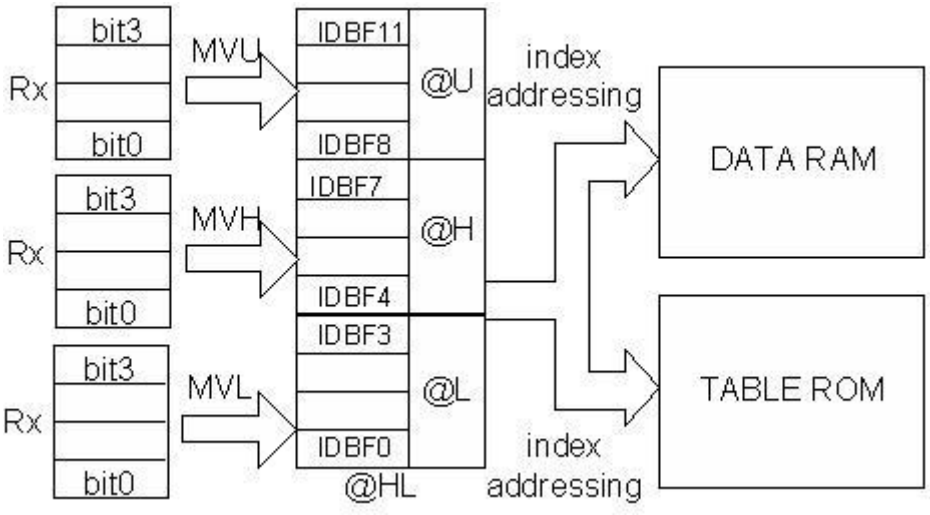
The table ROM is organized with 512(8-N) x 8 bits that share memory space with the instruction ROM (as shown in the figure above). This memory space stores the constant data or look up table for the usage of main program. All of the table ROM addresses are specified by the index address register (@HL). The data width can be 8 bits (512(8-N) x 8 bits) or 4 bits (1024(8-N) x 4 bits) depending on usage.

2.5 INDEX ADDRESS REGISTER (@HL)

This is a versatile address pointer for the data memory (RAM) and table ROM (TROM). The index address register (@HL) is a 12-bit register, and the contents of the register can be modified by executing MVH, MVL and MVU instructions. MVL instructions, when executed, will load the content of specified data memory to the lower nibble of the index register (@L). In the same manner, executing MVH and MVU instructions will load the content of the data RAM (Rx) to the higher nibble of the register @H and @U, respectively.

@U register				@H register				@L register			
Bit3	Bit2	Bit1	Bit0	Bit3	Bit2	Bit1	Bit0	Bit3	Bit2	Bit1	Bit0
IDBF11	IDBF10	IDBF9	IDBF8	IDBF7	IDBF6	IDBF5	IDBF4	IDBF3	IDBF2	IDBF1	IDBF0

The index address register can specify the full range addresses of the table ROM and data memory.



This figure shows the diagram of the index address register.

The index address register is a write-only register, CPHL X instruction can specify 8-bit immediate data to compare with the content of @H and @L. When the result of comparison is equivalent, the instruction behind CPHL X will be skipped (NOP); if not equivalent, the instruction behind CPHL X will be executed normally.

Note: During the comparison of the index address, all the interrupt enable flags (IEF) have to be cleared to avoid malfunction.

The comparison bit pattern is shown below:

CPHL X	X7	X6	X5	X4	X3	X2	X1	X0
@HL	IDBF7	IDBF6	IDBF5	IDBF4	IDBF3	IDBF2	IDBF1	IDBF0

Example:

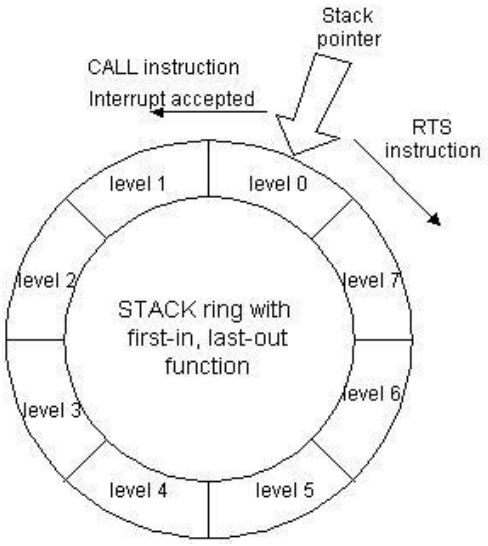
```
……                ; @HL = 30h
SIE*    0h        ; disable IEF
CPHL    30h
JMP     lable1    ; this instruction will be force as NOP
JMP     lable2    ; this instruction will be executed and then jump to lable2
…….
lable1:
……..
lable2:
```

2.6 STACK REGISTER (STACK)

Stack is a specially designed register following the first-in-last-out rule. It is used to save the contents of the program counter sequentially during subroutine calls or execution of interrupt service routines. The contents of the stack register are returned sequentially to the program counter (PC) when return instructions (RTS) are executed. The stack register is organized by using 14 bits by 8 levels, but with no overflow flag; hence only 8 levels of subroutine calls or interrupts are allowed (If the stacks are full, and either an interrupt occurs or a subroutine call executes, the first level will be overwritten).

Once the subroutine call or interrupt causes a stack register (STACK) overflow, the stack pointer will return to 0 and the contents of the level 0 stack will be overwritten by the PC value. The contents of the stack register (STACK) are returned sequentially to the program counter (PC) when the RTS instruction is executed. Once the RTS instruction causes a stack register (STACK) underflow, the stack pointer will return to level 7 and the content of the level 7 stack will be restored to the program counter.

The following figure shows the diagram of the stack.



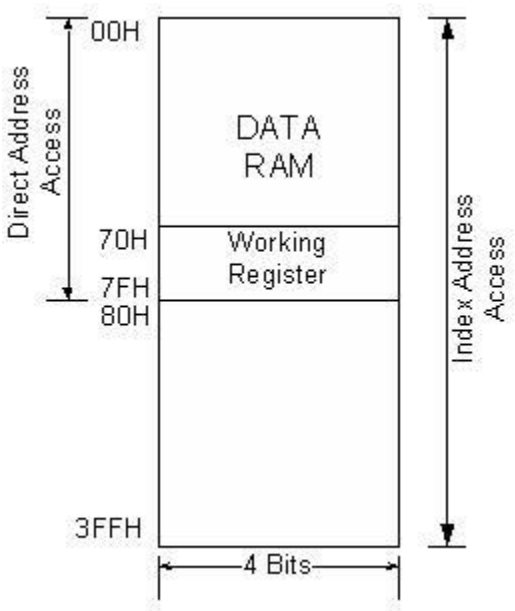
2.7 DATA MEMORY (RAM)

Static RAM is organized with 1024 addresses x 4 bits and used to store data.

The data memory may be accessed through two methods:

1. rect addressing mode
   The address of the data memory is specified by the instructions and the addressing range is from 00H to 7FH.
2. Index addressing mode
   The index address register (@HL) specifies the address of the data memory and all address space from 00H to 3FFH can be accessed.

The 16 specified addresses (70H to 7FH) in the direct addressing memory are also used as 16 working registers. The function of working registers will be described in detail *in section 2-6*.



This figure shows the Data Memory (RAM) and Working Register Organization.

2.8 WORKING REGISTER (WR)

The locations 70H to 7FH of the data memory (RAM) are not only used as general-purpose data memory but also as working registers (WR). The following will introduce the general usage of working registers:

- They can be used to perform operations on the contents of the working register and immediate data. Such as: ADCI, ADCI*, SBCI, SBCI*, ADDI, ADDI*, SUBI, SUBI*, ADNI, ADNI*, ANDI, ANDI*, EORI, EORI*, ORI, ORI*.
- They can be used to transfer data between the working register and any address in the direct addressing data memory (RAM). Such as: MWR Rx, Ry; MRW Ry, Rx.
- They can be used to decode (or directly transfer) the contents of the working register and output to the LCD PLA circuit. Such as: LCT, LCB, LCP.

2.9 ACCUMULATOR (AC)

The accumulator (AC) is a register that plays the most important role in operations and controls. By using it in conjunction with the ALU (Arithmetic and Logic Unit), data transfer between the accumulator and other registers or data memory is made possible.

2.10 ALU (Arithmetic and Logic Unit)

This is circuitry that performs arithmetic and logic operations. The ALU provides the following functions:

- Binary addition/subtraction (INC, DEC, ADC, SBC, ADD, SUB, ADN, ADCI, SBUI, ADNI)
- Logic operation (AND, EOR, OR, ANDI, EORI, ORI)
- Shift (SR0, SR1, SL0, SL1)
- Decision (JB0, JB1, JB2, JB3, JC, JNC, JZ, and JNZ)
- BCD operation (DAA, DAS)

2.11 HEXADECIMAL CONVERT TO DECIMAL (HCD)

Decimal format is another number format for TM8727. When the content of the data memory has been assigned as decimal format, it is necessary to convert the results to decimal format after the execution of ALU instructions. When the decimal converting operation is being processed, all of the operand data (including the contents of the data memory (RAM), accumulator (AC), immediate data, and look-up table) should be in the decimal format, or the results of conversion will be incorrect.

Instructions DAA, DAA*, DAA @HL can convert data from hexadecimal to decimal format after any addition operation. The conversion rules are shown in the following table and illustrated in example 1.

AC data before DAA execution	CF data before DAA execution	AC data after DAA execution	CF data after DAA execution
0 ≤ AC ≤ 9	CF = 0	no change	no change
A ≤ AC ≤ F	CF = 0	AC= AC+ 6	CF = 1
0 ≤ AC ≤ 3	CF = 1	AC= AC+ 6	no change

Example 1:

```
LDS     10h, 9      ; Load immediate data “9” to data memory address 10H.
LDS     11h, 1      ; Load immediate data “1” to data memory address 11H and AC.
RF 1h               ; Reset CF to 0.
ADD*    10h         ; Contents of the data memory address 10H and AC are
                    ; binary-added; the result loads to AC & data memory address
                    ; 10H. (R10 = AC = AH, CF = 0)
DAA*    10h         ; Convert the content of AC to
                    ; Decimal format.
                    ; The result in the data memory address 10H is “0” and in
                    ; The CF is “1”. This represents the decimal number “10”.
```

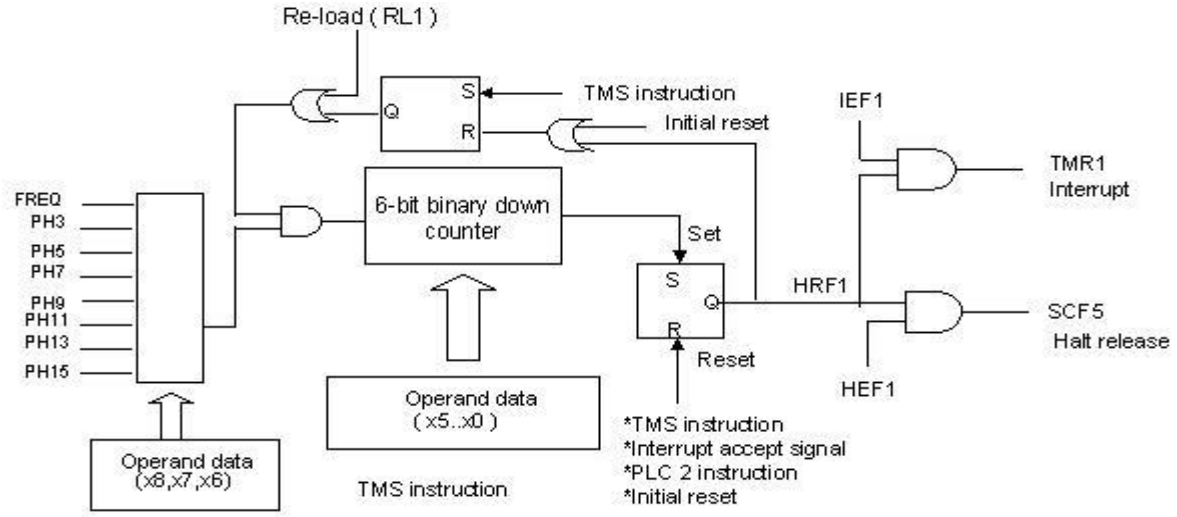
Instructions DAS, DAS*, DAS @HL can convert the data from hexadecimal format to decimal format after any subtraction operation. The conversion rules are shown in the following table and illustrated in Example 2.

AC data before DAS execution	CF data before DAS execution	AC data after DAS execution	CF data after DAS execution
0 ≤ AC ≤ 9	CF = 1	No change	no change
6 ≤ AC ≤ F	CF = 0	AC= AC+A	no change

Example 2:

```
LDS     10h, 1      ; Load immediate data "1" to the data memory address 10H.
LDS     11h, 2      ; Load immediate data "2" to the data memory address 11H and AC.
SF      1h          ; Set CF to 1, which means no borrowing has occurred.
SUB*    10h         ; Content of data memory address 10H is binary-subtracted;
                    ; The result loads to data memory address
                    ; 10H. (R10 = AC = FH, CF = 0)
DAS*    10h         ; Convert the content of the data memory address 10H to decimal
                    ; Format. The result in the data memory address 10H is "9" and in
                    ; The CF is "0". This represents the decimal number "–1".
```

2.12 TIMER 1 (TMR1)



This figure shows the TMR1 organization.

2.12.1 NORMAL OPERATION

TMR1 consists of a programmable 6-bit binary down counter, which is loaded and enabled by executing the TMS or TMSX instructions. Once the TMR1 counts down to 3Fh, it generates an underflow signal to set the halt release request flag 1 (HRF1) to 1 and then stops counting down. When HRF1 = 1, and the TMR1 interrupt enable flag (IEF1) = 1, an interrupt is generated.

When HRF1 = 1, if the IEF1 = 0 and the TMR1 halt release enable (HEF1) = 1, the program will escape from halt mode (if CPU is in halt mode) and then set the start condition flag 5 (SCF5) to 1 in the status register 3 (STS3). After power on reset, the default clock source of TMR1 is PH3. If watchdog reset occurs, the clock source of TMR1 will remain the same.

The following table shows the definition of each bit in TMR1 instructions.

OPCODE	Select clock				Initiate value of timer				
TMSX X	X8	X7	X6	X5	X4	X3	X2	X1	X0
TMS Rx	0	AC3	AC2	AC1	AC0	Rx3	Rx2	Rx1	Rx0
TMS @HL	0	bit7	bit6	bit5	Bit4	bit3	bit2	bit1	bit0

The following table shows the clock source setting for TMR1.

X8	X7	X6	clock source
0	0	0	PH9
0	0	1	PH3
0	1	0	PH15
0	1	1	FREQ
1	0	0	PH5
1	0	1	PH7
1	1	0	PH11
1	1	1	PH13

Note:

1. When the TMR1 clock is PH3
TMR1 set time = (Set value + error) * 8 * 1/fosc (KHz) (ms)
2. When the TMR1 clock is PH9
TMR1 set time = (Set value + error) * 512 * 1/fosc (KHz) (ms)
3. When the TMR1 clock is PH15
TMR1 set time = (Set value + error) * 32768 * 1/fosc (KHz) (ms)
4. When the TMR1 clock is PH5
TMR1 set time = (Set value + error) * 32 * 1/fosc (KHz) (ms)
5. When the TMR1 clock is PH7
TMR1 set time = (Set value + error) * 128 * 1/fosc (KHz) (ms)
6. When the TMR1 clock is PH11
TMR1 set time = (Set value + error) * 2048 * 1/fosc (KHz) (ms)
7. When the TMR1 clock is PH13
TMR1 set time = (Set value + error) * 8192 * 1/fosc (KHz) (ms)
Set value: Decimal number of timer set value
Error: The tolerance of set value, 0 < error <1.
Fosc: Input of the pre-divider
PH3: The 3rd stage output of the pre-divider
PH5: The 5th stage output of the pre-divider
PH7: The 7th stage output of the pre-divider
PH9: The 9th stage output of the pre-divider
PH11: The 11th stage output of the pre-divider
PH13: The 13th stage output of the pre-divider
PH15: The 15th stage output of the pre-divider
8. When the TMR1 clock is FREQ
TMR1 set time = (Set value + error) * 1/FREQ (KHz) (ms).
FREQ: *Refer to section 3-3-4.*

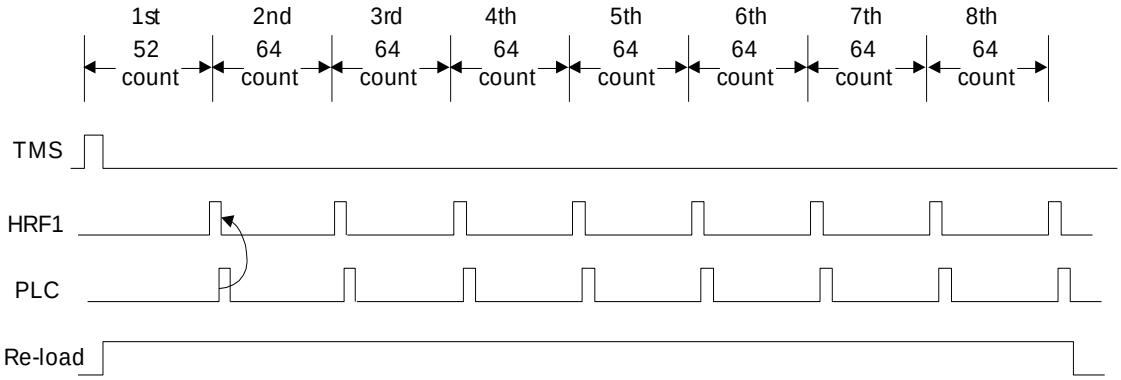
2.12.2 RE-LOAD OPERATION

TMR1 provides the re-load function, which can extend any time interval greater than 3Fh. The SF 80h instruction enables the re-load function and RF 80h instruction disables it. When the re-load function is enabled, the TMR1 will not stop counting until the re-load function is disabled and TMR1 underflows again. During this operation, the program must use the halt release request flag or interrupt to check the wanted counting value.

- It is necessary to execute either the TMS or the TMSX instructions to set the down count value before the re-load function is enabled, because TMR1 will automatically count down with an unknown value once the re-load function is enabled.
- Never disable the re-load function before the last expected halt release or interrupt occurs. If TMS related instructions are not executed after each halt release or interrupt occurs, the TMR1 will stop operating immediately after the re-load function is disabled.

For example:

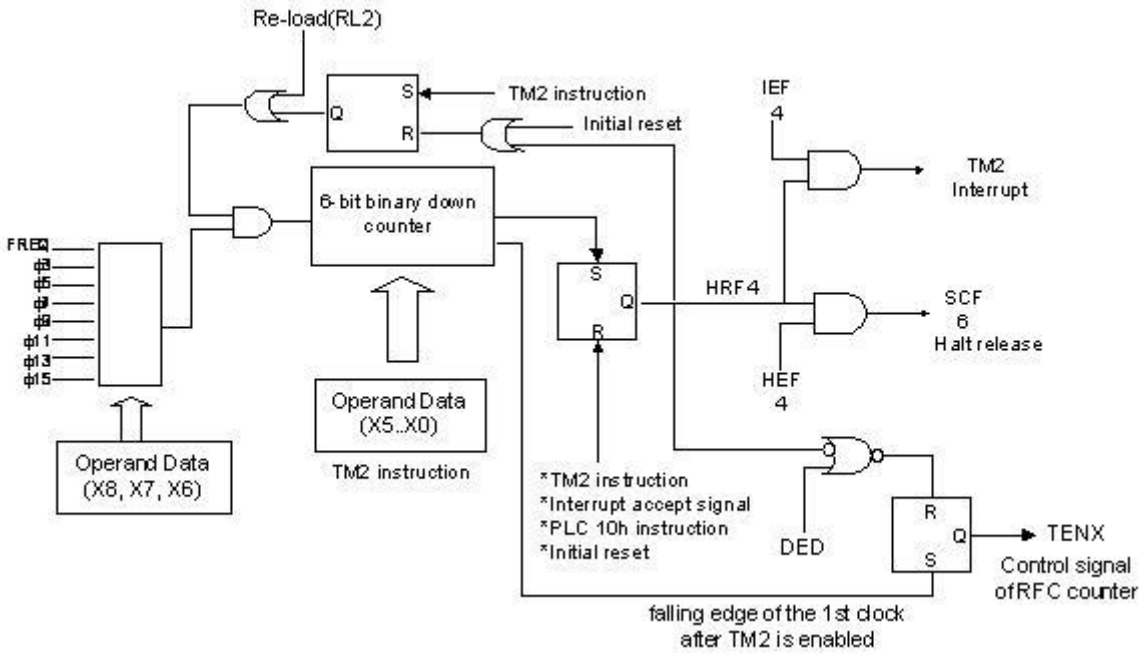
If the expected count down value is 500, it may be divided as 52 + 7 * 64. First, set the initiate count down value of TMR1 to 52 and start counting, then enable the TMR1 halt release or interrupt function. Before the first time underflow occurs, enable the re-load function. The TMR1 will continue operating even though TMR1 underflow occurs. When halt release or interrupt occurs, clear the HRF1 flag through a PLC instruction. After a halt release or interrupt occurs 8 times, disable the re-load function; counting is completed.



In this example, S/W enters the halt mode to wait for the underflow of TMR1.

```
        LDS     0, 0            ;initiate the underflow counting register
        PLC     2
        SHE     2               ;enable the HALT release caused by TMR1
        TMSX    34h             ;initiate the TMR1 value (52) and clock source is ϕ9
        SF      80h             ;enable the re-load function
RE_LOAD:
        HALT
        INC*    0               ;increase the underflow counter
        PLC     2               ;clear HRF1
        JB3     END_TM1         ;if the TMR1 underflow counter is equal to 8, exit subroutine
        JMP     RE_LOAD
        END_TM1:
        RF      80h             ;disable the re-load function
```

2.13 TIMER 2 (TMR2)



The figure shows the TMR2 organization.

2.13.1 NORMAL OPERATION

TMR2 consists of a programmable 6-bit binary down counter, which is loaded and enabled by executing either the TM2 or the TM2X instructions. Once TMR2 counts down to 3Fh, it stops counting, then generates an underflow signal and sets the halt release request flag 4 (HRF4) to 1.

- When HRF4 = 1, and the TMR2 interrupt enabler (IEF4) is set to 1, the interrupt occurs.
- When HRF4 =1, IEF4 = 0, and the TMR2 halt release enabler (HEF4) is set to 1, the program will escape from halt mode (if CPU is in halt mode) and HRF4 sets the start condition flag 6 (SCF6) to 1 in the status register 4 (STS4).

After power on reset, the default clock source of TMR2 is PH7.

If watchdog reset occurs, the clock source of TMR2 will remain the same.

The following table shows the definition of each bit in TMR2 instructions.

OPCODE	Select clock			Initiate value of timer					
TM2X X	X8	X7	X6	X5	X4	X3	X2	X1	X0
TM2 Rx	0	AC3	AC2	AC1	AC0	Rx3	Rx2	Rx1	Rx0
TM2 @HL	0	bit7	bit6	bit5	Bit4	bit3	bit2	bit1	bit0

The following table shows the clock source setting for TMR2.

X8	X7	X6	clock source
0	0	0	PH9
0	0	1	PH3
0	1	0	PH15
0	1	1	FREQ
1	0	0	PH5
1	0	1	PH7
1	1	0	PH11
1	1	1	PH13

Note:

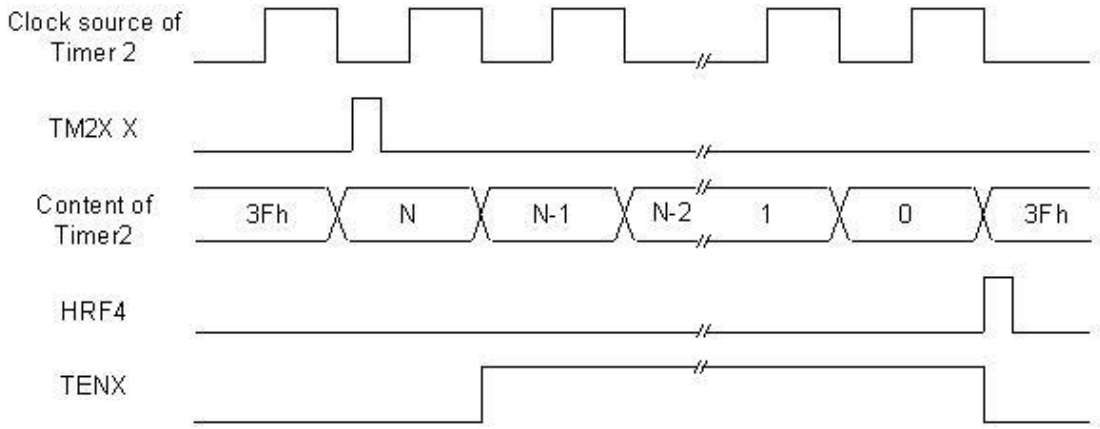
1. When the TMR2 clock is PH3
TMR2 set time = (Set value + error) * 8 * 1/fosc (KHz) (ms)
2. When the TMR2 clock is PH9
TMR2 set time = (Set value + error) * 512 * 1/fosc (KHz) (ms)
3. When the TMR2 clock is PH15
TMR2 set time = (Set value + error) * 32768 * 1/fosc (KHz) (ms)
4. When the TMR2 clock is PH5
TMR2 set time = (Set value + error) * 32 * 1/fosc (KHz) (ms)
5. When the timer clock is PH7
TMR2 set time = (Set value + error) * 128 * 1/fosc (KHz) (ms)
6. When the TMR2 clock is PH11
TMR2 set time = (Set value + error) * 2048 * 1/fosc (KHz) (ms)
7. When the TMR2 clock is PH13
TMR2 set time = (Set value + error) * 8192 * 1/fosc (KHz) (ms)
Set value: Decimal number of timer set value
Error: the tolerance of set value, 0 < error <1.
Fosc: Input of the pre-divider
PH3: The 3rd stage output of the pre-divider
PH5: The 5th stage output of the pre-divider
PH7: The 7th stage output of the pre-divider
PH9: The 9th stage output of the pre-divider
PH11: The 11th stage output of the pre-divider
PH13: The 13th stage output of the pre-divider
PH15: The 15th stage output of the pre-divider
8. When the TMR2 clock is FREQ
TMR2 set time = (Set value + error) * 1/FREQ (KHz) (ms).
FREQ: *Refer to section 3-3-4.*

2.13.2 RE-LOAD OPERATION

TMR2 also provides the re-load function, the same as TMR1. The instruction SF2 1 enables the re-load function; the instruction RF2 1 disables it.

2.13.3 TIMER 2 (TMR2) IN RESISTOR TO FREQUENCY CONVERTER (RFC)

TMR2 also controls the operation of RFC function. TMR2 will set TENX flag to 1 to enable the RFC counter; once the TMR2 underflows, the TENX flag will be reset to 0 automatically. In this case, Timer 2 can set an accurate time period without setting a value error like the other operations of TMR1 and TMR2. *Refer to 2-16 for detailed information on controlling the RFC counter*.



The following figure shows the operating timing of TMR 2 in RFC mode.

TMR2 also provides the re-load function when controlling the RFC function.

The SF2 1h instruction enables the re-load function, and the DED flag should be set to 1 by SF2 2h instruction. Once DED flag has been set to 1, TENX flag will not be cleared to 0 while TMR2 underflows (but HRF4 will be set to1). The DED flag must be cleared to 0 by executing RF2 2h instruction before the last HRF4 occurs; thus, the TENX flag will be reset to 0 after the last HRF4 flag delivery. After the last underflow (HRF4) of TMR2 occurs, disable the re-load function by executing the RF2 1h instruction.

For example:

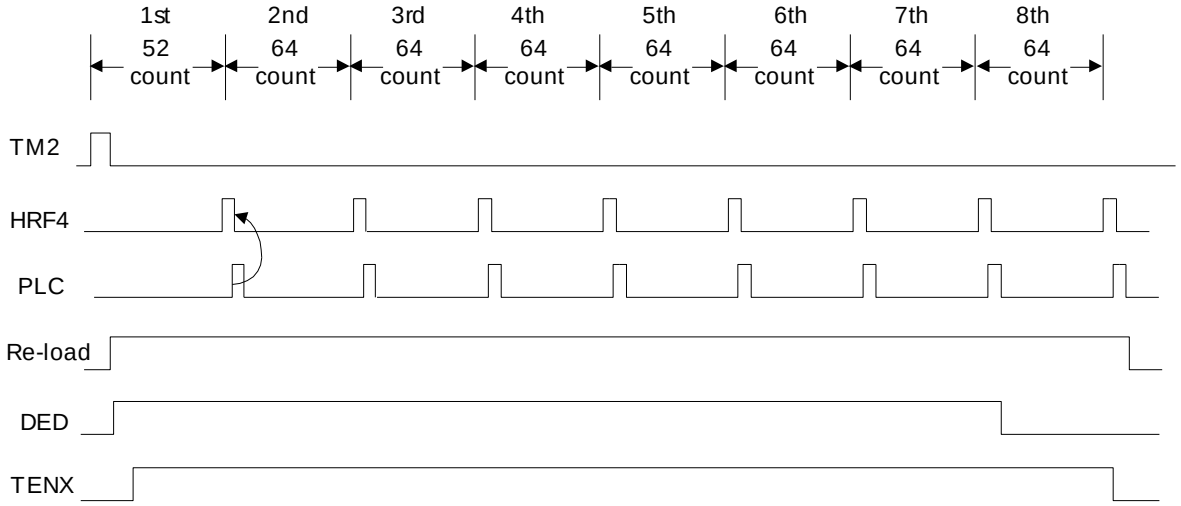
If the target set value is 500, it will be divided as 52 + 7 * 64.

1. the initiate value of TMR2 to 52 and start counting.
2. Enable the TMR2 halt release or interrupt function.
3. Before the first underflow occurs, enable the re-load function and set the DED flag. The TMR2 will continue counting even if TMR2 underflows.
4. When halt release or interrupt occurs, clear the HRF4 flag by PLC instruction and increase the counting value to count the underflow times.
5. When halt release or interrupt occurs for the 7^{th} time, reset the DED flag.

6. When halt release or interrupt occurs for the 8th time, disable the re-load function and the counting is completed.

In this example, S/W enters the halt mode to wait for the underflow of TM2.

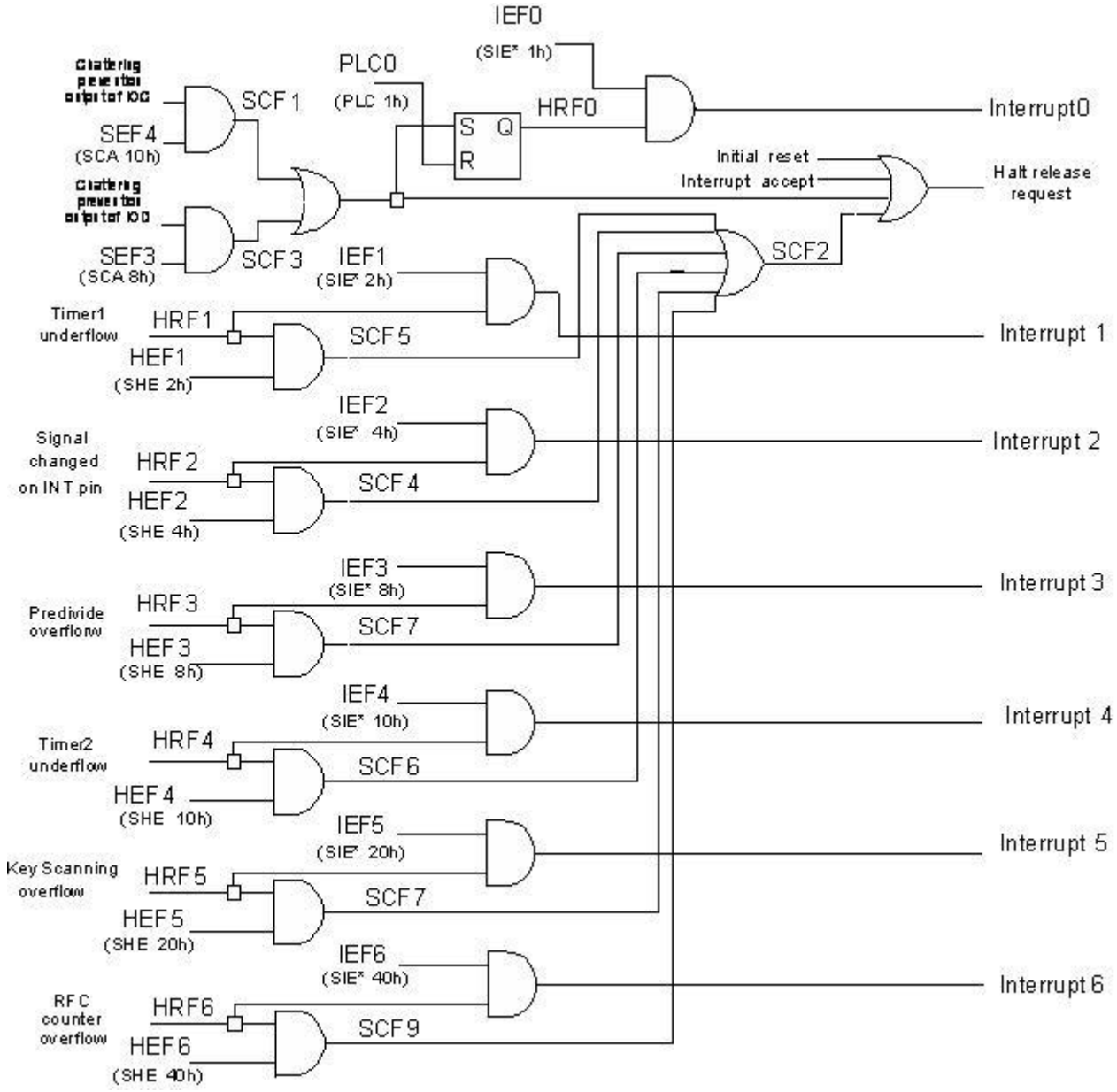
```
        LDS     0,0             ;initiate the underflow counting register
        PLC     10h
        SHE     10h             ;enable the halt release caused by TM2
        SRF     19h             ;enable RFC, and controlled by TM2
        TM2X    34h             ;initiate the TM value(52) and clock source is ϕ9
        SF2      3h             ;enable the re-load function and set DED flag to 1
RE_LOAD:
        HALT
        INC*    0               ;increase the underflow counter
        PLC     10h             ;clear HRF4
        LDS     20h, 7
        SUB     0               ;when halt is released for the 7th time, reset DED flag
        JNZ     NOT_RESET_DED
        RF2     2               ;reset DED flag
NOT_RESET_DED:
        LDA     0               ;store underflow counter to AC
        JB3     END_TM1         ; if the TM2 underflow counter is equal to 8, exit this subroutine
        JMP     RE_LOAD
END_TM1:
        RF2     1               ;disable the re-load function
```



This figure shows the operating timing of TMR2 re-load function for RFC

2.14 STATUS REGISTER (STS)

The status register (STS) is organized with 4 bits and comes in 4 types: status register 1 (STS1) to status register 4 (STS4). The following figure shows the configuration of the start condition flags for TM8727.



2.14.1 STATUS REGISTER 1 (STS1)

Status register 1 (STS1) consists of 2 flags:

1. rry flag (CF)
   The carry flag is used to save the results of the carry or borrow during the arithmetic operation.
2. Zero flag (Z)
   Indicate the accumulator (AC) status. When the content of the accumulator is 0, the Zero flag is set to 1. If the content of the accumulator is not 0, the zero flag is reset to 0.

   The MAF instruction can be used to transfer data in status register 1 (STS1) to the accumulator (AC) and the data memory (RAM).

   The MRA instruction can be used to transfer data of the data memory (RAM) to the status register 1 (STS1).

The bit pattern of status register 1 (STS1) is shown below.

Bit 3	Bit 2	Bit 1	Bit 0
Carry flag (AC)	Zero flag(Z)	NA	NA
Read / write	Read only	Read only	Read only

2.14.2 STATUS REGISTER 2 (STS2)

Status register 2 (STS2) consists of start condition flag 1, 2 (SCF1, SCF2) and the backup flag.

The MSB instruction can be used to transfer data in status register 2 (STS2) to the accumulator (AC) and the data memory (RAM), but it is impossible to transfer data of the data memory (RAM) to status register 2 (STS2).

The following table shows the bit pattern of each flag in status register 2 (STS2).

Bit 3	Bit 2	Bit 1	Bit 0
Start condition flag 3 (SCF3)	Start condition flag 2 (SCF2)	Start condition flag 1 (SCF1)	Backup flag (BCF)
Halt release caused by the IOD port	Halt release caused by SCF4,5,6,7,9	Halt release caused by the IOC port	The backup mode status
Read only	Read only	Read only	Read only

- Start condition flag 3 (SCF3)
  When the SCA instruction specified signal change occurs at port IOD to release the halt mode, SCF3 will be set. Executing the SCA instruction will cause SCF3 to be reset to 0.
- Start condition flag 1 (SCF1)
  When the SCA instruction specified signal change occurs at port IOC to release the halt mode, SCF1 will be set. Executing the SCA instruction will cause SCF1 to be reset to 0.
- Start condition flag 2 (SCF2)
  When a factor other than port IOA and IOC causes the halt mode to be released, SCF2 will be set to1. In this case, if one or more start condition flags in SCF4, 5, 6, 7, 9 are set to 1, SCF2 will also be set

to 1 simultaneously. When all of the flags in SCF4, 5, 6, 7, 9 are cleared, start condition flag 2 (SCF2) is reset to 0.
Note: If start condition flag is set to 1, the program will not be able to enter halt mode.

- Backup flag (BCF)
  This flag can be set/reset by executing the SF 2h/RF 2h instruction.

2.14.3 STATUS REGISTER 3 (STS3)

When the halt mode is released by the start condition flag 2 (SCF2), status register 3 (STS3) will store the status of the factor in the release of the halt mode.

Status register 3 (STS3) consists of 4 flags:

1. Start condition flag 4 (SCF4)
   Start condition flag 4 (SCF4) is set to 1 when the signal change at the INT pin causes the halt release request flag 2 (HRF2) to be output and the halt release enable flag 2 (HEF2) is set beforehand. To reset start condition flag 4 (SCF4), the PLC instruction must be used to reset the halt release request flag 2 (HRF2) otherwise the SHE instruction must be used to reset the halt release enable flag 2 (HEF2).
2. Start condition flag 5 (SCF5)
   Start condition flag 5 (SCF5) is set when an underflow signal from Timer 1 (TMR1) causes the halt release request flag 1 (HRF1) to be output and the halt release enable flag 1 (HEF1) is set beforehand. To reset start condition flag 5 (SCF5), the PLC instruction must be used to reset the halt release request flag 1 (HRF1) otherwise the SHE instruction must be used to reset the halt release enable flag 1 (HEF1).
3. Start condition flag 7 (SCF7)
   Start condition flag 7 (SCF7) is set when an overflow signal from the pre-divider causes the halt release request flag 3 (HRF3) to be output and the halt release enable flag 3 (HEF3) is set beforehand. To reset start condition flag 7 (SCF7), the PLC instruction must be used to reset the halt release request flag 3 (HRF3) otherwise the SHE instruction must be used to reset the halt release enable flag 3 (HEF3).
4. Contents of the pre-divider on the 15th stage.

The MSC instruction is used to transfer the contents of status register 3 (STS3) to the accumulator (AC) and the data memory (RAM).

The following table shows the Bit Pattern of Status Register 3 (STS3).

Bit 3	Bit 2	Bit 1	Bit 0
Start condition flag 7 (SCF7)	15th stage of the pre-divider	Start condition flag 5 (SCF5)	Start condition flag 4 (SCF4)
Halt release caused by pre-divider overflow		Halt release caused by TMR1 underflow	Halt release caused by INT pin
Read only	Read only	Read only	Read only

2.14.4 STATUS REGISTER 3X (STS3X)

When the halt mode is released with start condition flag 2 (SCF2), status register 3X (STS3X) will store the status of the factor in the release of the halt mode.

Status register 3X (STS3X) consists of 3 flags:

1. Start condition flag 8 (SCF8)
   SCF8 is set to 1 when any one of KI1~4 =1/0 (KI1~4=1 in LED mode / KI1~4=0 in LCD mode) causes the halt release request flag 5 (HRF5) to be output and the halt release enable flag 5 (HEF5) is set beforehand. To reset the start condition flag 8 (SCF8), the PLC instruction must be used to reset the halt release request flag 5 (HRF5) otherwise the SHE instruction must be used to reset the halt release enable flag 5 (HEF5).
2. Start condition flag 6 (SCF6)
   SCF6 is set to 1 when an underflow signal from timer 2 (TMR2) causes the halt release request flag 4 (HRF4) to be output and the halt release enable flag 4 (HEF4) is set beforehand. To reset the start condition flag 6 (SCF6), the PLC instruction must be used to reset the halt release request flag 4 (HRF4) otherwise the SHE instruction must be used to reset the halt release enable flag 4 (HEF4).
3. Start condition flag 9 (SCF9)
   SCF9 is set when a finish signal from mode 3 of RFC function causes the halt release request flag 6 (HRF6) to be output and the halt release enable flag 9 (HEF9) is set beforehand. In this case, the 16-counter of RFC function must be controlled by CX pin; *please refer to 2-16-9*. To reset the start condition flag 9 (SCF9), the PLC instruction must be used to reset the halt release request flag 6 (HRF6) otherwise the SHE instruction must be used to reset the halt release enable flag 6 (HEF6).

The MCX instruction can be used to transfer the contents of status register 3X (STS3X) to the accumulator (AC) and the data memory (RAM).

The following table shows the Bit Pattern of Status Register 3X (STS3X).

Bit 3	Bit 2	Bit 1	Bit 0
Start condition flag 9 (SCF9)	NA	Start condition flag 6 (SCF6)	Start condition flag 8 (SCF8)
Halt release caused by RFC counter finish		Halt release caused by TMR2 underflow	Halt release caused by SKI underflow
Read only	Read only	Read only	Read only

2.14.5 STATUS REGISTER 4 (STS4)

Status register 4 (STS4) consists of 3 flags:

1. System clock selection flag (CSF)
   The system clock selection flag (CSF) indicates which clock source of the system clock generator (SCG) is being used. Executing the SLOW instruction will change the clock source (BCLK) of the system clock generator (SCG) to the slow speed oscillator (XT clock), and resets the system clock selection flag (CSF) to 0. Executing the FAST instruction will change the clock source (BCLK) of the system clock generator (SCG) to the fast speed oscillator (CF clock), and sets the system clock selection flag (CSF) to 1. For the operation of the system clock generator, refer to 3-3.
2. Watchdog timer enable flag (WTEF)
   The watchdog timer enable flag (WDF) indicates the operating status of the watchdog timer.

3. Overflow flag of 16-bit counter of RFC (RFOVF)
The overflow flag of 16-bit counter of RFC (RFOVF) is set to 1 when the overflow of the 16-bit counter of RFC occurs. The flag will reset to 0 when this counter is initiated by executing the SRF instruction.

The MSD instruction can be used to transfer the contents of status register 4 (STS4) to the accumulator (AC) and the data memory (RAM).

The following table shows the Bit Pattern of Status Register 4 (STS4)

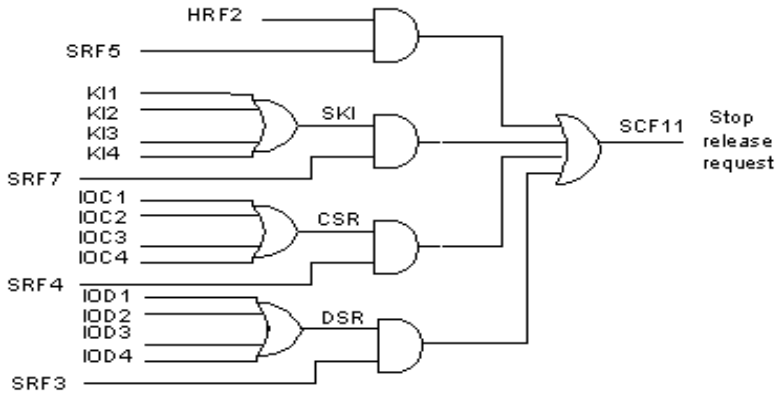
Bit 3	Bit 2	Bit 1	Bit 0
Reserved	The overflow flag of 16-bit counter of RFC (RFVOF)	Watchdog timer Enable flag (WDF)	System clock selection flag (CSF)
Read only	Read only	Read only	Read only

2.14.6 2-14-6. START CONDITION FLAG 11 (SCF11)

Start condition flag 11 (SCF11) will set to 1 in STOP mode when following conditions are met:

- A high level signal comes from the OR-ed output of the pins defined as input mode in IOC port, which causes the stop release flag of IOC port (CSR) to output. The stop release enable flag 4 (SRF4) is must be set beforehand.
- A high level signal comes from the OR-ed output of the pins defined as input mode in IOD port, which causes the stop release flag of IOD port (DSR) to output. The stop release enable flag 3 (SRF3) must be set beforehand.
- A high level signal comes from the OR-ed output of the signals latch for KI1~4, which causes the stop release flag of Key Scanning (SKI) to output. The stop release enable flag 4 (SRF7) must be set beforehand.
- The signal change from the INT pin causes the halt release flag 2 (HRF2) to output. The stop release enable flag 5 (SRF5) must be set beforehand.

The following figure shows the organization of start condition flag 11 (SCF 11).



The stop release flags (SKI, CSR, DSR, and HRF2) are specified by the stop release enable flags (SRFx). These flags should be cleared before the chip enters stop mode. All of the pins in the IOA and IOC ports

have to be set in input mode and keep in 0 state before the chip enters the STOP mode, otherwise the program cannot enter STOP mode. Instruction SRE is used to set or reset the stop release enable flags (SRF4, 5, 7).

The following table shows the stop release request flags.

	The OR-ed latched signals for KI1~4	The OR-ed input mode pins of IOC (IOD) port	The rising or falling edge on INT pin
Stop release request flag	SKI	CSR (DSR)	HRF2
Stop release enable flag	SRF7	SRF4 (SRF3)	SRF5

2.15 CONTROL REGISTER (CTL)

The control register (CTL) comes in 4 types: control register 1 (CTL1) to control register 4 (CTL4).

2.15.1 CONTROL REGISTER 1 (CTL1)

The control register 1 (CTL1), being a 1-bit register:

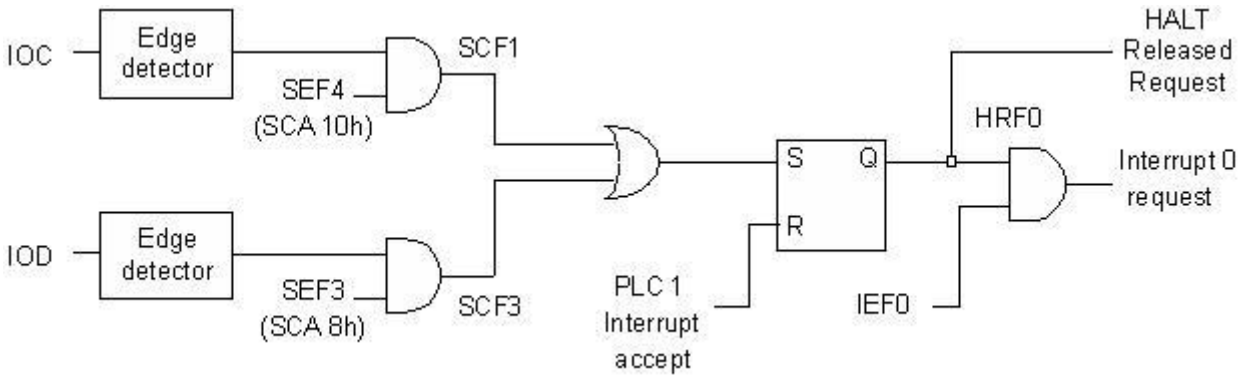
- Switch enable flag 4 (SEF4)
  Stores the status of the input signal change at pins of IOC set in input mode that causes the halt mode or stop mode to be released.
- Switch enable flag 3 (SEF3)
  Stores the status of the input signal change at pins of IOD set in input mode that causes the halt mode or stop mode to be released.

Executed the SCA instruction may set or reset these flags.

The following table shows Bit Pattern of Control Register 1 (CTL1).

Bit 4	Bit 3
Switch enable flag 4 (SEF4)	Switch enable flag 3 (SEF3)
Enable the halt release caused by the signal change on IOC port	Enable the halt release caused by the signal change on IOD port
Write only	Write only

The following figure shows the organization of control register 1 (CTL1).



2.15.1.1 ngs for Halt Mode

If the SEF4 (SEF3) is set to 1, the signal change on the IOC (IOD) port will cause the halt mode to be released and SCF1 (SCF3) will be set to 1. Because the input signal of IOC (IOD) port are ORed, it is necessary to keep the unchanged input signals at "0" state; only one of the input signal can change state.

2.15.1.2 The Settings for Stop Mode

If SRF4 (SRF3) and SEF4 (SEF3) are set, the stop mode will be released to set the SCF1 (SCF3) when a high level signal is applied to one of the input mode pins of IOC (IOD) port and the other pins stay in "0" state.

After the stop mode is released, TM8727 enters the halt condition. The high level signal must hold for a while to allow the chattering prevention circuitry of IOC (IOD) port to detect this signal and then set SCF1 (SCF3) to release the halt mode, otherwise the chip will return to stop mode again.

2.15.1.3 Interrupt for CTL1

The control register 1 (CTL1) performs the following function in the execution of the SIE instruction to enable the interrupt function. The input signal change at the input pins in IOC (IOD) port will deliver the SCF1 (SCF3) when SEF4 (SEF3) has been set to 1 by executing the SCA instruction. Once the SCF1 (SCF3) is delivered, the halt release request flag (HRF0) will be set to 1. In this case, if the interrupt enable flag 0 (IEF0) is set to 1 by executing the SIE instruction, the interrupt request flag 0 (interrupt 0) will be delivered to interrupt the program.

If the interrupt 0 is accepted by SEF4 (SEF3) and IEF0, the interrupt 0 request to the next signal change at IOC (IOD) will be inhibited. To release this mode, the SCA instruction must be executed again. *Refer to 2-16-1-1*.

2.15.2 CONTROL REGISTER 2 (CTL2)

Control register 2 (CTL2) consists of halt release enable flags 1, 2, 3, 4, 5, 6 (HEF1, 2, 3, 4, 5, 6) and is set by SHE instruction.

The bit pattern of the control register (CTL2) is shown below.

Halt release enable flag	HEF6	HEF5	HEF4
Halt release condition	Enable the halt release caused by RFC counter to be finished (HRF6)	Enable the halt release caused by Key Scanning (HRF5)	Enable the halt release caused by TMR2 underflow (HRF4)
Halt release enable flag	HEF3	HEF2	HEF1
Halt release condition	Enable the halt release caused by pre-divider overflow (HRF3)	Enable the halt release caused by INT pin (HRF2)	Enable the halt release caused by TM1 underflow (HRF1)

When the halt release enable flag 6 (HEF6) is set, a finish signal from the 16-bit counter of RFC causes the halt mode to be released. In the same manner, when HEF1 to HEF4 are set to 1, the following conditions will cause the halt mode to be released, respectively: an underflow signal from TMR1, the

signal change at the INT pin, an overflow signal from the pre-divider and an underflow signal from TMR2, a 'H' signal from OR-ed output of KI1~4 latch signals.

When the stop release enable flag 5 (SRF5) and the HEF2 are set, the signal change at the INT pin can cause the stop mode to be released. When the stop release enable flag 7 (SRF7) and the HEF5 are set, the 'H' signal from OR-ed output of K1~4 latch signals can cause the stop mode to be released.

2.15.3 CONTROL REGISTER 3 (CTL3)

Control register 3 (CTL3) is organized with 7 bits of interrupt enable flags (IEF) to enable/disable interrupts. The interrupt enable flag (IEF) is set/reset by the SIE* instruction.

The bit pattern of control register 3 (CTL3) is shown below.

Interrupt enable flag	IEF6	IEF5	IEF4
Interrupt request flag	Enable the interrupt request caused by RFC counter to be finished (HRF6)	Enable the interrupt request caused by Key Scanning (HRF5)	Enable the interrupt request caused by TMR2 underflow (HRF4)
Interrupt flag	Interrupt 6	Interrupt 4	Interrupt 4
Interrupt enable flag	IEF3	IEF2	IEF1
Interrupt request flag	Enable the interrupt request caused by pre-divider overflow (HRF3)	Enable the interrupt request caused by INT pin (HRF2)	Enable the interrupt request caused by TM1 underflow (HRF1)
Interrupt flag	Interrupt 3	Interrupt 2	Interrupt 1
Interrupt enable flag	IEF0		
Interrupt request flag	Enable the interrupt request caused by IOC or IOD port signal to be changed (HRF0)		
Interrupt flag	Interrupt 0		

When any of the interrupts are accepted, the corresponding HRFx and the interrupt enable flag (IEF) will be reset to 0 automatically. Therefore, the desirable interrupt enable flag (IEFx) must be set again before exiting from the interrupt routine.

2.15.4 CONTROL REGISTER 4 (CTL4)

Control register 4 (CTL4), being a 3-bit register, is set/reset by SRE instruction.

The following table shows the Bit Pattern of Control Register 4 (CTL4).

Stop release enable flag	SRF7	SRF5	SRF4 (SRF3)
Stop release request flag	Enable the stop release request caused by signal change on KI1~4 (SKI)	Enable the stop release request caused by signal change on INT pin (HRF2)	Enable the stop release request caused by signal change on IOC (IOD)

When the stop release enable flag 7 (SRF7) is set to 1, the input signal change at the KI1~4 pins causes the stop mode to be released. In the same manner, when SRF4 (SRF3) and SRF5 are set to 1, the input

signal changes at the input mode pins of the IOC (IOD) port. The signal change on the INT pin causes the stop mode to be released as well.

Example:

This example illustrates the stop mode released by the port IOC, KI1~4 and INT pin. Assume all of the pins in IOD and IOC have been set to input mode.

```
PLC     25h         ; Reset the HRF0, HRF2 and HRF5.
SHE     24h         ; HEF2 and HEF5 is set so that the signal change at INT or KI1~4 pin
                    ; causes start condition flag 4 or 8 to be set.
SCA     10h         ; SEF4 is set so that the signal changes at port IOC
                    ; cause the start conditions SCF1 to be set.
SRE     0b0h        ; SRF7, 5, 4 are set so that the signal changes at KI1~4 pins, port
                    ; IOC and INT pin cause the stop mode to be released.
STOP                ; Enter the stop mode.

 ……                 ;STOP release

MSC     10h         ; Check the signal change at INT pin that causes the stop mode to be
                    ; released.
MSB     11h         ; Check the signal change at port IOC that causes the stop mode to be
                    ; released.
MCX     12h         ; Check the signal change at KI1~4 pins that causes the stop mode to
                    ; be released.
```

2.16 HALT FUNCTION

The halt function is provided to minimize the current dissipation of the TM8727 when the LCD is operating. During halt mode, the program memory (ROM) is not in operation; only the oscillator circuit, pre-divider circuit, sound circuit, I/O port chattering prevention circuit, and LCD driver output circuit are in operation (If the timer has started operating, the timer counter still operates in the halt mode).

After the HALT instruction is executed, and no halt release signal (SCF1, SCF3, HRF1 ~ 6) is delivered, the CPU enters halt mode.

The following 3 conditions are available to release halt mode:

1. An interrupt is accepted.
   When an interrupt is accepted, the halt mode is released automatically, and the program will enter halt mode again by executing the RTS instruction after completion of the interrupt service. When halt mode is released and an interrupt is accepted, the halt release signal is reset automatically.
2. The signal change specified by the SCA instruction is applied to port IOC (SCF1) or IOD (SCF3).
3. The halt release condition specified by the SHE instruction is met (HRF1 ~ HRF6). When the halt mode is released in either (2) or (3), it is necessary that either the MSB, or the MSC, or the MCX instruction is executed in order to test the halt release signal. It is also necessary to execute the PLC instruction to reset the halt release signal (HRF). Even when the halt instruction is executed, in the state where the halt release signal is delivered, the CPU does not enter the halt mode.

2.17 HEAVY LOAD FUNCTION

When heavy loading (lamp light-up, motor start, etc...) causes a temporary voltage drop in supply voltage, the heavy loading function (set BCF = 1) prevents TM8727 from malfunctioning, especially where a battery with high internal impedance, such as Li battery or alkali battery, is used.

During back up mode, the 32.768 KHz Crystal Oscillator will add an extra buffer in parallel and switch the internal power (BAK) from VDD1 to VDD2 (Li power option only). In this condition, all of the functions in TM8727 will work under the VDD voltage range, causing TM8727 to get better noise immunity.

To shorten the start-up time of 32.768 KHz Crystal oscillator, TM8727 will set the BCF to 1 for initial and can be reset BCF to 0 by executing instruction (RF 02h) when the Ag and Li power mode option is used. In the EXT-V power mode option, however, BCF don't have any affect to system.

Table 2-17-(1) The back-up flag status in different conditions.

	Ag option	Li option	EXT-V option	Remark
Reset cycle	BCF=1	BCF=1	Don't Care	large current
After reset cycle	BCF=1	BCF=1	Don't Care	large current
SF 2 executed	BCF=1	BCF=1	Don't Care	large current
RF 2 executed	BCF=0	BCF=0	Don't Care	

When the heavy load function is performed, the current dissipation will increase.

Table 2-17-(2) Ag power option:

	Initial reset	After reset	STOP mode	SF 2	RF 2
BCF	1	1	1*	1	0
Internal logic	VDD	VDD	VDD	VDD	VDD
Peripheral logic	VDD	VDD	VDD	VDD	VDD

Table 2-17-(3) Li power option:

	Initial reset	After reset	Stop mode	SF 2	RF 2
BCF	1	1	1*	1	0
Internal logic	VDD	VDD	VDD	VDD	1/2 VDD
Peripheral logic	VDD	VDD	VDD	VDD	VDD

Table 2-17-(4) EXT-V power option:

	Initial reset	After reset	Stop mode	SF 2	RF 2
BCF	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care
Internal logic	VDD	VDD	VDD	VDD	VDD
Peripheral logic	VDD	VDD	VDD	VDD	VDD

Note: When the program enters the stop mode, the BCF will set to 1 automatically to insure that the low speed oscillator will start up in a proper condition while stop release occurs.

2.18 STOP FUNCTION (STOP)

The stop function is another solution used to minimize the current dissipation for TM8727. In stop mode, all of the functions in TM8727 are held, including oscillators. All of the LCD corresponding signals (COM and Segment) will output "L" level. In this mode, TM8727 does not dissipate any power in the stop mode. Because the stop mode will set the BCF flag to 1 automatically, it is recommended to reset the BCF flag after releasing the stop mode in order to reduce power consumption.

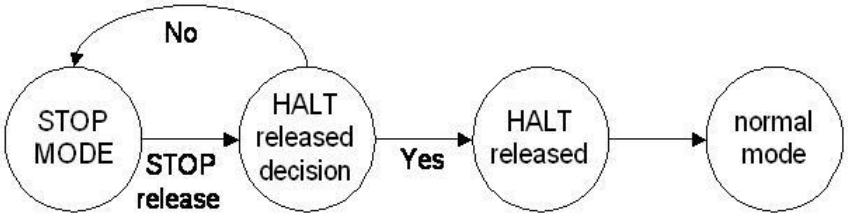
Before the stop instruction is executed, all of the signals on the pins set to input modes on IOD and IOC ports must be in the "L" state, and no stop release signal (SRFn) should be delivered. The CPU will then enter stop mode.

The following conditions cause stop mode to be released.

- One of the signals on the input mode pin of IOD or IOC port is in "H" state and holds long enough to cause the CPU to be released from halt mode.
- A signal change in the INT pin.
- The stop release condition specified by the SRE instruction is met.

When the TM8727 is released from stop mode, the TM8727 enters the halt mode immediately and will process the halt release procedure. If the "H" signal on the IOC (IOD) port does not hold long enough to set the SCF1 (SCF3), once the signal on the IOC port returns to "L", the TM8702 will enter stop mode. The backup flag (BCF) will be set to 1 automatically after the program enters stop mode.

The following diagram shows the stop release state machine procedure.



Before the stop instruction is executed, the following operations must be completed:

- Specify the stop release conditions through the SRE instruction.
- Specify the halt release conditions corresponding to the stop release conditions, if needed.
- Specify the interrupt conditions corresponding to the stop release conditions, if needed.

When stop mode is released by an interrupt request, the TM8727 will enter the halt mode immediately. While the interrupt is accepted, the halt mode will be released by the interrupt request. Stop mode returns by executing the RTS instruction after the completion of interrupt service.

stop release, it is necessary that either the MSB, or the MSC or the MCX instruction be executed to test the halt release signal. Then, the PLC instruction must be executed to reset the halt release signal.

Even when the stop instruction is executed in the state where the stop release signal (SRF) is delivered, the CPU does not enter stop mode, but instead enters halt mode. When stop mode is released and an interrupt is accepted, the halt release signal (HRF) is reset automatically.

2-19. BACK UP FUNCTION

TM8727 provides a back up mode to avoid system malfunction when heavy loading occurs, such as buzzer activation, LED illumination, etc.... Since heavy loading will cause a large voltage drop in the supply voltage, the system will malfunction in this condition.

Once the program enters back up mode (BCF = 1), 32.768 KHz Crystal oscillator will operate in a large driver condition and the internal logic function operates with a higher supply voltage. TM8727 will get a higher power supply noise margin while back up mode is active, but it will also receive an increase in power consumption.

The backup flag (BCF) indicates the status of the backup function. BCF flag can be set or reset by executing the SF or RF instructions, respectively.

The backup function has different performance corresponding to different power mode options, shown in the following table.

1.5V battery mode:

TM8727 status	BCF flag status
Initial reset cycle	BCF = 1 (hardware controlled)
After initial reset cycle	BCF = 1 (hardware controlled)
Executing SF 2h instruction	BCF = 1
Executing RF 2h instruction	BCF = 0
HALT mode	Previous state
STOP mode	BCF = 1 (hardware controlled)

TM8727 status	BCF = 0	BCF = 1
32.768 KHz Crystal Oscillator	Small driver	Large driver
Voltage on BAK pin	VDD1	VDD1
Internal operating voltage	VDD1	VDD1

3V battery or higher mode:

TM8727 status	BCF flag status
Initial reset cycle	BCF = 1 (hardware controlled)
After initial reset cycle	BCF = 1 (hardware controlled)
Executing SF 2h instruction	BCF = 1
Executing RF 2h instruction	BCF = 0
HALT mode	Previous state
STOP mode	BCF = 1 (hardware controlled)

	BCF = 0	BCF = 1
32.768 KHz Crystal Oscillator	Small driver	Large driver
Voltage on BAK pin	VDD1	VDD2
Internal operating voltage	VDD1	VDD2

Ext-V power mode:

TM8727 status	BCF flag status
Initial reset cycle	BCF = 0 (hardware controlled)
After initial reset cycle	BCF = 0 (hardware controlled)
Executing SF 2h instruction	BCF = 1
Executing RF 2h instruction	BCF = 0
HALT mode	Previous state
STOP mode	BCF = 1 (hardware controlled)

	BCF = 0	BCF = 1
32.768 KHz Crystal Oscillator	Large driver	Large driver
Voltage on BAK pin	VDD2	VDD2
Internal operating voltage	VDD2	VDD2

Note: For power saving reasons, it is recommended to reset BCF flag to 0 when back up mode is not used.

3. NTROL FUNCTION

3.1 RRUPT FUNCTION

There are 7 interrupt resources: 3 external interrupt factors and 4 internal interrupt factors. When an interrupt is accepted, the program in execution is suspended temporarily and the corresponding interrupt service routine specified by a fix address in the program memory (ROM) is called.

The following table shows the flag and service of each interrupt:

Table 3-1-(1) Interrupt information

Interrupt source	INT pin	IOC or IOD port	TMR1 underflow	Pre-divider overflow	TMR2 underflow	Key matrix Scanning	RFC counter overflow
Interrupt vector	010H	014H	018H	01CH	020H	024H	028H
Interrupt enable flag	IEF2	IEF0	IEF1	IEF3	IEF4	IEF5	IEF6
Interrupt priority	6th	5th	2nd	1st	3rd	7th	4th
Interrupt request flag	Interrupt 2	Interrupt 0	Interrupt 1	Interrupt 3	Interrupt 4	Interrupt 5	Interrupt 6