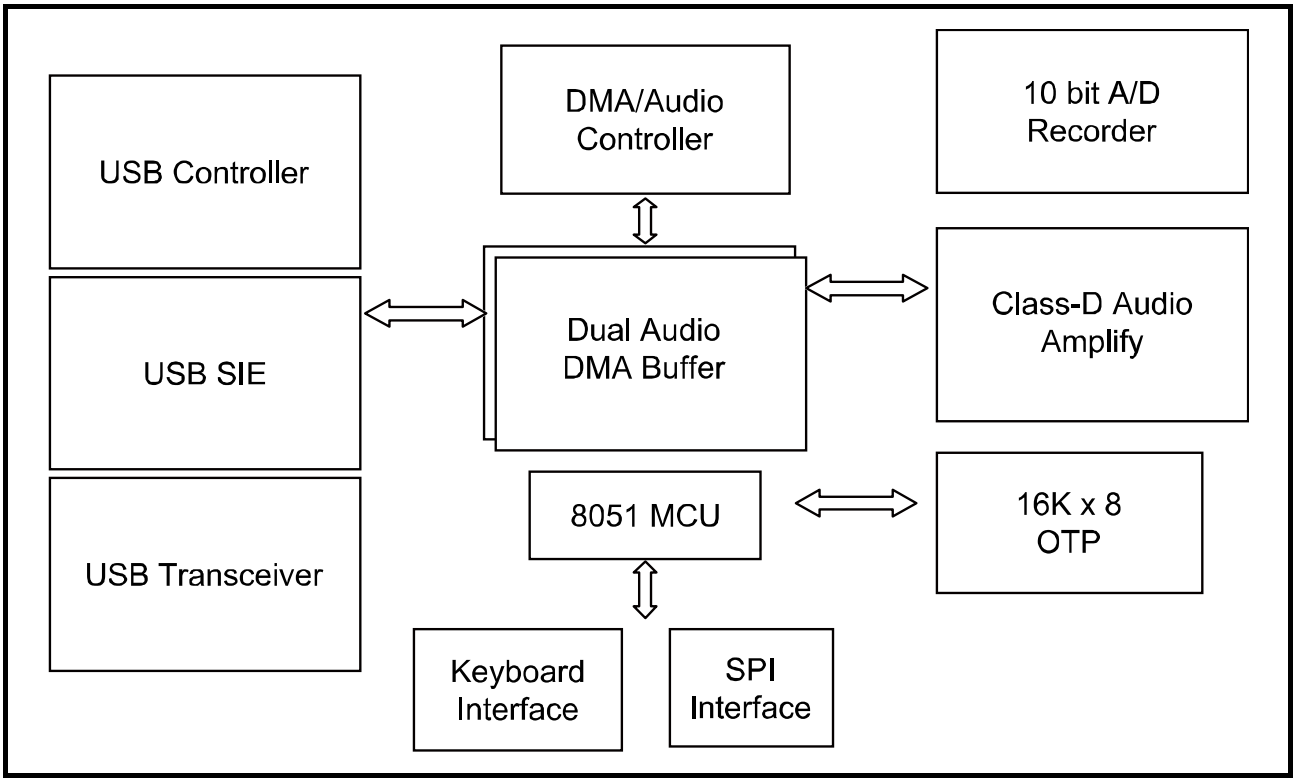
General Description

The TMU6102 is an 8-bit micro-controller embedded device tailored to the USB audio and USB keyboard application. It is able to play two channels PC audio and record one channel voice through Full-Speed USB bus.

FEATURE

1. Compliance with the Universal Serial Bus specification v2.0 Full-Speed
2. Built-in USB Transceiver & 3.3V Regulator
3. Isochronous transfer with adaptive synchronization
4. High performance 48KHz sampling rate for audio playback
5. 24KHz sampling rate for voice recording
6. Two channel audio Class-D Amplify for speaker driving
7. 64-level volume control; VR adjustment available
8. Embedded 10 bits ADC input
9. USB keyboard interface
10. Support USB Suspend function
11. 16K x 8 internal program OTP-ROM
12. Support SPI Interface
13. 12MHz crystal oscillation
14. 48 / 80 pin package

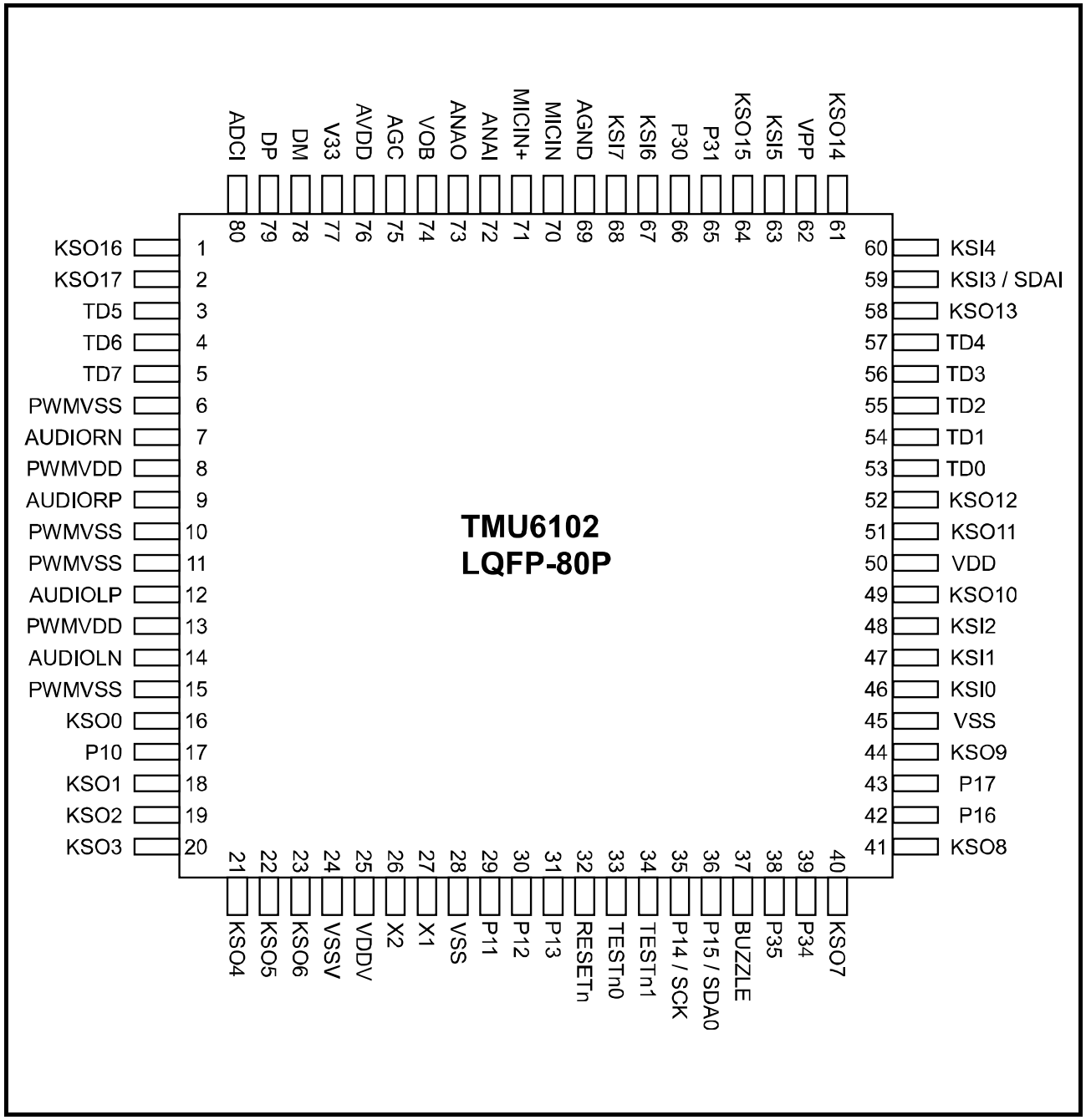
Block Diagram

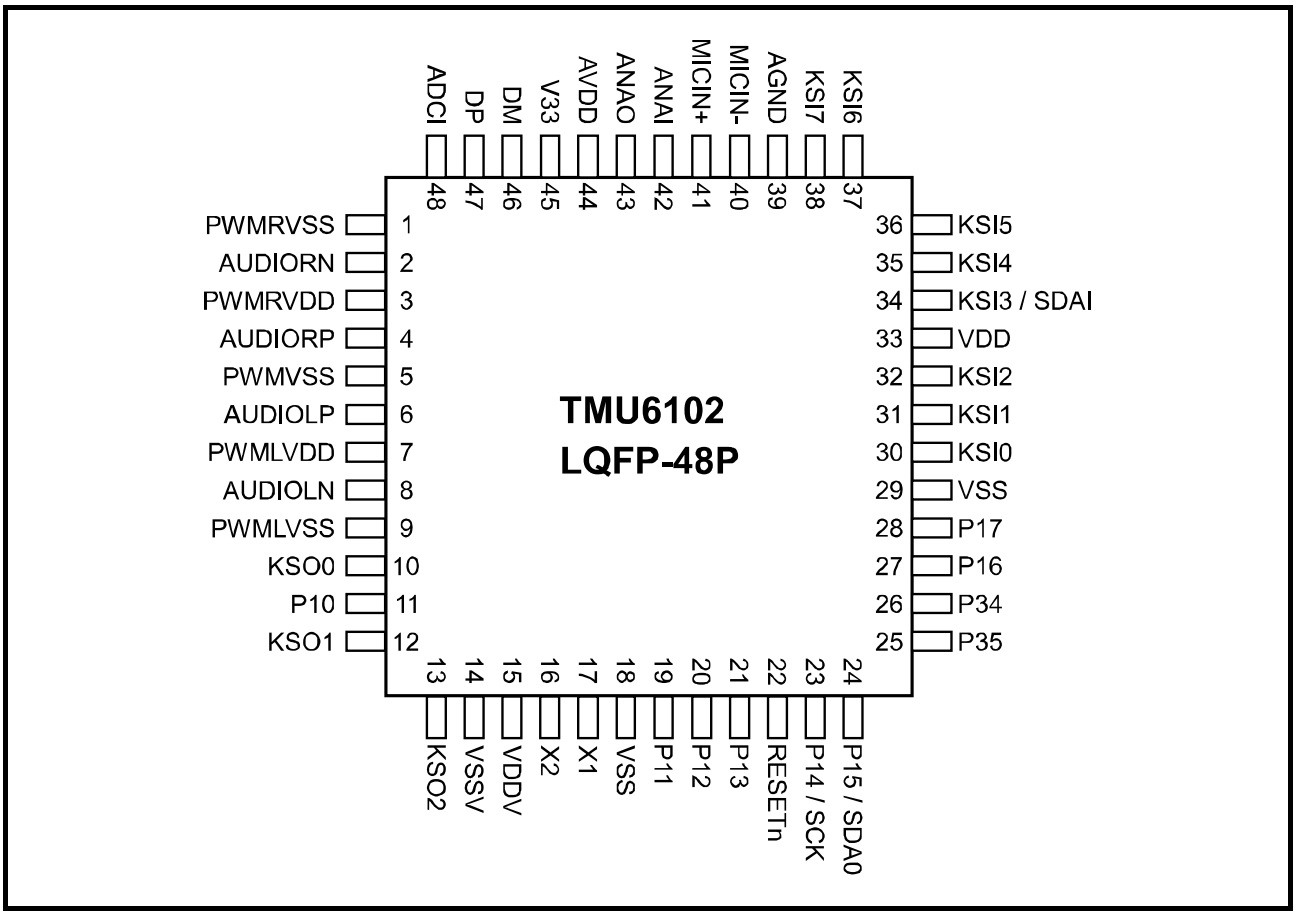


PIN Description

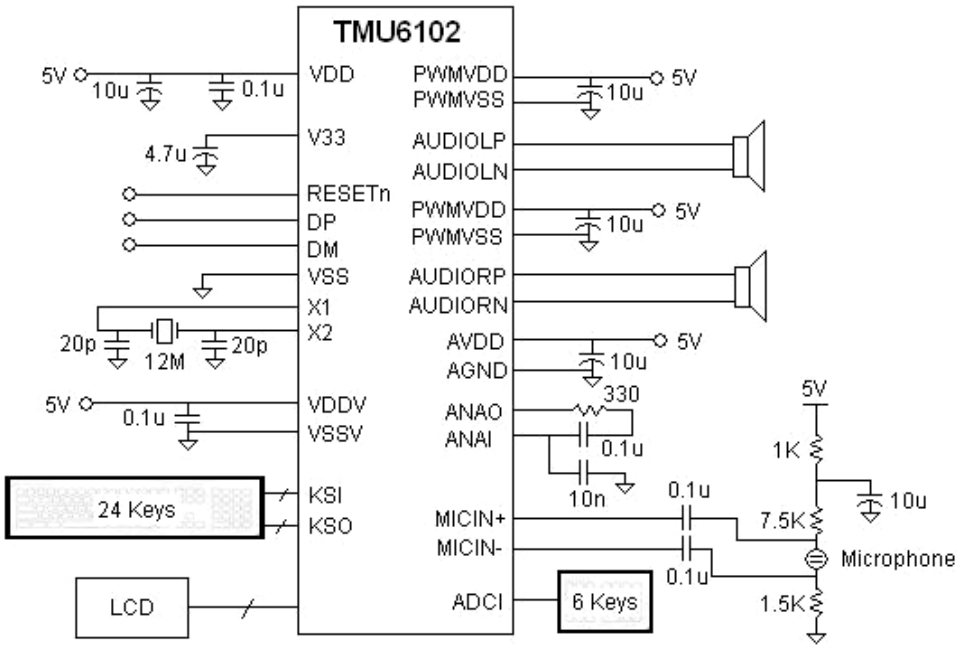
Name	I/O	Description
V33	O	3.3V Regulator output
VSS	P	Ground
VDD	P	5V Power from USB cable
VDDV	P	5V Power for PLL
VSSV	P	Ground for PLL
AVDD	P	5V Power for Recorder
AGND	P	Ground for Recorder
VPP/RSTn	P	High Voltage Power/ Chip reset (active low)
PWMVDD	P	5V Power for Audio Output
PWMVSS	P	Ground for Audio Output
ADC	I	VR input for volume adjustment
X1	I	Crystal in (12MHz)
X2	O	Crystal out
TESTn0	I	Test Mode control bit 0
TESTn1	I	Test Mode control bit 1
DP	I/O	USB positive data signal
DM	I/O	USB negative data signal
AUDIOLP	O	Audio output
AUDIOLN	O	Audio output
AUDIORP	O	Audio output
AUDIORN	O	Audio output
MICIN+	I	MIC IN+
MICIN-	I	MIC IN-
ANAO	O	Recorder AC Couple Out
ANAI	I	Recorder AC Couple In
AGC	I	Recorder AGC
VOB	O	Recorder VOB Connect 25K Resister to Ground when register setting use External resister
BUZZLE	O	Buzzer
KSI[7:0]	I	Key-scan Input
KSO[17:0]	O	Key-scan Output
P1[7:0]	I/O	General purpose I/O
P3[5,4,1,0]	I/O	General purpose I/O
TDI[7:0]	I/O	TESTER I/O

Pin Assignment Diagram

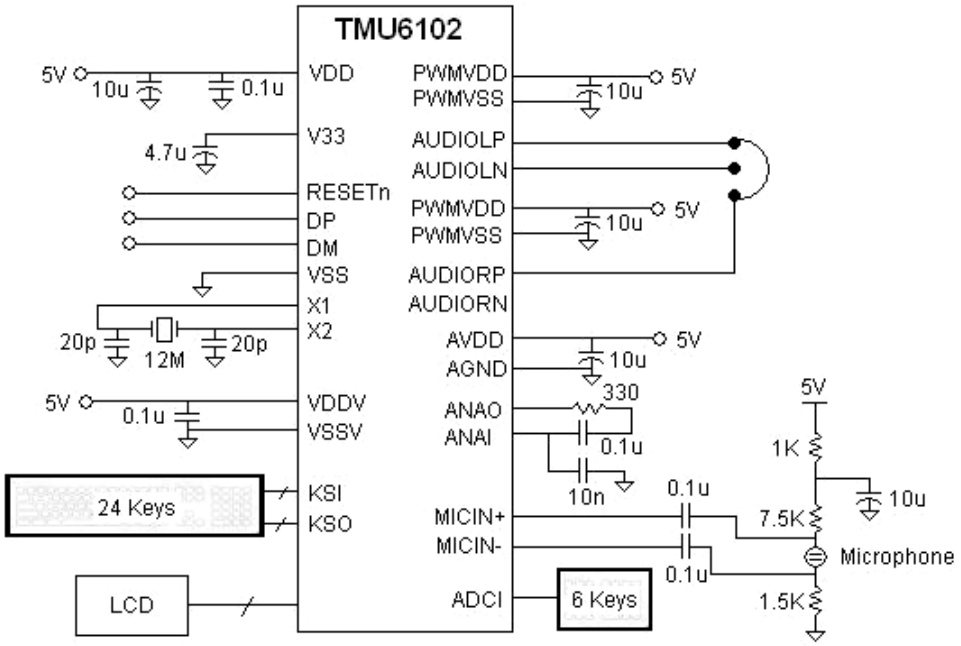




APPLICATION CIRCUIT



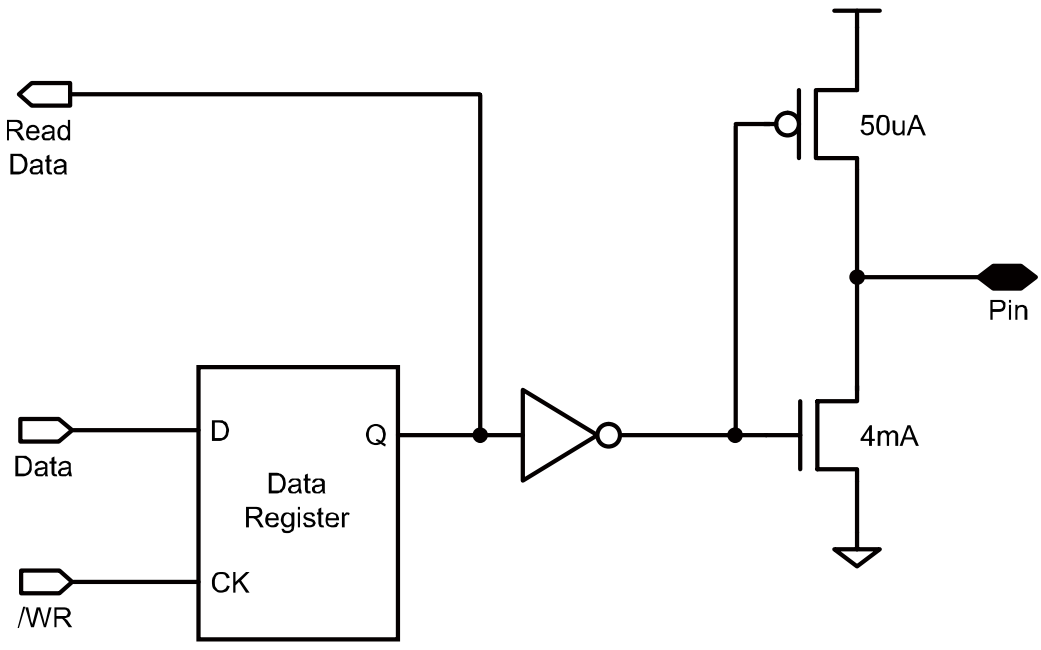
Speaker Application



Earphone Application

KSO[17:0]

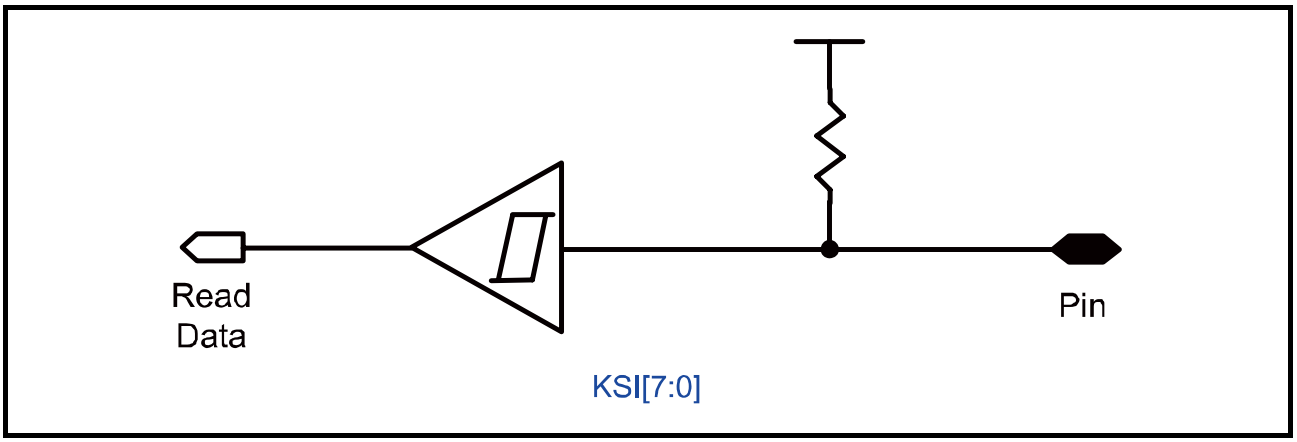
These pins are used as keyboard scan outputs. They have at least 4mA drive and sink strength.



KSO[17:0]

KSI[7:0]

These pins are used as keyboard scan inputs. Each one of them has a pull up resistor. In addition, each KSI pin can cause Keyboard interrupt (KBDint) if the corresponding interrupt mask bit (KBDmask) is 0. The KBDint is asserted at the falling edge of KSI pin.



ABSOLOUTE MAXIMUM RATINGS

GND= 0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to 5.5	V
Maximum Input Voltage	Vin	-0.3 to VDD+0.3	V
Maximum output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	-20 to +70	℃
Maximum Storage Temperature	Tstg	-25 to +125	℃

OPERATING CONDITION

at Ta= -20℃ to 70℃, GND= 0V

Name	Symb.	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	4.5		5.5	V
Input “H” Voltage	Vih	4.0		5.5	V
Input “L” Voltage	Vil	0		1.0	V
Crystal frequency	Fosc		12		MHz

ELECTRICAL PARAMETER

at Ta= -20℃ to 70℃, GND= 0V

Name	Symb.	Typ	Unit
Maximum Audio Output Current per Channel @ 8ohm Load	Iout	453	mA

DC ELECTRICAL CHARACTERISTICS

at Ta=-25 ℃, VDD5=5.0V, VSS= 0V, Fosc=12MHz

Name	Symb.	Min.	Typ.	Max.	Unit	Condition	Note
Operating current	Icc		50		mA	Fosc=12MHz	
KSO Output High Voltage	Voh1		4.0		V	Ioh=40uA	
KSO Output Low Voltage	Vol		0.4		V	Iol=16mA	
P1/P3 Output High Voltage	Voh		4.0		V	Ioh=30uA	
P1/P3 Output Low Voltage	Vol		0.4		V	Iol=14mA	
LED(P3.5) Output Low Voltage	Vol		0.4		V	Iol=34mA	
V33 output voltage	V33	3.2		3.4	V	VDD=5V	

Register Mapping

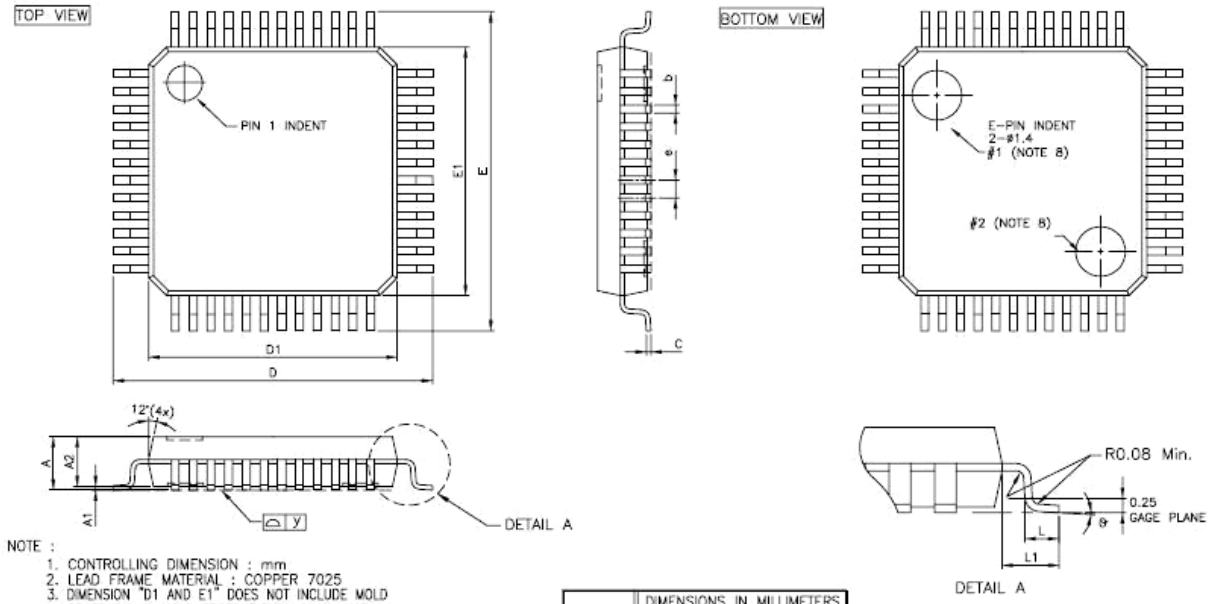
Name	Address	R/W	Rst	Description
PWRdwn	1F00	W	0	Write this register to enter Power-Down Mode
WDTe	1F01	W	0	Clear WDT and enable WDT
TESTreg	1F02.3~0	W	0	Test Mode option. Keep “0” in normal mode.
SET0ie	1F03.7	W	0	SET0Int Interrupt enable
TX0ie	1F03.6	W	0	TX0Int Interrupt enable
RC1ie	1F03.5	W	0	RC1Int Interrupt enable
TX2IE	1F03.4	W	0	TX2Int Interrupt enable
TX3IE	1F03.3	W	0	TX3Int Interrupt enable
RSTie	1F03.2	W	0	RSTInt Interrupt enable
RSMIE	1F03.1	W	0	RSMInt Interrupt enable
SUSPIE	1F03.0	W	0	SUSPInt Interrupt enable
TX4IE	1F04.7	W	0	TX4Int Interrupt enable
KBDIE	1F04.6	W	0	KBDInt Interrupt enable
OUT0IE	1F04.5	W	0	OUT0INT Interrupt enable
RC5IE	1F04.4	W	0	RC5INT Interrupt Enable
SET0Int	1F05.7	R/W	0	Endpoint 0 Setup Token receive Interrupt flag, write 0 to clear flag.
TX0Int	1F05.6	R/W	0	Endpoint 0 Transmit Interrupt flag, write 0 to clear flag.
RC1Int	1F05.5	R/W	0	Endpoint 1 Receive Interrupt flag, write 0 to clear flag.
TX2Int	1F05.4	R/W	0	TX2 Interrupt flag, write 0 to clear flag.
TX3Int	1F05.3	R/W	0	TX3 Interrupt flag, write 0 to clear flag.
RSTInt	1F05.2	R/W	0	USB Bus Reset Interrupt flag, write 0 to clear flag.
RSMInt	1F05.1	R/W	0	USB Resume Interrupt flag, write 0 to clear flag.
SUSPInt	1F05.0	R/W	0	USB Suspend Interrupt flag, write 0 to clear flag.
TX4Int	1F06.7	R/W	0	TX4 Interrupt flag, write 0 to clear flag.
KBDInt	1F06.6	R/W	0	Keyboard Interrupt flag, write 0 to clear flag.
OUT0INT	1F06.5	R/W	0	Endpoint 0 OUT Token receive Interrupt flag, write 0 to clear flag
RC5INT	1F06.4	R/W	0	Endpoint 5 Receive Interrupt flag, write 0 to clear flag
RVOL	1F07.7~2	R/W	0	Right Channel Volume
LVOL	1F08.7~2	R/W	0	Left Channel Volume
CKFAST	1F09.7	R/W	0	0: 12M clock to 8051, 1:32M clock to 8051
EARDT	1F09.3	R	0	Earphone detect
LOUD2	1F09.1	R/W	0	Loud2 mode
EARPHONE	1F09.0	R/W	0	Earphone mode
PWMon	1F0A.7	R/W	0	PWM function enable
USBadr	1F0A.6~0	R/W	0	USB function address

Susp	1F0B.7	R/W	0	S/W force USB interface into suspend mode.
Rsmo	1F0B.6	R/W	0	S/W force USB interface send RESUME signal in suspend mode.
EP1cfg	1F0B.5	R/W	0	Set Endpoint 1 configured
RC0rdy	1F0B.0	R/W	0	Endpoint 0 ready for receive, clear by H/W while RC0I occurs.
TX0rdy	1F0C.6	R/W	0	Endpoint 0 ready for transmit, clear by H/W while TX0I occurs.
TX0tgl	1F0C.5	R/W	0	Endpoint 0 transmit DATA1/DATA0 packet.
EP0stall	1F0C.4	R/W	0	Endpoint 0 will stall OUT/IN packet.
TX0cnt	1F0C.3~0	R/W	0	Endpoint 0 transmit byte count.
EP2CFG	1F0D.7	R/W	0	Set Endpoint 2 configured
TX2rdy	1F0D.6	R/W	0	Endpoint 2 ready for transmit, clear by H/W while TX2I occurs.
TX2tgl	1F0D.5	R/W	0	Endpoint 2 transmit DATA1/DATA0 packet.
EP2stall	1F0D.4	R/W	0	Endpoint 2 will stall OUT/IN packet.
TX2cnt	1F0D.3~0	R/W	0	Endpoint 2 transmit byte count.
EP3CFG	1F0E.7	R/W	0	Set Endpoint 3 configured
CLR_RC1CNT	1F0E.6	W	1	write 0 to clear RC1CNT(Reg. 1F1E)
TX3cnt	1F0F.6~0	R/W	0	Endpoint 3 transmit byte count.
EP4CFG	1F10.7	R/W	0	Set Endpoint 4 configured
TX4rdy	1F10.6	R/W	0	Endpoint 4 ready for transmit, clear by H/W while TX2I occurs.
TX4tgl	1F10.5	R/W	0	Endpoint 4 transmit DATA1/DATA0 packet.
EP4stall	1F10.4	R/W	0	Endpoint 4 will stall OUT/IN packet.
TX4cnt	1F10.3~0	R/W	0	Endpoint 4 transmit byte count.
RC0tgl	1F11.7	R		1: received DATA1 packet; 0: received DATA0 Packet.
RC0err	1F11.6	R		Endpoint 0 received data error.
EP0dir	1F11.5	R		1: IN transfer; 0: OUT/SETUP transfer.
EP0set	1F11.4	R		SETUP Token indicator.
OUT0cnt	1F11.3~0	R		OUT0 Received data byte count.
HW_WRPWM	1F12.2	R/W	1	1:PWM BUF is filled by HW; 0: by FW
MIC2PWM	1F12.1	R/W	0	1: Enable MIC data write to PWM buf (MIC buf is necessary) 0: MIC data only write to MIC buf
RECS	1F12.0	R/W	0	MIC Record Start
KSO[7:0]	1F13	R/W	1	Key Scan output [7:0]
KSO[15:8]	1F14	R/W	1	Key Scan output [15:8]
KSI[7:0]	1F15	R		Key Scan input [7:0]
KBDMASK	1F16	W	0	mask KSI[7:0] interrupt function while the corresponding bit is "1"
KSO[17:16]	1F17.1~0	R/W	1	Key Scan output [17:16]
ADC	1F18.5~0	R		ADC Voltage (1KHz sampling)
BZE	1F19.7	W	0	Buzzer Output Enable
BZ_DV_RATIO	1F19.6~0	W	0	Buzzer Clock Divide Ratio
DIS_VREF	1F1A.7	W	0	Disable Vref
REF2VOB	1F1A.6	W	0	Enable ref voltage to VOB
EN_INT_R	1F1A.5	W	1	Enable MIC ADC Internal Resister
PGC_AGCN	1F1A.4	W	0	MIC ADC PGC/AGC select 0:AGC, 1:PGC
FLT_EN	1F1A.3	W	0	MIC ADC Filter Enable
PCTL[2:0]	1F1A.2~0	W	0	MIC ADC PCTL
RC5TGL	1F1B.7	R		1: received DATA1 packet; 0: received DATA0 Packet.
RC5ERR	1F1B.6	R		Endpoint 5 received data error.
EP5STALL	1F1B.5	R/W	0	Endpoint 5 will stall OUT/IN packet.
EP5CFG	1F1B.4	R/W	0	Set Endpoint 5 configured

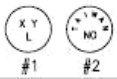
RC5RDY	1F1B.3	R/W	0	Endpoint 5 ready for receive, clear by H/W while RC5I occurs.
RC5CNT[3:0]	1F1C.3~0	R		OUT5 Received data byte count.
ADCQ[9:2]	1F1D	R	-	ADCQ[9:2] data
RC1CNT	1F1E	R	-	RC1CNT
SET0FIFO	1F20~1F27	R		Endpoint 0 SET Receive Buffer (8 Bytes)
OUT0FIFO	1F40~1F47	R		Endpoint 0 OUT Receive Buffer (8 Bytes)
TX0FIFO	1F20~1F27	W		Endpoint 0 Transmit Buffer (8 Bytes)
TX2FIFO	1F28~1F2F	W		Endpoint 2 Transmit Buffer (8 Bytes)
TX4FIFO	1F30~1F37	W		Endpoint 4 Transmit Buffer (8 Bytes)
OUT5FIFO	1F48~1F4F	R		Endpoint 5 Receive Buffer (8 Bytes)
SPI_MODE	1F5A.7	W	0	1: Set SPI MODE
CPOL	1F5A.6	W	0	SPI Clock Polarity
CPHA	1F5a.5	W	0	SPI Clock Phase
IS_BUSY	1F5A.0	R	0	SPI Busy bit
SPI_EN	1F5B.7	W	0	Enable SPI
CRS[6:0]	1F5B.6~0	W	0	SPI Clock Select
SPI_RX_DATA	1F5C	R	-	SPI Receive data
SPI_TX_DATA	1F5D	W	0	SPI Transmit data

Package Information

- LQFP 48 PIN



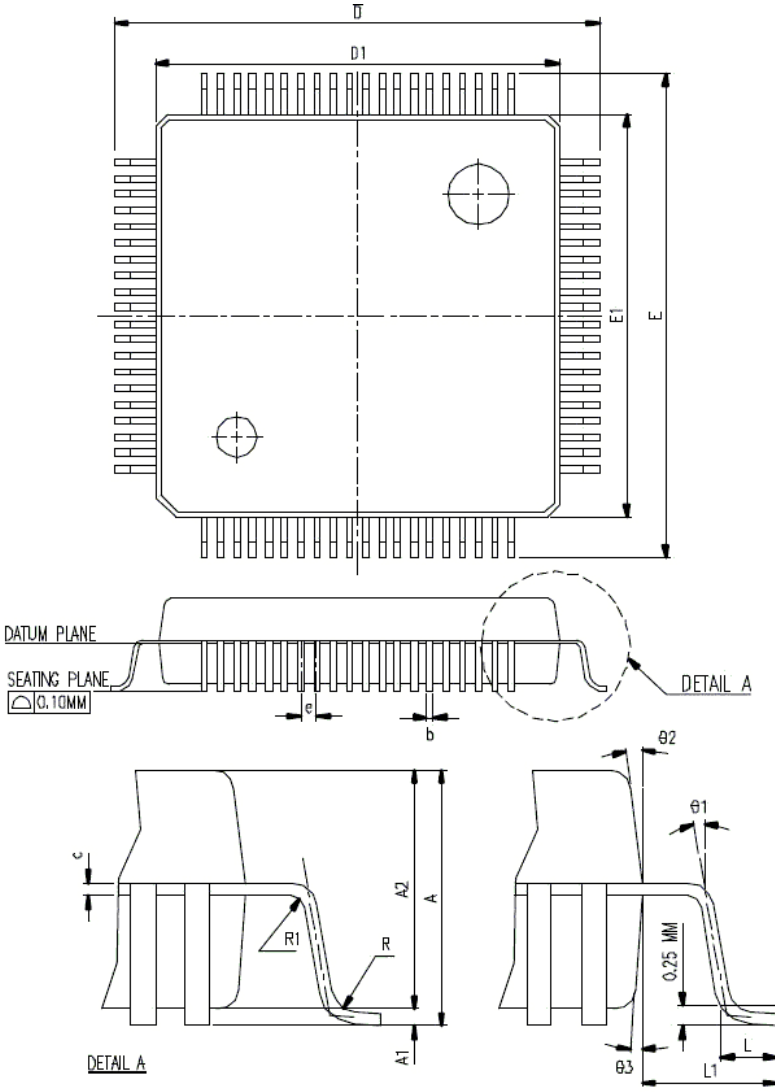
NOTE :
1. CONTROLLING DIMENSION : mm
2. LEAD FRAME MATERIAL : COPPER 7025
3. DIMENSION "D1 AND E1" DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-026-BBC
8. BOTTOM E-PIN INDENT IN MARKED AS BELOW :



X : A, B, C,...
Y : 1 ~ 12
NO : DENOTE MOLD SET NUMBER

SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
C	0.09	—	0.20
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
e	—	0.50	—
L	0.45	0.60	0.75
L1	—	1.00	—
θ	0°	3.5°	7°
y	0.0	—	0.08

- LQFP 80 PIN



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN	NOM	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09		0.16	0.004		0.006
e	0.40 BASIC			0.016 BASIC		
D	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	12.00 BASIC			0.472 BASIC		
E1	10.00 BASIC			0.394 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BCE)					

⚠ *NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.