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TM8762

DATA SHEET

Rev 1.2

AMENDMENT HISTORY

Version	Date	Description
1.0	Jun, 2015	New release
1.1	Dec, 2016	modify P.13 Voh1d, Voh1e from 1.0V to 2.2V
1.2	Jul, 2023	P.14 Application circuit 1.5V -> 3V

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GENERAL DESCRIPTION

The TM8762 is an embedded high-performance 4-bit microcomputer with LCD/LED driver. It contains all the necessary functions, such as 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock operation, Resistance to Frequency Converter(RFC), EL panel driver, LCD driver, look-up table, watchdog timer and key matrix scanning circuitry in a signal chip.

FEATURE

1. Low power dissipation.

2. Powerful instruction set (143 instructions).

- Binary addition, subtraction, BCD adjust, logical operation in direct and index addressing mode.
- Single-bit manipulation (set, reset, decision for branch).
- Various conditional branch.
- 16 working registers and manipulation.
- Table look-up.
- LCD driver data transfer.

3. Memory capacity.

- ROM capacity 2048 x 16 bits.
- RAM capacity 128 x 4 bits.

4. LCD/LED driver output.

- 5 common outputs and 35 segment outputs (up to drive 175 LCD/LED segments).
- 1/2 Duty, 1/3 Duty, 1/4 Duty or 1/5 Duty for both LCD/LED drivers is selected by mask option.
- 1/2 Bias or 1/3 Bias for LCD driver is selected by mask option.
- Single instruction to turn off all segments.
- All segment outputs could be defined as CMOS or P_open drain output type by mask option.

5. Input/output ports.

- Port IOA 4 pins (with internal pull-low), muxed with SEG24~27.
- Port IOB 4 pins (with internal pull-low), muxed with SEG28~31.
- Port IOC 4 pins (with internal pull-low/low-level-hold), muxed with SEG32~35. IOC port had built in the input signal chattering prevention circuitry.

6. 8 level subroutine nesting.

7. Interrupt function.
- External factors 3 (INT pin, Port IOC & KI input).
- Internal factors 4 (Pre-Divider, Timer1, Timer2 & RFC).

8. Built-in EL panel driver.
- ELC, ELP (Muxed with SEG28, SEG29).

9. Built in Alarm, clock or single tone melody generator.
- BZB, BZ (Muxed with SEG30, SEG31).

10. Built-in R to F Converter circuit.
- CX, RR, RT, RH (Muxed with SEG24~SEG27).

11. Built in key matrix scanning function.
- K1~K16 (Shared with SEG1~SEG16).
- KI1~KI4 (Muxed with SEG32~SEG35).

12. Two 6-bit programmable timer with programmable clock source.

13. Watch dog timer.

14. Built-in Voltage doubler, halver, tripler charge pump circuit.

15. Dual clock operation
- slow clock oscillation can be defined as X'tal or external RC type oscillator by mask option.
- fast clock oscillation can be defined as internal R or external R type oscillator by mask option.

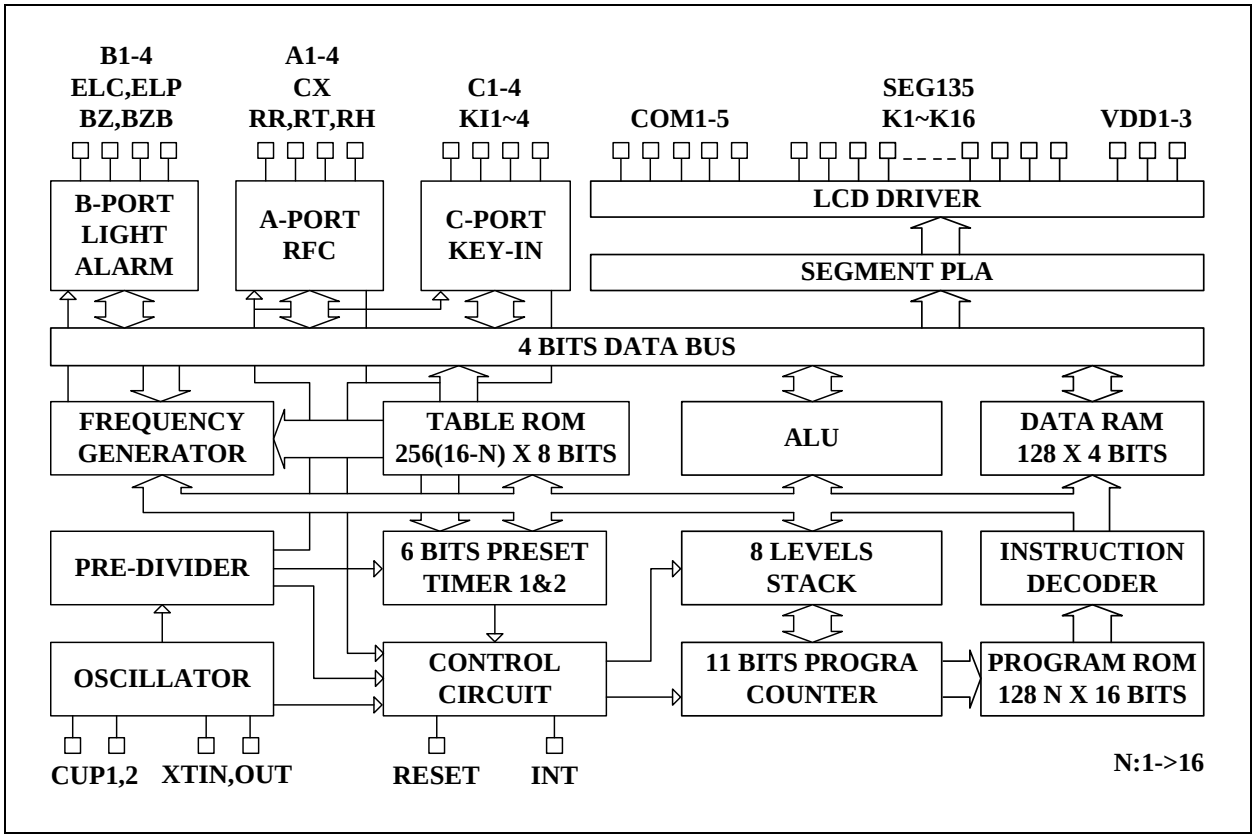
16. HALT function.

17. STOP function.

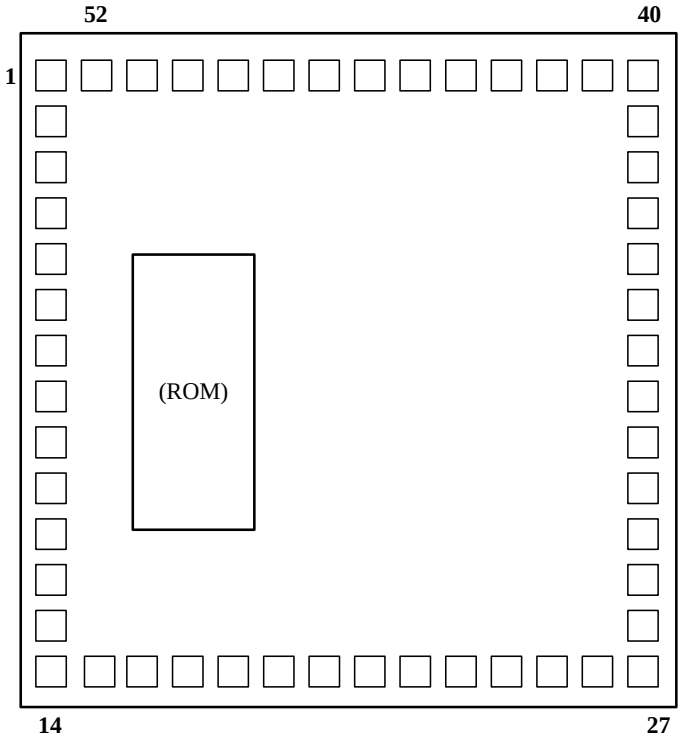
APPLICATION

■ Timer / Calendar / Calculator / Thermometer

BLOCK DIAGRAM



PAD DIAGRAM



The substrate of chip should be connected to GND.

PAD COORDINATE

No	Name	No	Name
1	BAK	27	SEG13/K13
2	XIN	28	SEG14/K14
3	XOUT	29	SEG15/K15
4	GND	30	SEG16/K16
5	VDD1	31	SEG17
6	VDD2	32	SEG18
7	VDD3	33	SEG19
8	CUP1	34	SEG20
9	CUP2	35	SEG21
10	COM1	36	SEG22
11	COM2	37	SEG23
12	COM3	38	SEG24/IOA1/CX
13	COM4	39	SEG25/IOA2/RR
14	COM5	40	SEG26/IOA3/RT
15	SEG1/K1	41	SEG27/IOA4/RH
16	SEG2/K2	42	SEG28/IOB1/ELC
17	SEG3/K3	43	SEG29/IOB2/ELP
18	SEG4/K4	44	SEG30/IOB3/BZB
19	SEG5/K5	45	SEG31/IOB4/BZ
20	SEG6/K6	46	SEG32/IOC1/KI1
21	SEG7/K7	47	SEG33/IOC2/KI2
22	SEG8/K8	48	SEG34/IOC3/KI3
23	SEG9/K9	49	SEG35/IOC4/KI4
24	SEG10/K10	50	RESET
25	SEG11/K11	51	INT
26	SEG12/K12	52	TEST

PIN DESCRIPTION

Name	I/O	Description
BAK	P	Positive Back-up voltage. At Li power Mode, connect a 0.1u capacitor to GND.
VDD1,2,3	P	LCD supply voltage, and positive supply voltage. • In Ag Mode, connect positive power to VDD1. • In Li or ExtV power mode, connect positive power to VDD2.
RESET	I	Input pin for external reset request signal, built-in internal pull-down resistor.
INT	I	Input pin for external INT request signal. • Falling edge or rising edge triggered is defined by mask option. • Internal pull-down or pull-up resistor is defined by mask option.
TESTA		Test signal input pin.
CUP1,2	O	Switching pins for supply the LCD driving voltage to the VDD1,2,3 pins. • Connect the CUP1 and CUP2 pins with non-polarized electrolytic capacitor when chip operated in 1/2 or 1/3 bias mode. • In no BIAS mode application, leave these pins opened.
XIN XOUT	I O	Time base counter frequency (clock specified. LCD alternating frequency. Alarm signal frequency) or system clock oscillation. • 32KHz Crystal oscillator. • In FAST mode, connect an external resistor could compose the RC oscillator (mask option). • In SLOW mode, connect an external resistor could compose the RC oscillator (mask option).
COM1~5	O	Output pins for driving the common pins of the LCD or LED panel.
SEG1-35	O	Output pins for driving the LCD or LED panel segment.
IOA1-4	I/O	Input / Output port A. (Muxed with SEG24~SEG27)
IOB1-4	I/O	Input / Output port B. (Muxed with SEG28~SEG31)
IOC1-4	I/O	Input / Output port C. (Muxed with SEG32~SEG35)
CX RR/RT/RH	I O	1 input pin and 3 output pins for RFC application. (Muxed with SEG24~SEG27)
ELC/ELP	O	Output port for EL panel driver. (Muxed with SEG28,SEG29)
BZB/BZ	O	Output port for alarm, clock or single tone melody generator. (Muxed with SEG30~SEG31)
K1~K16	O	Output port for key matrix scanning.(Shared with SEG1~SEG16)
KI1~4	I	Input port for key matrix scanning.(Muxed with SEG32~SEG35)
GND	P	Negative supply voltage.

ABSOLOUTE MAXIMUM RATINGS

GND= 0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD1	-0.3 to 5.5	V
	VDD2	-0.3 to 5.5	
	VDD3	-0.3 to 8.5	
Maximum Input Voltage	Vin	-0.3 to VDD1/2+0.3	
Maximum output Voltage	Vout1	-0.3 to VDD1/2+0.3	
	Vout2	-0.3 to VDD3+0.3	
Maximum Operating Temperature	Topg	-20 to +70	℃
Maximum Storage Temperature	Tstg	-25 to +125	

POWER CONSUMPTION

at Ta=-20℃ to 70℃,GND= 0V

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
HALT mode	IHALT1	Only 32.768KHz Crystal oscillator operating, without loading. Ag mode, VDD1=1.5V, BCF = 0		2	5	uA
	IHALT2	Only 32.768KHz Crystal oscillator operating, without loading. Li mode, VDD2=3.0V, BCF = 0		2	5	
STOP mode	ISTOP				1	

Note: When RC oscillator function is operating, the current consumption will depend on the frequency of oscillation.

ALLOWABLE OPERATING CONDITIONS

at Ta=-20℃ to 70℃,GND= 0V

Name	Symb.	Condition	Min.	Max.	Unit
Supply Voltage	VDD1		1.2	5.25	V
	VDD2		2.4	5.25	
	VDD3		2.4	8.0	
Oscillator Start-Up Voltage	VDDB	Crystal Mode	1.3		
Oscillator Sustain Voltage	VDDB	Crystal Mode	1.2		
Supply Voltage	VDD1	Ag Mode	1.2	1.65	
Supply Voltage	VDD2	EXT-V, Li Mode	2.4	5.25	
Input “H” Voltage	Vih1	Ag Battery Mode	VDD1-0.7	VDD1+0.7	
Input “L” Voltage	Vil1		-0.7	0.7	
Input “H” Voltage	Vih2	Li Battery Mode	VDD2-0.7	VDD2+0.7	
Input “L” Voltage	Vil2		-0.7	0.7	
Input “H” Voltage	Vih3	OSCIN at Ag Battery Mode	0.8xVDD1	VDD1	
Input “L” Voltage	Vil3		0	0.2xVDD1	
Input “H” Voltage	Vih4	OSCIN at Li Battery Mode	0.8xVDD2	VDD2	
Input “L” Voltage	Vil4		0	0.2xVDD2	
Input “H” Voltage	Vih5	CFIN at Li Battery or EXT-V Mode	0.8xVDD2	VDD2	
Input “L” Voltage	Vil5		0	0.2xVDD2	
Input “H” Voltage	Vih6	RC Mode	0.8xVDDO	VDDO	
Input “L” Voltage	Vil6		0	0.2xVDDO	
Operating Freq	Fopg1	Crystal Mode	32		KHz
	Fopg2	RC Mode	10	1000	

INTERNAL RC FREQUENCY RANGE

Option Mode	BAK	Min.	Typ.	Max.
250KHz	1.5V	200KHz	300KHz	400KHz
	3.0V	200KHz	250KHz	300KHz
500KHz	1.5V	450KHz	600KHz	750KHz
	3.0V	400KHz	500KHz	600KHz

ALLOWABLE OPERATING FREQUENCY

at Ta=-20℃ to 70℃,GND= 0V

Condition	Max, Operating Frequency
BAK=1.5V (VDD1)	800KHz
BAK=3V (VDD2)	4MHz

ELECTRICAL CHARACTERISTICS

at#1:VDD1=1.2V(Ag);

at#2:VDD2=2.4V(Li):

at#3:VDD2=4V(Ext-V);

Input Resistance

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
"L" Level Hold Tr(IOC)	Rllh1	Vi=0.2VDD1,#1	10	40	100	KΩ
	Rllh2	Vi=0.2VDD2,#2				
	Rllh3	Vi=0.2VDD2,#3	5	20	50	
IOA/B/C Pull-Down Tr	Rmad1	Vi=VDD1,#1	200	500	1000	
	Rmad2	Vi=VDD2,#2				
	Rmad3	Vi=VDD2,#3	100	250	500	
INT Pull-up Tr	Rintu1	Vi=VDD1,#1	200	500	1000	
	Rintu2	Vi=VDD2,#2				
	Rintu3	Vi=VDD2,#3	100	250	500	
INT Pull-Down Tr	Rintd1	Vi=GND,#1	200	500	1000	
	Rintd2	Vi=GND,#2				
	Rintd3	Vi=GND,#3	100	250	500	
RES Pull-Down R	Rres1	Vi=GND or VDD1,#1	10	40	100	
	Rres2	Vi=GND or VDD2,#2				
	Rres3	Vi=GND or VDD2,#3				

Dc Output Characteristics

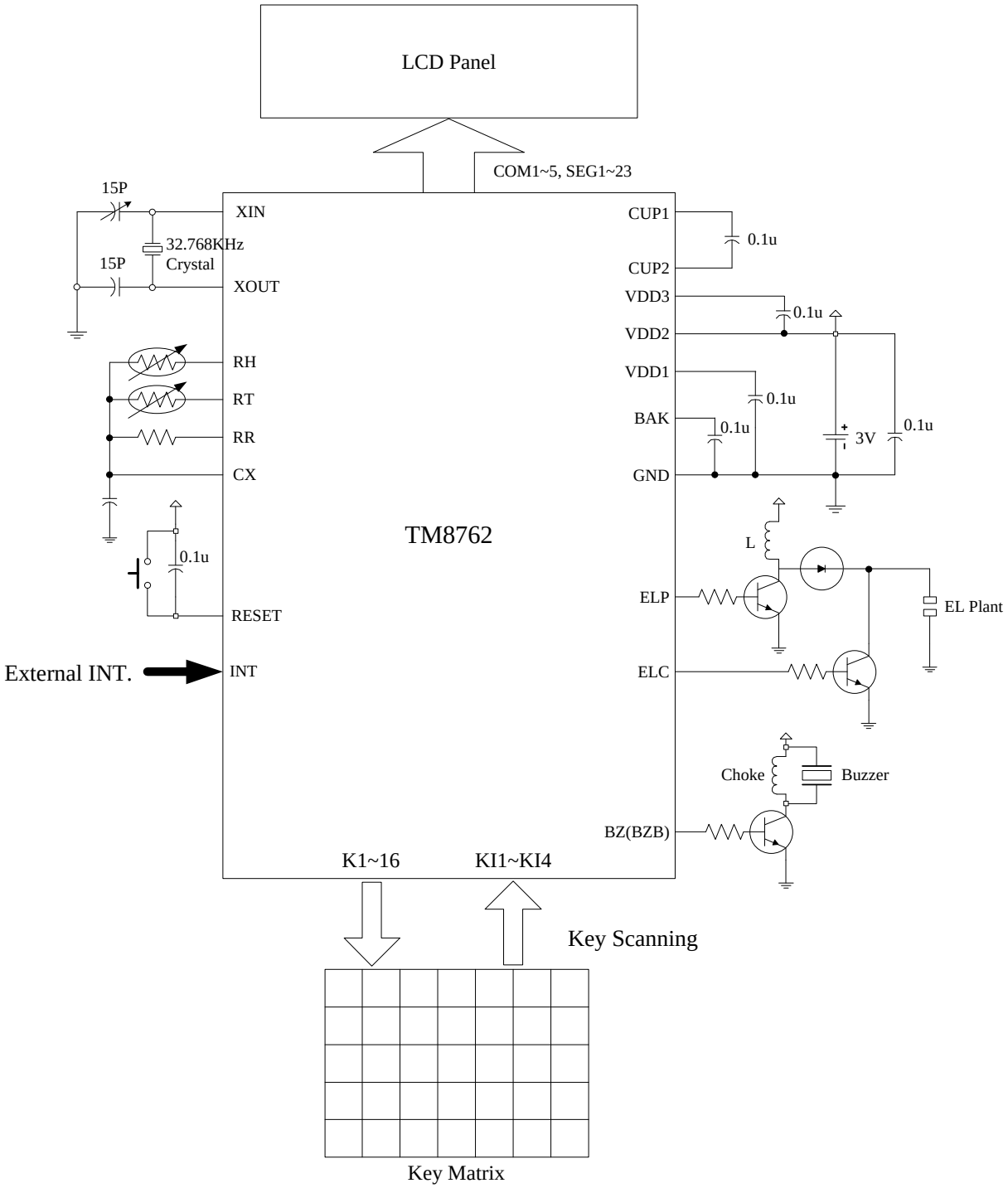
Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output "H" Voltage	Voh1c	Ioh=-200uA,#1	SEG1~35	0.8	0.9	1.0	V
	Voh2c	Ioh=-1mA,#2		1.5	1.8	2.1	
	Voh3c	Ioh=-3mA,#3		2.5	3.0	3.5	
Output "L" Voltage	Vol1c	Iol=400uA,#1		0.2	0.3	0.4	
	Vol2c	Iol=2mA,#2		0.3	0.6	0.9	
	Vol3c	Iol=6mA,#3		0.5	1.0	1.5	

Segment Driver Output Characteristics

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit
Static Display Mode							
Output ”H” Voltage	Voh1d	Ioh=-1uA,#1	SEG-n	2.2			V
	Voh2d	Ioh=-1uA,#2		2.2			
	Voh3d	Ioh=-1uA,#3		3.8			
Output ”L” Voltage	Vol1d	Iol=1uA,#1				0.2	
	Vol2d	Iol=1uA,#2				0.2	
	Vol3d	Iol=1uA,#3				0.2	
Output ”H” Voltage	Voh1e	Ioh=-10uA,#1	COM-n	2.2			
	Voh2e	Ioh=-10uA,#2		2.2			
	Voh3e	Ioh=-10uA,#3		3.8			
Output ”L” Voltage	Vol1e	Iol=10uA,#1				0.2	
	Vol2e	Iol=10uA,#2				0.2	
	Vol3e	Iol=10uA,#3				0.2	
1/2 Bias Display Mode							
Output ”H” Voltage	Voh12f	Ioh=-1uA,#1,#2	SEG-n	2.2			V
	Voh3f	Ioh=-1uA,#3		3.8			
Output ”L” Voltage	Vol12f	Iol=1uA,#1,#2				0.2	
	Vol3f	Iol=1uA,#3				0.2	
Output ”H” Voltage	Voh12g	Ioh=-10uA,#1,#2	COM-n	2.2			
	Voh3g	Ioh=-10uA,#3		3.8			
Output ”M” Voltage	Vom12g	Iol/h=+/-10uA,#1,#2		1.0		1.4	
	Vom3g	Iol/h=+/-10uA,#3		1.8		2.2	
Output ”L” Voltage	Vol12g	Iol=10uA,#1,#2				0.2	
	Vol3g	Iol=10uA,#3				0.2	
1/3 Bias display Mode							
Output ”H” Voltage	Voh12i	Ioh=-1uA,#1,#2	SEG-n	3.4			V
	Voh3i	Ioh=-1uA,#3		5.8			
Output ”M1” Voltage	Vom12i	Iol/h=+/-10uA,#1,#2		1.0		1.4	
	Vom13i	Iol/h=+/-10uA,#3		1.8		2.2	
Output ”M2” Voltage	Vom22i	Iol/h=+/-10uA,#1,#2		2.2		2.6	
	Vom23i	Iol/h=+/-10uA,#3		3.8		4.2	
Output ”L” Voltage	Vol12i	Iol=1uA,#1,#2				0.2	
	Vol3i	Iol=1uA,#3				0.2	
Output ”H” Voltage	Voh12j	Ioh=-10uA,#1,#2	COM-n	3.4			
	Voh3j	Ioh=-10uA,#3		5.8			
Output ”M1” Voltage	Vom12j	Iol/h=+/-10uA,#1,#2		1.0		1.4	
	Vom13j	Iol/h=+/-10uA,#3		1.8		2.2	
Output ”M2” Voltage	Vom22j	Iol/h=+/-10uA,#1,#2		2.2		2.6	
	Vom23j	Iol/h=+/-10uA,#3		3.8		4.2	
Output ”L” Voltage	Vol12j	Iol=10uA,#1,#2				0.2	
	Vol3j	Iol=10uA,#3				0.2	

TYPICAL APPLICATION CIRCUIT

This application circuit is simply an example, and is not guaranteed to work.



Li power mode, 1/3 Bias, 1/5 Duty

Instruction Table

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
LCT	Lz,Ry	0000 001Z ZZZZ YYYY	(Lz)	←7SEG ← (Ry)	
LCB	Lz,Ry	0000 010Z ZZZZ YYYY	(Lz)	←7SEG ←(Ry)	Blank Zero
LCP	Lz,Ry	0000 011Z ZZZZ YYYY	(Lz)	← (Ry) , (AC)	
LCD	Lz,@HL	0000 100Z ZZZZ 0000	(Lz)	← (R@HL)	
LCT	Lz,@HL	0000 100Z ZZZZ 0001	(Lz)	←7SEG ← (R@HL)	
LCB	Lz,@HL	0000 100Z ZZZZ 0010	(Lz)	←7SEG ← (R@HL)	Blank Zero
LCP	Lz,@HL	0000 100Z ZZZZ 0011	(Lz)	←(R@HL) , (AC)	
OPA	Rx	0000 1010 0XXX XXXX	(IOA)	← (Rx)	
OPAS	Rx,D	0000 1011 DXXX XXXX	IOA1,2,3,4	← (Rx)0, (Rx)1,D,Pulse	
OPB	Rx	0000 1100 0XXX XXXX	(IOB)	← (Rx)	
OPC	Rx	0000 1101 0XXX XXXX	(IOC)	← (Rx)	
FRQ	D,Rx	0001 00DD 0XXX XXXX	FREQ D=00 D=01 D=10 D=11	← (Rx) , (AC) : 1/4 Duty : 1/3 Duty : 1/2 Duty : 1/1 Duty	
FRQ	D,@HL	0001 01DD 0000 0000	FREQ	← (T@HL)	
FRQX	D,X	0001 10DD XXXX XXXX	FREQ	← X	
MVL	Rx	0001 1100 0XXX XXXX	(@L)	← (Rx)	
MVH	Rx	0001 1101 0XXX XXXX	(@H)	← (Rx) , (AC)	
ADC	Rx	0010 0000 0XXX XXXX	(AC)	← (Rx) + (AC) + CF	CF
ADC	@HL	0010 0000 1000 0000	(AC)	← (R@HL) + (AC) + CF	CF
ADC*	Rx	0010 0001 0XXX XXXX	(AC), (Rx)	← (Rx) + (AC) + CF	CF
ADC*	@HL	0010 0001 1000 0000	(AC), (R@HL)	← (R@HL) + (AC) + CF	CF
SBC	Rx	0010 0010 0XXX XXXX	(AC)	← (Rx) + (AC)B + CF	CF
SBC	@HL	0010 0010 1000 0000	(AC)	← (R@HL) + (AC)B + CF	CF
SBC*	Rx	0010 0011 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC)B + CF	CF
SBC*	@HL	0010 0011 1000 0000	(AC),(R@HL)	← (R@HL) + (AC)B + CF	CF
ADD	Rx	0010 0100 0XXX XXXX	(AC)	← (Rx) + (AC)	CF
ADD	@HL	0010 0100 1000 0000	(AC)	← (R@HL) + (AC)	CF
ADD*	Rx	0010 0101 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC)	CF
ADD*	@HL	0010 0101 1000 0000	(AC),(R@HL)	← (R@HL) + (AC)	CF
SUB	Rx	0010 0110 0XXX XXXX	(AC)	← (Rx) + (AC)B + 1	CF
SUB	@HL	0010 0110 1000 0000	(AC)	← (R@HL) + (AC)B + 1	CF
SUB*	Rx	0010 0111 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC)B + 1	CF
SUB*	@HL	0010 0111 1000 0000	(AC),(R@HL)	← (R@HL) + (AC)B + 1	CF
ADN	Rx	0010 1000 0XXX XXXX	(AC)	← (Rx) + (AC)	
ADN	@HL	0010 1000 1000 0000	(AC)	← (R@HL) + (AC)	
ADN*	Rx	0010 1001 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC)	
ADN*	@HL	0010 1001 1000 0000	(AC),(R@HL)	← (R@HL) + (AC)	
AND	Rx	0010 1010 0XXX XXXX	(AC)	← (Rx) AND (AC)	
AND	@HL	0010 1010 1000 0000	(AC)	← (R@HL) AND (AC)	
AND*	Rx	0010 1011 0XXX XXXX	(AC),(Rx)	← (Rx) AND (AC)	
AND*	@HL	0010 1011 1000 0000	(AC),(R@HL)	← (R@HL) AND (AC)	

Instruction		Machine Code	Function		Flag/Remark
EOR	Rx	0010 1100 0XXX XXXX	(AC)	← (Rx) EOR (AC)	
EOR	@HL	0010 1100 1000 0000	(AC)	← (R@HL) EOR (AC)	
EOR*	Rx	0010 1101 0XXX XXXX	(AC),(Rx)	← (Rx) EOR (AC)	
EOR*	@HL	0010 1101 1000 0000	(AC),(R@HL)	← (R@HL) EOR (AC)	
OR	Rx	0010 1110 0XXX XXXX	(AC)	← (Rx) OR (AC)	
OR	@HL	0010 1110 1000 0000	(AC)	← (R@HL) OR (AC)	
OR*	Rx	0010 1111 0XXX XXXX	(AC),(Rx)	← (Rx) OR (AC)	
OR*	@HL	0010 1111 1000 0000	(AC),(R@HL)	← (R@HL) OR (AC)	
ADCI	Ry,D	0011 0000 DDDD YYYY	(AC)	← (Ry) + D + CF	CF
ADCI*	Ry,D	0011 0001 DDDD YYYY	(AC),(Ry)	← (Ry) + D + CF	CF
SBCI	Ry,D	0011 0010 DDDD YYYY	(AC)	← (Ry) + DB + CF	CF
SBCI*	Ry,D	0011 0011 DDDD YYYY	(AC),(Ry)	← (Ry) + DB + CF	CF
ADDI	Ry,D	0011 0100 DDDD YYYY	(AC)	← (Ry) + D	CF
ADDI*	Ry,D	0011 0101 DDDD YYYY	(AC),(Ry)	← (Ry) + D	CF
SUBI	Ry,D	0011 0110 DDDD YYYY	(AC)	← (Ry) + DB + 1	CF
SUBI*	Ry,D	0011 0111 DDDD YYYY	(AC),(Ry)	← (Ry) + DB + 1	CF
ADNI	Ry,D	0011 1000 DDDD YYYY	(AC)	← (Ry) + D	
ADNI*	Ry,D	0011 1001 DDDD YYYY	(AC),(Ry)	← (Ry) + D	
ANDI	Ry,D	0011 1010 DDDD YYYY	(AC)	← (Ry) AND D	
ANDI*	Ry,D	0011 1011 DDDD YYYY	(AC),(Ry)	← (Ry) AND D	
EORI	Ry,D	0011 1100 DDDD YYYY	(AC)	← (Ry) EOR D	
EORI*	Ry,D	0011 1101 DDDD YYYY	(AC),(Ry)	← (Ry) EOR D	
ORI	Ry,D	0011 1110 DDDD YYYY	(AC)	← (Ry) OR D	
ORI*	Ry,D	0011 1111 DDDD YYYY	(AC),(Ry)	← (Ry) OR D	
INC*	Rx	0100 0000 0XXX XXXX	(AC),(Rx)	← (Rx) + 1	CF
INC*	@HL	0100 0000 1000 0000	(AC),(R@HL)	← (R@HL) + 1	CF
DEC*	Rx	0100 0001 0XXX XXXX	(AC),(Rx)	← (Rx) - 1	CF
DEC*	@HL	0100 0001 1000 0000	(AC),(R@HL)	← (R@HL) - 1	CF
IPA	Rx	0100 0010 0XXX XXXX	(AC),(Rx)	← (IOA)	
IPB	Rx	0100 0100 0XXX XXXX	(AC),(Rx)	← (IOB)	
IPC	Rx	0100 0111 0XXX XXXX	(AC),(Rx)	← (IOC)	
MAF	Rx	0100 1010 0XXX XXXX	(AC),(Rx)	← STS1	B3 : CF B2 : ZERO B1 : (No use) B0 : (No use)
MSB	Rx	0100 1011 0XXX XXXX	(AC),(Rx)	← STS2	B3 : (No use) B2 : SCF2 (HRx) B1 : SCF1 (CPT) B0 : BCF
MSC	Rx	0100 1100 0XXX XXXX	(AC),(Rx)	← STS3	B3 : SCF7 (PDV) B2 : PH15 B1 : SCF5 (TM1) B0 : SCF4 (INT)
MCX	Rx	0100 1101 0XXX XXXX	(AC),(Rx)	← STS3X	B3 : SCF9 (RFC) B2 : (No use) B1 : SCF6 (TM2) B0 : SCF8 (SKI)
MSD	Rx	0100 1110 0XXX XXXX	(AC),(Rx)	← STS4	B3 : (No use) B2 : RFOVF B1 : WDF

Instruction		Machine Code	Function		Flag/Remark
					B0 : CSF
SR0	Rx	0101 0000 0XXX XXXX	(AC)n, (Rx)n (AC)3, (Rx)3	← (Rx) (n+1) ← 0	
SR1	Rx	0101 0001 0XXX XXXX	(AC)n, (Rx)n (AC)3, (Rx)3	← (Rx) (n+1) ← 1	
SL0	Rx	0101 0010 0XXX XXXX	(AC)n, (Rx)n (AC)0, (Rx)0	← (Rx) (n-1) ← 0	
SL1	Rx	0101 0011 0XXX XXXX	(AC)n, (Rx)n (AC)0, (Rx)0	← (Rx) (n-1) ← 1	
DAA		0101 0100 0000 0000	(AC)	← BCD (AC)	CF
DAA*	Rx	0101 0101 0XXX XXXX	(AC),(Rx)	← BCD (AC)	CF
DAA*	@HL	0101 0101 1000 0000	(AC),(R@HL)	← BCD (AC)	CF
DAS		0101 0110 0000 0000	(AC)	← BCD (AC)	CF
DAS*	Rx	0101 0111 0XXX XXXX	(AC),(Rx)	← BCD (AC)	CF
DAS*	@HL	0101 0111 1000 0000	(AC),(R@HL)	← BCD (AC)	CF
LDS	Rx,D	0101 1DDD DXXX XXXX	(AC),(Rx)	← D	
LDH	Rx,@HL	0110 0000 0XXX XXXX	(AC),(Rx)	← H (T@HL)	
LDH*	Rx,@HL	0110 0001 0XXX XXXX	(AC),(Rx) (@HL)	← H (T@HL) ← (@HL) + 1	
LDL	Rx,@HL	0110 0010 0XXX XXXX	(AC),(Rx)	← L (T@HL)	
LDL*	Rx,@HL	0110 0011 0XXX XXXX	(AC),(Rx) (@HL)	← L (T@HL) ← (@HL) + 1	
MRF1	Rx	0110 0100 0XXX XXXX	(AC),(Rx)	← (RFC)3-0	
MRF2	Rx	0110 0101 0XXX XXXX	(AC),(Rx)	← (RFC7)-4	
MRF3	Rx	0110 0110 0XXX XXXX	(AC),(Rx)	← (RFC)11-8	
MRF4	Rx	0110 0111 0XXX XXXX	(AC),(Rx)	← (RFC)15-12	
STA	Rx	0110 1000 0XXX XXXX	(Rx)	← (AC)	
STA	@HL	0110 1000 1000 0000	(R@HL)	← (AC)	
LDA	Rx	0110 1100 0XXX XXXX	(AC)	← (Rx)	
LDA	@HL	0110 1100 1000 0000	(AC)	← (R@HL)	
MRA	Rx	0110 1101 0XXX XXXX	CF	← (Rx)3	
MRW	@HL,Rx	0110 1110 0XXX XXXX	(AC),(R@HL)	← (Rx)	
MWR	Rx,@HL	0110 1111 0XXX XXXX	(AC),(Rx)	← (R@HL)	
MRW	Ry,Rx	0111 0YYY YXXX XXXX	(AC),(Ry)	← (Rx)	
MWR	Rx,Ry	0111 1YYY YXXX XXXX	(AC),(Rx)	← (Ry)	
JB0	X	1000 0XXX XXXX XXXX	PC	← X	if (AC)0 = 1
JB1	X	1000 1XXX XXXX XXXX	PC	← X	if (AC)1 = 1
JB2	X	1001 0XXX XXXX XXXX	PC	← X	if (AC)2 = 1
JB3	X	1001 1XXX XXXX XXXX	PC	← X	if (AC)3 = 1
JNZ	X	1010 0XXX XXXX XXXX	PC	← X	if (AC) ≠ 0
JNC	X	1010 1XXX XXXX XXXX	PC	← X	if CF = 0
JZ	X	1011 0XXX XXXX XXXX	PC	← X	if (AC) = 0
JC	X	1011 1XXX XXXX XXXX	PC	← X	if CF = 1
CALL	X	1100 0XXX XXXX XXXX	STACK (PC)	← (PC) + 1 ← X	
JMP	X	1101 0XXX XXXX XXXX	(PC)	← X	
RTS		1101 1000 0000 0000	(PC)	← STACK	CALL Return
SCC	X	1101 1001 0X00 0XXX	X6 = 1 X6 = 0 X2,1,0=001	: Cfq = BCLK : Cfq = PH0 : Cch = PH10	

Instruction		Machine Code	Function		Flag/Remark
			X2,1,0=010 X2,1,0=100	: Cch = PH8 : Cch = PH6	
SCA	X	1101 1010 000X 0000	X4	: Enable SEF4	C1-4
SPA	X	1101 1100 000X XXXX	X4 X3~0	: Set IOA4-1 Pull-Low : Set IOA4-1 I/O	
SPB	X	1101 1101 000X XXXX	X4 X3~0	: Set IOB4-1 Pull-Low : Set IOB4-1 I/O	
SPC	X	1101 1110 000X XXXX	X4 X3-0	: Set IOC4-1 Pull-Low / Low-Level-Hold : Set IOC4-1 I/O	
TMS	Rx	1110 0000 0XXX XXXX	Timer1	← (Rx) & (AC)	
TMS	@HL	1110 0001 0000 0000	Timer1	← (T@HL)	
TMSX	X	1110 0010 XXXX XXXX	X7,6 = 11 X7,6 = 10 X7,6 = 01 X7,6 = 00 X5~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
SPK	X	1110 0011 0XXX XXXX	X6=1 X6=0 X5 =1 X4 =1 X3~0	: KEY_S release by scanning cycle : KEY_S release by normal key scanning : Set all Hi-z : Set all = 1 : Set n of 16	 IOC=normal IOC=KEY SCAN IOC=KEY SCAN
TM2	Rx	1110 0100 0XXX XXXX	Timer2	← (Rx) & (AC)	
TM2	@HL	1110 0101 0000 0000	Timer2	← (T@HL)	
TM2X	X	1110 011X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer2 Value	
SHE	X	1110 1000 0XXX XXX0	X6 X5 X4 X3 X2 X1	: Enable HEF6 : Enable HEF5 : Enable HEF4 : Enable HEF3 : Enable HEF2 : Enable HEF1	RFC KEY_S TMR2 PDV INT TMR1
SIE*	X	1110 1001 0XXX XXXX	X6 X5 X4 X3 X2 X1 X0	: Enable IEF6 : Enable IEF5 : Enable IEF4 : Enable IEF3 : Enable IEF2 : Enable IEF1 : Enable IEF0	RFC KEY_S TMR2 PDV INT TMR1 CPT
PLC	X	1110 101X 0XXX XXXX	X8 X6-0	: Reset PH15~11 : Reset HRF6-0	
SRF	X	1110 1100 00XX XXXX	X5 X4 X3 X2 X1 X0	: Enable Cx Control : Enable TM2 Control : Enable Counter : Enable RH Output : Enable RT Output : Enable RR Output	 ENX EHM ETP ERR

Instruction		Machine Code	Function		Flag/Remark
SRE	X	1110 1101 X0XX 0000	X7 X5 X4	: Enable SRF7 : Enable SRF5 : Enable SRF4	SRF7 (KEY_S) SRF5 (INT) SRF4 (C Port)
FAST		1110 1110 0000 0000	SCLK	: High Speed Clock	
SLOW		1110 1111 0000 0000	SCLK	: Low Speed Clock	
SF	X	1111 0000 X00X XXXX	X7 X4 X3 X2 X1 X0	: Reload 1 Set : WDT Enable : HALT after EL : EL LIGHT On : BCF Set : CF Set	RL1 WDF BCF CF
RF	X	1111 0100 X00X 0XXX	X7 X4 X2 X1 X0	:Reload 1 Reset : WDT Reset : EL LIGHT Off : BCF Reset : CF Reset	RL1 WDF BCF CF
SF2	X	1111 1000 0000 XXXX	X3 X2 X1 X0	: Enable INT powerful Pull-low : Close all Segments : Dis-ENX Set : Reload 2 Set	INTPL RSOFF DED RL2
RF2	X	1111 1001 0000 XXXX	X3 X2 X1 X0	: Disable INT powerful Pull-low : Release Segments : Dis-ENX Reset : Reload 2 Reset	INTPL RSOFF DED RL2
ALM	X	1111 101X XXXX XXXX	X8,7,6=111 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: FREQ : DC1 : PH3 : PH4 : PH5 : DC0 ← PH15~10	
ELC	X	1111 110X XXXX XXXX	X8=1 X8=0 X7,6=11 X7,6=10 X7,6=01 X7,6=00 X5,4=11 X5,4=10 X5,4=01 X5,4=00 X3,2=11 X3,2=10 X3,2=01 X3,2=00 X1,0=11 X1,0=10 X1,0=01 X1,0=00	BCLKX PH0 BCLK/8 BCLK/4 BCLK/2 BCLK 1/1 1/2 2/3 3/4 PH5 PH6 PH7 PH8 1/1 1/2 1/3 1/4	ELP - CLK BCLKX ELP - DUTY ELC - CLK ELC - DUTY
HALT		1111 1110 0000 0000	Halt Operation		
STOP		1111 1111 0000 0000	Stop Operation		

Symbol Description

Symbol	Description	Symbol	Description
( )	Content of Register	D	Immediate Data
AC	Accumulator	(D)B	Complement of Immediate Data
(AC)n	Content of Accumulator (bit n)	PC	Program Counter
(AC)B	Complement of content of Accumulator	CF	Carry Flag
X	Address of program or control data	ZERO	Zero Flag
Rx	Address X of data RAM	WDF	Watch-Dog Timer Enable Flag
(Rx)n	Bit n content of Rx	7SEG	7 segment decoder for LCD
Ry	Address Y of working register	BCLK	System clock for instruction
R@HL	Address of data RAM specified by @HL	IEFn	Interrupt Enable Flag
BCF	Back-up Flag	HRFn	HALT Release Flag
@HL	Generic Index address register	HEFn	HALT Release Enable Flag
(@HL)	Content of generic Index address register	Lz	Address of LCD PLA Latch
(@L)	Content of lowest nibble Index register	SRFn	STOP Release Enable Flag
(@H)	Content of middle nibble Index register	SCFn	Start Condition Flag
(@U)	Content of highest nibble Index register	Cch	Clock Source of Chattering prevention ckt.
T@HL	Address of Table ROM	Cfq	Clock Source of Frequency Generator
H(T@HL)	High Nibble content of Table ROM	SEFn	Switch Enable Flag
L(T@HL)	Low Nibble content of Table ROM	FREQ	Frequency Generator setting Value
TMR	Timer Overflow Release Flag	CSF	Clock Source Flag
Ctm	Clock Source of Timer	P	Program Page
PDV	Pre-Divider	RFOVF	RFC Overflow Flag
STACK	Content of stack	RFC	Resistor to Frequency counter
TM1	Timer 1	(RFC)n	Bit data of Resistor to Frequency counter
TM2	Timer 2		