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TM8763

DATA SHEET

Rev 1.2

AMENDMENT HISTORY

Version	Date	Description
1.0	Feb, 2013	New release
1.1	Jan, 2014	1. Modify Ag and Li Battery Mode Input Voltage 2. Modify DC Output Characteristics 3. Modify Segment Driver Output Characteristics Static Display Mode
1.2	Dec, 2016	Modify P.14 Form

CONTENTS

GENERAL DESCRIPTION

The TM8763 is an embedded high-performance 4-bit microcontroller with LCD/LED driver. It contains all the necessary functions, such as 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock, EL light, LCD driver, look-up table, watchdog timer and keyboard scanning in a signal chip.

FEATURES

1. Low power dissipation.

2. Powerful instruction set (135 instructions).

- Binary addition, subtraction, BCD adjustment, logical operation in direct and index addressing mode.
- Single bit manipulation (set, reset, decision for branch).
- Various conditional branches.
- 16 working registers and manipulation.
- Table look-up.
- LCD driver data transfer.

3. LCD/LED driver output.

- 27 LCD/LED driver outputs (up to drive 135 LCD/LED segments).
- 1/1 Duty, 1/2 Duty, 1/3 Duty, 1/4 Duty or 1/5 Duty for both LCD/LED selected by MASK option.
- 1/2 Bias or 1/3 Bias for LCD selected by MASK option.
- Single instruction to turn off all segments.
- Mask option is used to select SEG1~12, 21~35 as DC outputs/P_open drain.

4. Memory capacity.

- ROM capacity 1536 x 16 bits.
- RAM capacity 96 x 4 bits.

5. Input/output ports.

- Port IOA 4 pins.(with internal pull-low, muxed with SEG24~27)
- Port IOB 4 pins.(with internal pull-low, muxed with SEG28~31)
- Port IOC 4 pins (with internal pull-low / low-level-hold muxed with SEG32~35)

IOC port has built-in input signal chattering prevention circuitry.

6. 8-level subroutine nesting.

7. Interrupt function.

- External factors 3 (INT pin, Port IOC & KI input).
- Internal factors 2 (Pre-Divider, Timer1).

8. Built-in EL-light driver.

- ELC, ELP (Muxed with SEG28, SEG29).

9. Built-in Alarm, Frequency or Melody generator.

- BZB, BZ (Muxed with SEG30, SEG31).

10. Built-in KEY_BOARD scanning function.

- K1~K12 (Shared with SEG1~SEG12).
- KI1~KI4 (Muxed with SEG32~SEG35).

11. One 6-bit programmable timer with programmable clock source.

12. Watch dog timer.

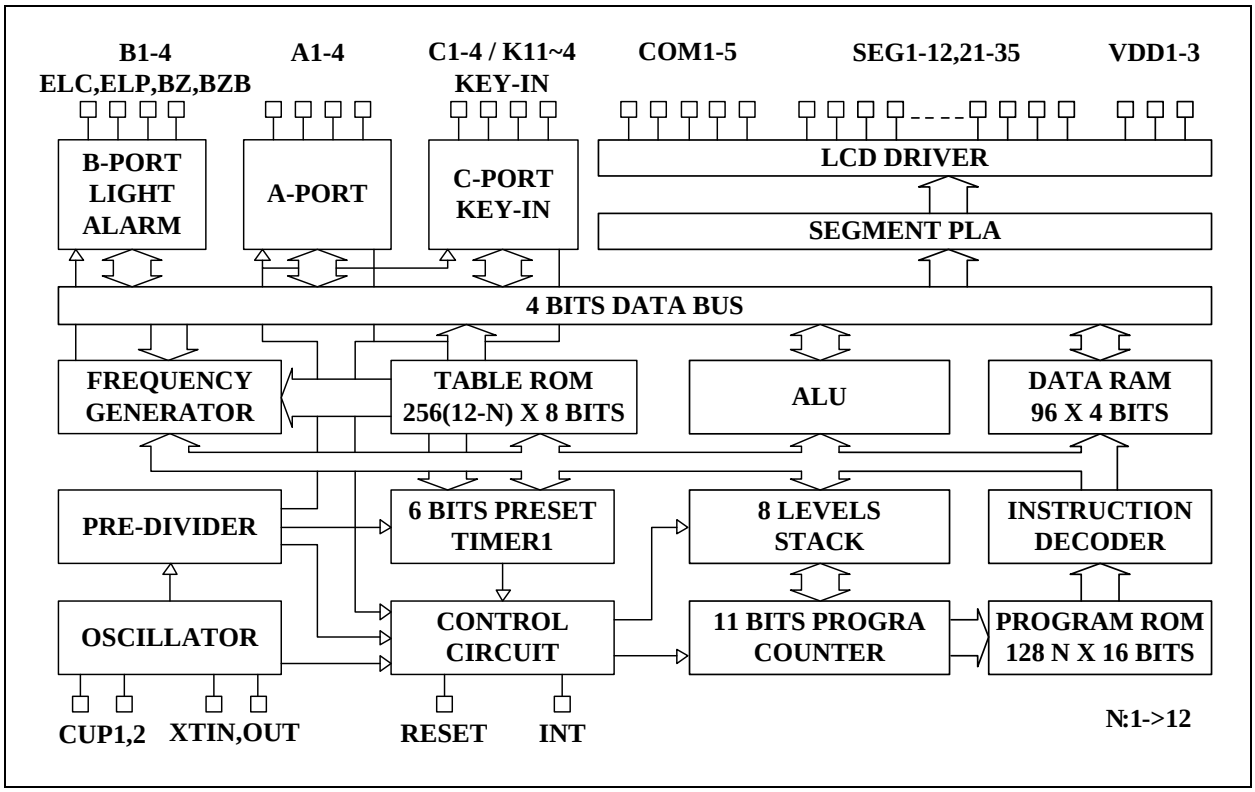
13. Built-in Voltage doubler, halver, tripler charge pump circuit.

14. Dual clock operation.

15. HALT function.

16. STOP function.

BLOCK DIAGRAM



PIN ASSIGNMENT

No	Name	No	Name
1	BAK	23	SEG9/K9
2	XIN	24	SEG10/K10
3	XOUT	25	SEG11/K11
4	GND	26	SEG12/K12
5	VDD1	27	SEG21
6	VDD2	28	SEG22
7	VDD3	29	SEG23
8	CUP1	30	SEG24/IOA1
9	CUP2	31	SEG25/IOA2
10	COM1	32	SEG26/IOA3
11	COM2	33	SEG27/IOA4
12	COM3	34	SEG28/IOB1/ELC
13	COM4	35	SEG29/IOB2/ELP
14	COM5	36	SEG30/IOB3/BZB
15	SEG1/K1	37	SEG31/IOB4/BZ
16	SEG2/K2	38	SEG32/IOC1/KI1
17	SEG3/K3	39	SEG33/IOC2/KI2
18	SEG4/K4	40	SEG34/IOC3/KI3
19	SEG5/K5	41	SEG35/IOC4/KI4
20	SEG6/K6	42	RESET
21	SEG7/K7	43	INT
22	SEG8/K8	44	TEST

PIN DESCRIPTION

Name	I/O	Description
BAK	P	Power Back-up voltage (+). • At Li Mode, connect a 0.1u capacitance to GND.
VDD1,2,3	P	LCD supply voltage and positive supply voltage. • In Ag power mode, connect positive power to VDD1. • In Li or ExtV power mode, connect positive power to VDD2.
RESET	I	Input pin for external reset request signal, with built-in pull-down resistor. • Reset cycle time can be defined as “PH15/2” or “PH12/2” by mask option. • Reset Type can be defined as “Level reset” or “Pulse reset” by mask option.
INT	I	Input pin for external interrupt request signal. • Falling edge or rising edge triggered is defined by mask option. • Internal pull-down or pull-up resistor is defined by mask option.
TESTA	I	Test signal input pin.
CUP1,2	O	Switching pins for supply the LCD driving voltage to the VDD1, 2, 3 pins. • Connect the CUP1 and CUP2 pins with non-polarized electrolytic capacitor when chip is operated in 1/2 or 1/3 bias mode. • In no BIAS mode application, leave these pins opened.
XIN XOUT	I O	Time based counter frequency (clock specified. LCD alternating frequency. Alarm signal frequency) or system clock oscillation. • 32 KHz Crystal oscillator. • In FAST ONLY mode option, connect an external resistor can compose an RC oscillator.
COM1~5	O	Output pins for driving the common pins of the LCD or LED panel.
SEG1-12,21-35	O	Output pins for driving the LCD or LED panel segment.
IOA1-4	I/O	Input/Output port A, and can be defined as SEG24~SEG27 by option.
IOB1-4	I/O	Input/Output port B, and can be defined as SEG28~SEG31 by option.
IOC1-4	I/O	Input/Output port C, and can be defined as SEG32~SEG35 by option.
ELC/ELP	O	Output port for EL panel driver, and can be defined as SEG28, 29 by option.
BZB/BZ	O	Output port for alarm, clock or single tone melody generator, and can be defined as SEG30, 31 by option.
KI1~4	I	Input port for key matrix scanning, and can be defined as SEG32~SEG35 by option.
GND	P	Negative supply voltage.

ABSOLUTE MAXIMUM RATINGS

(GND=0V)

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD1	-0.3 to 5.5	V
	VDD2	-0.3 to 5.5	
	VDD3	-0.3 to 8.5	
Maximum Input Voltage	Vin	-0.3 to VDD1/2 +0.3	
Maximum Output Voltage	Vout1	-0.3 to VDD1/2 +0.3	
	Vout2	-0.3 to VDD3 +0.3	
Maximum Operating Temperature	Topg	-20 to +70	℃
Maximum Storage Temperature	Tstg	-25 to +125	

POWER CONSUMPTION

At Ta= -20°C to 70°C, GND=0V

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
HALT mode	IHALT1	Only 32768 Crystal oscillator operating, without loading. Ag mode, VDD1=1.5V, BCF=0		2	5	uA
	IHALT2	Only 32768 Crystal oscillator operating, without loading. Li mode, VDD2=3.0V, BCF=0		2	5	
STOP mode	ISTOP				1	

Note: When RC oscillator function is operating, the current consumption will depend on the frequency of oscillation.

ALLOWABLE OPERATING CONDITIONS

At Ta= -20°C to 70°C, GND=0V

Name	Symb.	Condition	Min.	Max.	Unit
Supply Voltage	VDD1		1.2	5.25	V
	VDD2		2.4	5.25	
	VDD3		2.4	8.0	
Oscillator Start-Up Voltage	VDDB	Crystal Mode	1.3		
Oscillator Sustain Voltage	VDDB		1.2		
Supply Voltage	VDD1	Ag Mode	1.2	1.65	
	VDD2	EXT-V, Li Mode	2.4	5.25	
Input “H” Voltage	Vih1	Ag Battery Mode	0.8xVDD1	VDD1	
Input “L” Voltage	Vil1		0	0.2xVDD1	
Input “H” Voltage	Vih2	Li Battery Mode	0.8xVDD2	VDD2	
Input “L” Voltage	Vil2		0	0.2xVDD2	
Input “H” Voltage	Vih3	OSCIN at Ag Battery Mode	0.8xVDD1	VDD1	
Input “L” Voltage	Vil3		0	0.2xVDD1	
Input “H” Voltage	Vih4	OSCIN at Li Battery Mode	0.8xVDD2	VDD2	
Input “L” Voltage	Vil4		0	0.2xVDD2	
Input “H” Voltage	Vih5	CFIN at Li Battery or EXT-V Mode	0.8xVDD2	VDD2	
Input “L” Voltage	Vil5		0	0.2xVDD2	
Input “H” Voltage	Vih6	RC Mode	0.8xVDDO	VDDO	
Input “L” Voltage	Vil6		0	0.2xVDDO	
Operating Frequency	Fopg1	Crystal Mode	32		KHz
	Fopg2	RC Mode	10	1000	

ALLOWABLE OPERATING FREQUENCY

At Ta= -20°C to 70°C, GND=0V

Condition	Max. Operating Frequency
BAK=1.5V (VDD1)	800 KHz
BAK=3V (VDD2)	4 MHz

INTERNAL RC FREQUENCY RANGE

Option Mode	BAK	Min.	Typ.	Max.
250 KHz	1.5V	200 KHz	300 KHz	400 KHz
	3.0V	200 KHz	250 KHz	300 KHz
500 KHz	1.5V	450 KHz	600 KHz	750 KHz
	3.0V	400 KHz	500 KHz	600 KHz

ELECTRICAL CHARACTERISTICS

Input Resistance

At#1: VDD1=1.5V (Ag);

At#2: VDD2=3.0V (Li):

At#3: VDD2=5.0V (Ext-V);

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
"L" Level Hold Tr(IOC)	Rllh1	Vi=0.2VDD1, #1	10	40	100	KΩ
	Rllh2	Vi=0.2VDD2, #2	10	40	100	
	Rllh3	Vi=0.2VDD2, #3	5	20	50	
IOA,B,C Pull-Down Tr	Rmad1	Vi=VDD1, #1	200	500	1000	
	Rmad2	Vi=VDD2, #2	200	500	1000	
	Rmad3	Vi=VDD2, #3	100	250	500	
INT Pull-up Tr	Rintu1	Vi=VDD1, #1	100	250	500	
	Rintu2	Vi=VDD2, #2	200	500	1000	
	Rintu3	Vi=VDD2, #3	100	250	500	
INT Pull-Down Tr	Rintd1	Vi=GND, #1	200	500	1000	
	Rintd2	Vi=GND, #2	200	500	1000	
	Rintd3	Vi=GND, #3	100	250	500	
RES Pull-Down R	Rres1	Vi=GND or VDD1, #1	10	40	100	
	Rres2	Vi=GND or VDD2, #2	10	40	100	
	Rres3	Vi=GND or VDD2, #3	10	40	100	

DC Output Characteristics

At#4: VDD1=1.2V (Ag);

At#5: VDD2=2.4V (Li):

At#6: VDD2=4.0V (Ext-V);

Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output “H” Voltage	Voh1c	Ioh= -100 uA, #4	SEG1~12 SEG21~35	1.0			V
	Voh2c	Ioh= -1 mA, #5		2.0			
	Voh3c	Ioh= -3 mA, #6		3.2			
Output “L” Voltage	Vol1c	Iol=200 uA, #4				0.2	
	Vol2c	Iol=2 mA, #5				0.4	
	Vol3c	Iol=6 mA, #6				0.8	

Segment Driver Output Characteristics

At#4: VDD1=1.2V (Ag);

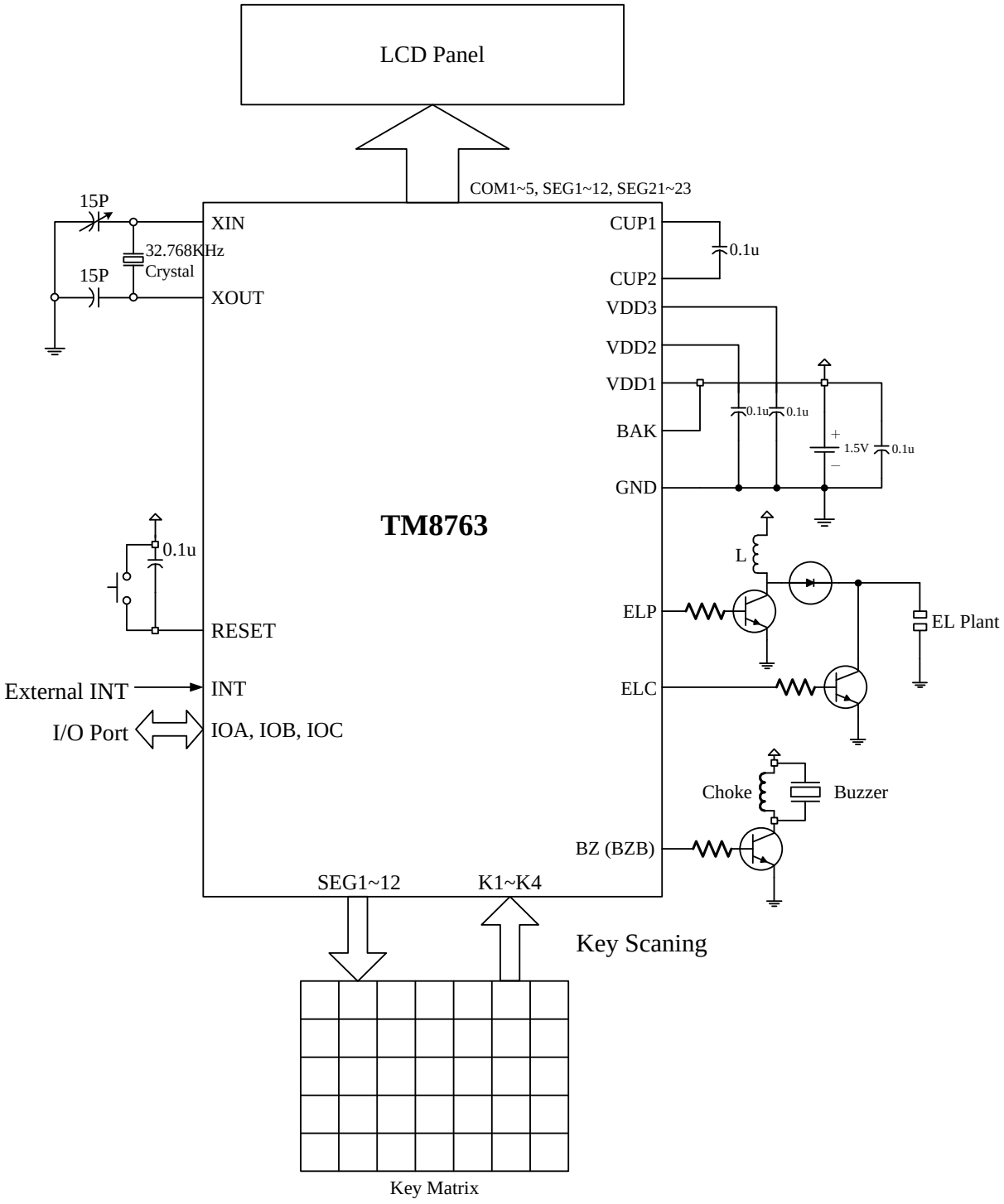
At#5: VDD2=2.4V (Li):

At#6: VDD2=4.0V (Ext-V);

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit.
Static Display Mode							
Output “H” Voltage	Voh1d	Ioh= -1 uA, #4	SEG-n	2.2			V
	Voh2d	Ioh= -1 uA, #5		2.2			
	Voh3d	Ioh= -1 uA, #6		3.8			
Output “L” Voltage	Voh1d	Ioh= 1 uA, #4				0.2	
	Voh2d	Ioh=1 uA, #5				0.2	
	Voh3d	Ioh=1 uA, #6				0.2	
Output “H” Voltage	Voh1e	Ioh= -10 uA, #4	COM-n	2.2			
	Voh2e	Ioh= -10 uA, #5		2.2			
	Voh3e	Ioh= -10 uA, #6		3.8			
Output “L” Voltage	Voh1e	Ioh=10 uA, #4				0.2	
	Voh2e	Ioh=10 uA, #5				0.2	
	Voh3e	Ioh=10 uA, #6				0.2	
1/2 Bias Display Mode							
Output “H” Voltage	Voh12f	Ioh= -1 uA, #4, #5	SEG-n	2.2			V
	Voh3f	Ioh= -1 uA, #6		3.8			
Output “L” Voltage	Vol12f	Iol= 1 uA, #4, #5				0.2	
	Vol3f	Iol= 1 uA, #6				0.2	
Output “H” Voltage	Voh12g	Ioh= -10 uA, #4, #5	COM-n	2.2			
	Voh3g	Ioh= -10 uA, #6		3.8			
Output “M” Voltage	Vom12g	Iol/h=+/-10 uA, #4, #5		1.0		1.4	
	Vom3g	Iol/h=+/-10 uA, #6		1.8		2.2	
Output “L” Voltage	Vol12g	Iol= 10 uA, #4, #5				0.2	
	Vol3g	Iol= 10 uA,#6				0.2	
1/3 Bias Display Mode							
Output “H” Voltage	Voh12i	Ioh= -1 uA, #4, #5	SEG-n	3.4			V
	Voh3i	Ioh= -1 uA, #6		5.8			
Output “M1” Voltage	Vom12i	Iol/h= +/-10 uA, #4, #5		1.0		1.4	
	Vom13i	Iol/h= +/-10 uA, #6		1.8		2.2	
Output “M2” Voltage	Vom22i	Iol/h= +/-10 uA, #4, #5		2.2		2.6	
	Vom23i	Iol/h= +/-10 uA, #6		3.8		4.2	
Output “L” Voltage	Vol12i	Iol=1 uA, #4, #5				0.2	
	Vol3i	Iol=1 uA, #6				0.2	
Output “H” Voltage	Voh12j	Ioh= -10 uA, #4, #5	COM-n	3.4			
	Voh3j	Ioh= -10 uA, #6		5.8			
Output “M1” Voltage	Vom12j	Iol/h= +/-10 uA, #4, #5		1.0		1.4	
	Vom13j	Iol/h= +/-10 uA, #6		1.8		2.2	
Output “M2” Voltage	Vom22j	Iol/h= +/-10 uA, #4, #5		2.2		2.6	
	Vom23j	Iol/h= +/-10 uA, #6		3.8		4.2	
Output “L” Voltage	Vol12j	Iol=10 uA, #4, #5				0.2	
	Vol3j	Iol=10 uA, #6				0.2	

TYPICAL APPLICATION CIRCUIT

This application circuit is simply an example, and is not guaranteed to work.



Ag power mode, 1/3Bias, 1/5Duty

INSTRUCTION TABLE

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
LCT	Lz, Ry	0000 001Z ZZZZ YYYY	Lz	← (7SEG ← Ry)	
LCB	Lz, Ry	0000 010Z ZZZZ YYYY	Lz	← (7SEG ← Ry)	Blank Zero
LCP	Lz, Ry	0000 011Z ZZZZ YYYY	Lz	← Ry & AC	
LCD	Lz, @HL	0000 100Z ZZZZ 0000	Lz	←T@HL	
LCT	Lz, @HL	0000 100Z ZZZZ 0001	Lz	← (7SEG ← @HL)	
LCB	Lz, @HL	0000 100Z ZZZZ 0010	Lz	← (7SEG ← @HL)	Blank Zero
LCP	Lz, @HL	0000 100Z ZZZZ 0011	Lz	← @HL & AC	
OPA	Rx	0000 1010 0XXX XXXX	Port (A)	← Rx	
OPAS	Rx, D	0000 1011 DXXX XXXX	A1, 2, 3, 4	← Rx0,Rx1,D,Pulse	
OPB	Rx	0000 1100 0XXX XXXX	Port (B)	← Rx	
OPC	Rx	0000 1101 0XXX XXXX	Port (C)	← Rx	
FRQ	D, Rx	0001 00DD 0XXX XXXX	FREQ D=00 D=01 D=10 D=11	← Rx & AC : 1/4 Duty : 1/3 Duty : 1/2 Duty : 1/1 Duty	
FRQ	D, @HL	0001 01DD 0000 0000	FREQ	←T@HL	
FRQX	D, X	0001 10DD XXXX XXXX	FREQ	← X	
MVL	Rx	0001 1100 0XXX XXXX	@L	← Rx	
MVH	Rx	0001 1101 0XXX XXXX	@H	← Rx & AC	
ADC	Rx	0010 0000 0XXX XXXX	AC	← Rx + AC + CF	CF
ADC	@HL	0010 0000 1000 0000	AC	← @HL + AC + CF	CF
ADC*	Rx	0010 0001 0XXX XXXX	AC, Rx	← Rx + AC + CF	CF
ADC*	@HL	0010 0001 1000 0000	AC, @HL	← @HL + AC + CF	CF
SBC	Rx	0010 0010 0XXX XXXX	AC	← Rx + ACB + CF	CF
SBC	@HL	0010 0010 1000 0000	AC	← @HL + ACB + CF	CF
SBC*	Rx	0010 0011 0XXX XXXX	AC, Rx	← Rx + ACB + CF	CF
SBC*	@HL	0010 0011 1000 0000	AC, @HL	← @HL + ACB + CF	CF
ADD	Rx	0010 0100 0XXX XXXX	AC	← Rx + AC	CF
ADD	@HL	0010 0100 1000 0000	AC	← @HL + AC	CF
ADD*	Rx	0010 0101 0XXX XXXX	AC, Rx	← Rx + AC	CF
ADD*	@HL	0010 0101 1000 0000	AC, @HL	← @HL + AC	CF
SUB	Rx	0010 0110 0XXX XXXX	AC	← Rx + ACB + 1	CF
SUB	@HL	0010 0110 1000 0000	AC	← @HL + ACB + 1	CF
SUB*	Rx	0010 0111 0XXX XXXX	AC, Rx	← Rx + ACB + 1	CF
SUB*	@HL	0010 0111 1000 0000	AC, @HL	← @HL + ACB + 1	CF
ADN	Rx	0010 1000 0XXX XXXX	AC	← Rx + AC	
ADN	@HL	0010 1000 1000 0000	AC	← @HL + AC	
ADN*	Rx	0010 1001 0XXX XXXX	AC, Rx	← Rx + AC	
ADN*	@HL	0010 1001 1000 0000	AC, @HL	← @HL + AC	
AND	Rx	0010 1010 0XXX XXXX	AC	← Rx AND AC	

Instruction		Machine Code	Function		Flag/Remark
AND	@HL	0010 1010 1000 0000	AC	← @HL AND AC	
AND*	Rx	0010 1011 0XXX XXXX	AC, Rx	← Rx AND AC	
AND*	@HL	0010 1011 1000 0000	AC, @HL	← @HL AND AC	
EOR	Rx	0010 1100 0XXX XXXX	AC	← Rx EOR AC	
EOR	@HL	0010 1100 1000 0000	AC	← @HL EOR AC	
EOR*	Rx	0010 1101 0XXX XXXX	AC, Rx	← Rx EOR AC	
EOR*	@HL	0010 1101 1000 0000	AC, @HL	← @HL EOR AC	
OR	Rx	0010 1110 0XXX XXXX	AC	← Rx OR AC	
OR	@HL	0010 1110 1000 0000	AC	← @HL OR AC	
OR*	Rx	0010 1111 0XXX XXXX	AC, Rx	← Rx OR AC	
OR*	@HL	0010 1111 1000 0000	AC, @HL	← @HL OR AC	
ADCI	Ry, D	0011 0000 DDDD YYYY	AC	← Ry + D + CF	CF
ADCI*	Ry, D	0011 0001 DDDD YYYY	AC, Ry	← Ry + D + CF	CF
SBCI	Ry, D	0011 0010 DDDD YYYY	AC	← Ry + DB + CF	CF
SBCI*	Ry, D	0011 0011 DDDD YYYY	AC, Ry	← Ry + DB + CF	CF
ADDI	Ry, D	0011 0100 DDDD YYYY	AC	← Ry + D	CF
ADDI*	Ry, D	0011 0101 DDDD YYYY	AC, Ry	← Ry + D	CF
SUBI	Ry, D	0011 0110 DDDD YYYY	AC	← Ry + DB + 1	CF
SUBI*	Ry, D	0011 0111 DDDD YYYY	AC, Ry	← Ry + DB + 1	CF
ADNI	Ry, D	0011 1000 DDDD YYYY	AC	← Ry + D	
ADNI*	Ry, D	0011 1001 DDDD YYYY	AC, Ry	← Ry + D	
ANDI	Ry, D	0011 1010 DDDD YYYY	AC	← Ry AND D	
ANDI*	Ry, D	0011 1011 DDDD YYYY	AC, Ry	← Ry AND D	
EORI	Ry, D	0011 1100 DDDD YYYY	AC	← Ry EOR D	
EORI*	Ry, D	0011 1101 DDDD YYYY	AC, Ry	← Ry EOR D	
ORI	Ry, D	0011 1110 DDDD YYYY	AC	← Ry OR D	
ORI*	Ry, D	0011 1111 DDDD YYYY	AC, Ry	← Ry OR D	
INC*	Rx	0100 0000 0XXX XXXX	AC, Rx	← Rx + 1	
INC*	@HL	0100 0000 1000 0000	AC, @HL	← @HL + 1	
DEC*	Rx	0100 0001 0XXX XXXX	AC, Rx	← Rx – 1	
DEC*	@HL	0100 0001 1000 0000	AC, @HL	← @HL – 1	
IPA	Rx	0100 0010 0XXX XXXX	AC, Rx	← Port (A)	
IPB	Rx	0100 0100 0XXX XXXX	AC, Rx	← Port (B)	
IPC	Rx	0100 0111 0XXX XXXX	AC, Rx	← Port (C)	
MAF	Rx	0100 1010 0XXX XXXX	AC, Rx	← STS1	B3: CF B2: ZERO B1: (No use) B0: (No use)
MSB	Rx	0100 1011 0XXX XXXX	AC, Rx	← STS2	B3: (No use) B2: SCF2 (HRx) B1: SCF1 (CPT) B0 BCF

Instruction		Machine Code	Function		Flag/Remark
MSC	Rx	0100 1100 0XXX XXXX	AC, Rx	← STS3	B3: SCF7 (PDV) B2: PH15 B1: SCF5 (TM1) B0: SCF4 (INT)
MCX	Rx	0100 1101 0XXX XXXX	AC, Rx	← STS3X	B3: (No use) B2: (No use) B1: (No use) B0: SCF8 (SKI)
MSD	Rx	0100 1110 0XXX XXXX	AC, Rx	← STS4	B3: (No use) B2: (No use) B1: WDF B0: CSF
SR0	Rx	0101 0000 0XXX XXXX	ACn, Rxn AC3, Rx3	← Rx (n+1) ← 0	
SR1	Rx	0101 0001 0XXX XXXX	ACn, Rxn AC3, Rx3	← Rx (n+1) ← 1	
SL0	Rx	0101 0010 0XXX XXXX	ACn, Rxn AC0, Rx0	← Rx (n-1) ← 0	
SL1	Rx	0101 0011 0XXX XXXX	ACn, Rxn AC0, Rx0	← Rx (n-1) ← 1	
DAA		0101 0100 0000 0000	AC	← BCD (AC)	
DAA*	Rx	0101 0101 0XXX XXXX	AC, Rx	← BCD (AC)	
DAA*	@HL	0101 0101 1000 0000	AC, @HL	← BCD (AC)	
DAS		0101 0110 0000 0000	AC	← BCD (AC)	
DAS*	Rx	0101 0111 0XXX XXXX	AC, Rx	← BCD (AC)	
DAS*	@HL	0101 0111 1000 0000	AC, @HL	← BCD (AC)	
LDS	Rx, D	0101 1DDD DXXX XXXX	AC, Rx	← D	
LDH	Rx, @HL	0110 0000 0XXX XXXX	AC, Rx	← H (T@HL)	
LDH*	Rx, @HL	0110 0001 0XXX XXXX	AC, Rx HL	← H (T@HL) ← HL + 1	
LDL	Rx, @HL	0110 0010 0XXX XXXX	AC, Rx	← L (T@HL)	
LDL*	Rx, @HL	0110 0011 0XXX XXXX	AC, Rx HL	← L (T@HL) ← HL + 1	
STA	Rx	0110 1000 0XXX XXXX	Rx	← AC	
STA	@HL	0110 1000 1000 0000	@HL	← AC	
LDA	Rx	0110 1100 0XXX XXXX	AC	← Rx	
LDA	@HL	0100 1100 1000 0000	AC	← @HL	
MRA	Rx	0110 1101 0XXX XXXX	CF	← Rx3	
MRW	@HL, Rx	0110 1110 0XXX XXXX	AC, @HL	← Rx	
MWR	Rx, @HL	0110 1111 0XXX XXXX	AC, Rx	← @HL	
MRW	Ry, Rx	0111 0YYY YXXX XXXX	AC, Ry	← Rx	
MWR	Rx, Ry	0111 1YYY YXXX XXXX	AC, Rx	← Ry	
JB0	X	1000 0XXX XXXX XXXX	PC	← X	if AC0 = 1
JB1	X	1000 1XXX XXXX XXXX	PC	← X	if AC1 = 1
JB2	X	1000 0XXX XXXX XXXX	PC	← X	if AC2 = 1
JB3	X	1000 1XXX XXXX XXXX	PC	← X	if AC3 = 1
JNZ	X	1010 0XXX XXXX XXXX	PC	← X	if AC ≠ 0

Instruction		Machine Code	Function		Flag/Remark
JNC	X	1010 1XXX XXXX XXXX	PC	← X	if CF=0
JZ	X	1011 0XXX XXXX XXXX	PC	← X	if AC=0
JC	X	1011 1XXX XXXX XXXX	PC	← X	if CF=1
CALL	X	1100 0XXX XXXX XXXX	STACK PC	← PC + 1 ← X	
JMP	X	1101 0XXX XXXX XXXX	PC	← X	
RTS		1101 1000 0000 0000	PC	← STACK	CALL Return
SCC	X	1101 1001 0X00 0XXX	X6=1 X6=0 X2, 1, 0=001 X2, 1, 0=010 X2, 1, 0=100	: Cfq=BCLK : Cfq=PH0 : Cch=PH10 : Cch=PH8 : Cch=PH6	
SCA	X	1101 1010 000X 0000	X4	: Enable SEF4	C1-4
SPA	X	1101 1100 0000 XXXX	X3~0	: Set A4-1 I/O	
SPB	X	1101 1101 0000 XXXX	X3~0	: Set B4-1 I/O	
SPC	X	1101 1110 000X XXXX	X4 X3-0	: Set C4-1 Pull-Low / Low-Level-Hold : Set C4-1 I/O	
TMS	Rx	1110 0000 0XXX XXXX	Timer1	← Rx & AC	
TMS	@HL	1110 0001 0000 0000	Timer1	← T@HL	
TMSX	X	1110 0010 XXXX XXXX	X7, 6=11 X7, 6=10 X7, 6=01 X7, 6=00 X5~0	: Ctm=FREQ : Ctm=PH15 : Ctm=PH3 : Ctm=PH9 : Set Timer1 Value	
SPK	X	1110 0011 0XXX XXXX	X6=1 X6=0 X5=1 X4=1 X3~0	: KEY_S release by scanning cycle : KEY_S release by normal key scanning : Set all Hi-z : Set all=1 : Set n of 12	IOC=normal IOC=KEY SCAN IOC=KEY SCAN
SHE	X	1110 1000 00X0 XXX0	X5 X3 X2 X1	: Enable HEF5 : Enable HEF3 : Enable HEF2 : Enable HEF1	KEY_S PDV INT TMR1
SIE*	X	1110 1001 00X0 XXXX	X5 X3 X2 X1 X0	: Enable IEF5 : Enable IEF3 : Enable IEF2 : Enable IEF1 : Enable IEF0	KEY_S PDV INT TMR1 CPT
PLC	X	1110 101X 00X0 XXXX	X8 X5, 3-0	: Reset PH15~11 : Reset HRF5,3-0	
SRE	X	1110 1101 X0XX 0000	X7 X5 X4	: Enable SRF7 : Enable SRF5 : Enable SRF4	SRF7(KEY_S) SRF5 (INT) SRF4 (C Port)
FAST		1110 1110 0000 0000	SCLK	: High Speed Clock	
SLOW		1110 1111 0000 0000	SCLK	: Low Speed Clock	

Instruction		Machine Code	Function		Flag/Remark
SF	X	1111 0000 X00X XXXX	X7 X4 X3 X2 X1 X0	: Reload 1 Set : WDT Enable : HALT after EL : EL LIGHT On : BCF Set : CF Set	 RL1 WDF BCF CF
RF	X	1111 0100 X00X 0XXX	X7 X4 X2 X1 X0	:Reload 1 Reset : WDT Disable : EL LIGHT Off : BCF Reset : CF Reset	RL1 WDF BCF CF
SF2	X	1111 1000 0000 XX00	X3 X2	: Enable INT powerful Pull-low : Close all Segments	INTPL RSOFF
RF2	X	1111 1001 0000 XX00	X3 X2	: Disable INT powerful Pull-low : Release Segments	INTPL RSOFF
ALM	X	1111 101X XXXX XXXX	X8, 7, 6=111 X8, 7, 6=100 X8, 7, 6=011 X8, 7, 6=010 X8, 7, 6=001 X8, 7, 6=000 X5~0	: FREQ : DC1 : PH3 : PH4 : PH5 : DC0 ← PH15~10	
ELC	X	1111 110X XXXX XXXX	X8=1 X8=0 X7, 6=11 X7, 6=10 X7, 6=01 X7, 6=00 X5, 4=11 X5, 4=10 X5, 4=01 X5, 4=00 X3, 2=11 X3, 2=10 X3, 2=01 X3, 2=00 X1, 0=11 X1, 0=10 X1, 0=01 X1, 0=00	BCLKX PH0 BCLK/8 BCLK/4 BCLK/2 BCLK 1/1 1/2 1/3 1/4 PH5 PH6 PH7 PH8 1/1 1/2 1/3 1/4	ELP - CLK BCLKX ELP - DUTY ELC - CLK ELC - DUTY
HALT		1111 1110 0000 0000	Halt Operation		
STOP		1111 1111 0000 0000	Stop Operation		

Symbol Description

AC	: Accumulator	D	: Immediate Data
ACn	: Accumulator bit n	PC	: Program Counter
X	: Address	CF	: Carry Flag
Rx	: Memory of address X	ZERO	: Zero Flag
Rxn	: Memory bit n of address X	WDF	: Watch-Dog Timer Enable Flag
Ry	: Memory of working register Y	HL	: Index Register
BCF	: Back-up Flag	BCLK	: System clock stop only in STOP condition
@HL	: Address of Index	IEFn	: Interrupt Enable Flag
HRFn	: HALT Release Flag	SRFn	: STOP Release Enable Flag
HEFn	: HALT Release Enable Flag	SCFn	: Start Condition Flag
TMR	: Timer Overflow Release Flag	Cch	: Clock Source of Chartering Detector
Ctm	: Clock Source of Timer	Cfq	: Clock Source of Frequency Generator
PDV	: Pre-Divider	SEFn	: Switch Enable Flag
Lz	: LCD Latch	FREQ	: Frequency Generator setting Value
T@HL	: Address of Index ROM	CSF	: Clock Source Flag
@L	: Low address of Index	@H	: High address of Index
H(T@HL)	: High Nibble of Index ROM	L(T@HL)	: Low Nibble of Index ROM
( )	: Content of Register		