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TM87ML28

DATA SHEET

Rev V1.3

AMENDMENT HISTORY

Version	Date	Description
1.0	Mar, 2018	New release.
1.1	Mar, 2019	Modify P.43 VDX4~0 : Set VDL regulator output voltage to VDX4~0 : Set VREG regulator output voltage
1.2	DEC, 2019	Deleted P15. LVR Current Max. 0.5uA
1.3	Mar, 2021	1. FEATURE(2) amended to delete "4 bits x 4 bits Multiplier" 2. PIN DESCRIPTION (COM1~9) amended and deleted "COM1~4 can be defined as COMS or Open Drain type output by option if COM5 is not defined as SEG52." 3. FEATURE(14) adds "Merge 2 or 3 timer as 12-bits or 18-bits timer by STM instruction." & "Extend 1 timer as 12-bits timer by STE instruction." 4. Modify NSS pin -> SSB pin 5. Change some “option” to “code option” for difference software option 6. Modify <SSTA1> IRQ usage conditions for SIOTYP=11 Mode 7. Correction: "STCL3" -> "SCTL3" 8. change VREG & VDL ±0.1V to ±4.5% 9. Cutting LBD initial 1.95/1.35V Spec. for LBD3~0-8~F/0~7 only

CONTENTS

GENERAL DESCRIPTION

The TM87ML28 is a Multiple Time Programmed ROM embedded high-performance 4-bit microcomputer with LCD driver. It contains all the necessary functions, such as 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock operation, Resistance to Frequency Converter(RFC), EL panel driver, Serial Peripheral Interface (I2C/UART/SPI), LCD driver, look-up table, watchdog timer and key matrix scanning circuitry in a signal chip.

FEATURE

1. Low power dissipation.
   1.5V/3V operating voltage range.

TM87ML28L	1.5V Power Mode
TM87ML28H	3V Power Mode

2. Powerful instruction set.
   Binary addition, subtraction, BCD. BCD can be executed directly in addition, subtraction.
   Single-bit manipulation (set, reset, decision for branch).
   Various conditional branches.
   16 initial working registers and manipulators. (can be extended to all RAM by Page Mode)
   Table look-up.
   LCD driver data transfer.

3. ROM(MTP) capacity. 8K x 16 bits.
   - Instruction ROM Max. capacity 8K x 16 bits.
   - Table ROM Max. capacity 8K x 8 bits.
   - Endurance: 50000 cycles (min.)
   - Built-in Table ROM Word Write by Instruction in 3V Power Mode

4. RAM capacity. 1024 x 4bits.

5. With direct/index addressing mode in data RAM access.

6. LCD driver output.
   - Max 423 LCD dots by 9 common outputs and 47 segment outputs.
   - SEG24~47 can be defined as IOA1~4/CX,RFC0~2 , IOB1~4/ELC,ELP,BZB,BZ , IOC/KI1~4,IOD1~4,IOE1~4,IOF1~4 by code option.
   - 1/1~1/9 Duty can be selected by code option.
   - 1/2 ~1/3 Bias can be selected by code option.
   - Single instruction to turn off all segments.
   - COM1~9,SEG1~47 can be defined as CMOS or P_open drain type output by code option.
   - COM5~9 can be defined as SEG52~48 by code option.
   - Built-in regulator mode for VL1/2 by code option.
7. Input/output ports.

- Port IOA 4 pins (with internal pull-low, input signal chattering prevention circuitry), and can be defined as SEG24~27/ CX,RFC0~2 or CX,RFC0~2/ ELC,ELP,BZB,BZ /SDA,SCL,RXD,TXD by code option.
- Port IOB 4 pins (with internal pull-low), and can be defined as SEG28~31/ ELC,ELP,BZB,BZ by code option.
- Port IOC 4 pins (with internal pull-low, low-level-hold, input signal chattering prevention circuitry), and can be defined as SEG32~35 / KI1~4 by code option.
- Port IOD 4 pins (with internal pull-low, input signal chattering prevention circuitry), and can be defined as SEG36~39 by code option.
- Port IOE 4 pins (with internal pull-low, input signal chattering prevention circuitry), and can be defined as SEG40~43 or RFC3~5,CX2/ELC,ELP,BZB,BZ/SIOX,SIOY,SCK,SSB by code option..
- Port IOF 4 pins (with internal pull-low, input signal chattering prevention circuitry), and can be defined as SEG44~47 by code option.

8. Interrupt function.
   - External factors 6(INT pin, SIO, Port IOA, IOC, IOD & KI input).
   - Internal factors 4(Pre-Divider, Timer1, Timer2, Timer3 & RFC).

9. Built-in EL-light driver.
   - ELC, ELP. Can be defined as SEG28,29/IOB1,2 or CX,RFC0/IOA1,2/SCA,SCL or RFC3,4/IOE1,2/MOSI,MISO by code option.

10. Built-in Alarm, clock or single tone melody generator.
    - BZB, BZ. Can be defined as SEG30,31/IOB3,4 or RFC2,3/IOA3,4/RXD,TXD or RFC5,CX2/IOE3,4/SCK/SSB by code option.

11. Built-in resistance to frequency converter.
    - CX,RFC0~2 Can be defined as SEG24~27/IOA1~4 or IOA1~4/ELC,ELP,BZB,BZ / SDA,SCL,RXD,TXD by code option.
    - RFC3~5,CX2 Can be defined as IOE1~4/ELC,ELP,BZB,BZ/SIOX,SIOY,SCK,SSB by code option.

12. Built-in key matrix scanning function.
    - KO1~KO16(Shared with SEG1~16)
    - KI1~KI4. Can be defined as SEG32~35/IOC1~4 by code option.

13. Built-in Serial Interface (UART/SPI/I2C).
    - SDA,SCL,RXD,TXD Can be defined as CX,RFC0~2/IOA1~4/ELC,ELP,BZB,BZ by code option.
    - SIOX,SIOY,SCK,SSB Can be defined as RFC3~5,CX2/IOE1~4/ELC,ELP,BZB,BZ by code option.

14. Three 6-bit programmable timers with programmable clock source.
    - Read out the content in anytime
    - Merge 2 or 3 timer as 12-bits or 18-bits timer by STM instruction.
    - Extend 1 timer as 12-bits timer by STE instruction.

15. Watch dog timer & Key-Reset (No initial LCD, CMOS, and P_open drain type output data after reset by Watchdog timer or Key-Reset, and need select “OFF” for code option of “LCD Display in Reset Cycle”.)

16. Built-in voltage charge halver & pump circuit.

17. Dual clock operation
    - slow clock oscillation can be defined as X’tal or external RC type oscillator by code option.
    - fast clock oscillation can be defined as 3.58MHz ceramic resonator, internal R or external R type oscillator by code option.
18. HALT function.

19. STOP function.

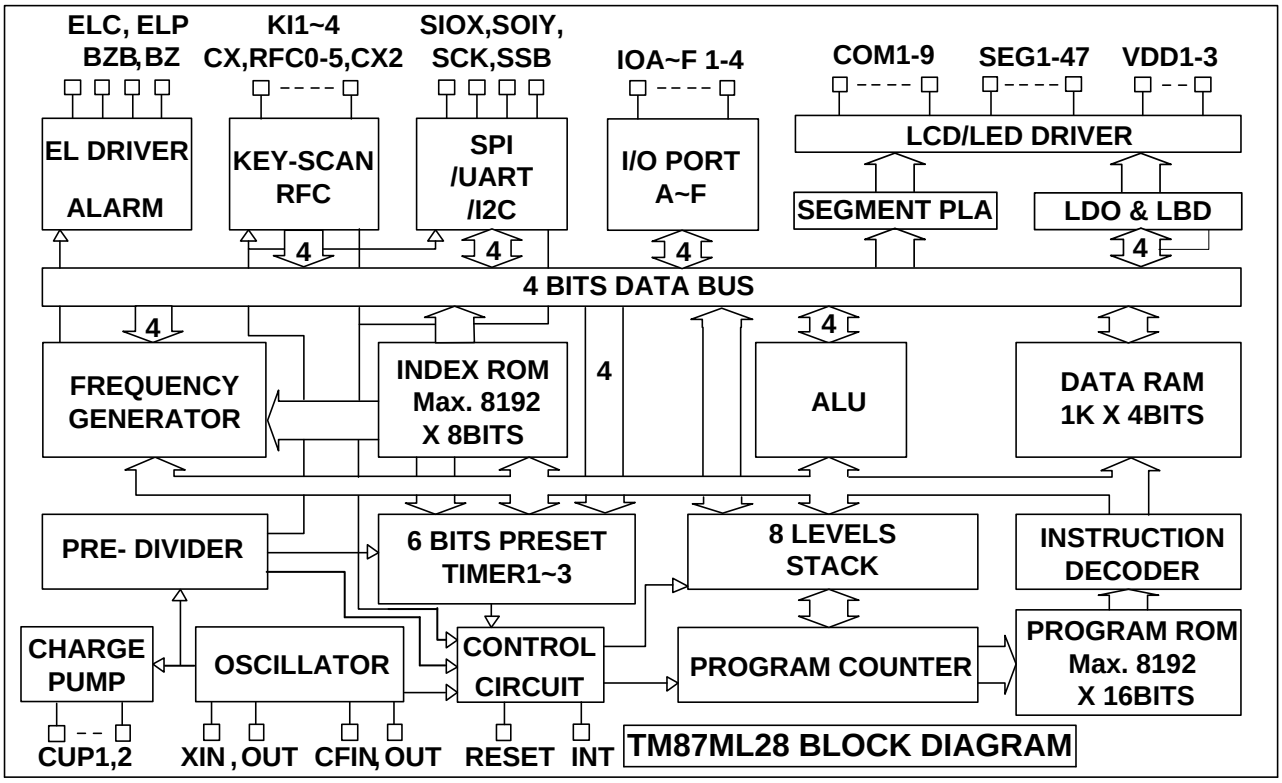
20. Built-in Low Battery Detect.

21. Built-in Low Voltage Reset.

APPLICATION

- Timer / Calendar / Calculator / Thermometer

BLOCK DIAGRAM



PAD ASSIGNMENT

No	Name	No	Name
1	BAK	41	SEG21
2	XIN	42	SEG22
3	XOUT	43	SEG23
4	CFIN	44	SEG24/IOA1/CX
5	CFOUT	45	SEG25/IOA2/RFC0<RR>
6	GND*	46	SEG26/IOA3/RFC1<RT>
7	VL1<VDD1>	47	SEG27/IOA4/RFC2<RH>
8	VL2<VDD2>	48	SEG28/IOB1/ELC
9	VL3<VDD3>	49	SEG29/IOB2/ELP
10	CUP1	50	SEG30/IOB3/BZB
11	CUP2	51	SEG31/IOB4/BZ
12	COM1	52	SEG32/IOC1/KI1
13	COM2	53	SEG33/IOC2/KI2
14	COM3	54	SEG34/IOC3/KI3
15	COM4	55	SEG35/IOC4/KI4
16	COM5/SEG52	56	SEG36/IOD1
17	COM6/SEG51	57	SEG37/IOD2
18	COM7/SEG50	58	SEG38/IOD3
19	COM8/SEG49	59	SEG39/IOD4
20	COM9/SEG48	60	SEG40/IOE1
21	SEG1(K1)	61	SEG41/IOE2
22	SEG2(K2)	62	SEG42/IOE3
23	SEG3(K3)	63	SEG43/IOE4
24	SEG4(K4)	64	SEG44/IOF1
25	SEG5(K5)	65	SEG45/IOF2
26	SEG6(K6)	66	SEG46/IOF3
27	SEG7(K7)	67	SEG47/IOF4
28	SEG8(K8)	68	CX'/IOA1'/ELC/SDA
29	SEG9(K9)	69	RFC0'/IOA2'/ELP/SCL
30	SEG10(K10)	70	RFC1'/IOA3'/BZB/RXD
31	SEG11(K11)	71	RFC2'/IOA4'/BZ/TXD
32	SEG12(K12)	72	RFC3/IOE1'/ELC/SIOX(MISO/TXD/SDA)
33	SEG13(K13)	73	RFC4/IOE2'/ELP/SIOY(MOSI/RXD/SCL)
34	SEG14(K14)	74	RFC5/IOE3'/BZB/SCK
35	SEG15(K15)	75	CX2/IOE4'/BZ/SSB
36	SEG16(K16)	76	RESET(VPP)
37	SEG17	77	INT
38	SEG18	78	VBAT
39	SEG19		
40	SEG20		

Symbol Description

'< >' : Pin name in TM8726/27/67/68

'( )' : Attached function

'/' : Option function

‘*’ : Two GND pad
‘’ : second group.

PIN DESCRIPTION

Name	I/O	Description
BAK	P	Positive Back-up voltage. If BAK=VL1/2 or VREG at BCF=0, connect a 0.1uF capacitor to GND. Positive voltage is need to BAK for Serial Program/Read Mode.
VBAT	P	Positive supply voltage. Positive voltage is need to VBAT for Serial Program/Read Mode.
VL1~3	P	LCD supply voltage. In 1.5V Power Mode & “LCD CHARGE PUMP MODE” code option = “VL1(NO REGULATOR”, connect positive power output to VL1. In 3V Power mode & “LCD CHARGE PUMP MODE”” code option = “VL1(NO REGULATOR)” or “VL2(NO REGULATOR)”, connect positive power to VL2. If “LCD CHARGE PUMP MODE” code option = “VDL(1.05V)” or “VDL(2.10V)”, connect Capacitors to VL1~3 For 1/3Bias by Capacitor Voltage Divider mode, connect positive power to VL3. Positive voltage is need to VL3 for Serial Program/Read Mode.
RESET	I	Input pin for external reset request signal, built-in internal pull-down resistor. High voltage is need to RESET pin for Serial Program/Read Mode.
INT	I	Input pin for external INT request signal. . Falling edge or rising edge triggered is defined by code option. . Internal pull-down or pull-up resistor is defined by code option.
CUP1,2	O	Switching pins for supply the LCD driving voltage to the VL1~3 pins. . Connect the CUP1 to CUP2 pins with non-polarized electrolytic capacitors when chip operated in 1/2 or 1/3 bias mode.
XIN XOUT	I O	Low speed oscillator, generates clock for time base functions(clock specified. LCD alternating frequency. Alarm signal frequency) or system clock oscillation. . The usage of 32KHz Crystal oscillator or external RC oscillator is defined by code option.
CFIN CFOUT	I O	High speed oscillator, system clock oscillation for FAST clock only or DUAL clock operation. The usage of 3.58MHz ceramic/resonator oscillator or external R type oscillator is defined by code option
COM1~9	O	Output pins for driving the common pins of the LCD panel. COM1~9 can be defined as COMS or Open Drain type output by code option. COM5~9 can be defined as SEG52~48 by code option.
SEG1-47	O	Output pins for driving the LCD panel segment. SEG24~27 can be defined as IOA1~4/CX,RFC0~2 by code option. SEG28~31 can be defined as IOB1~4/ELC,ELP,BZB,BZ by code option. SEG32~35 can be defined as IOC1~4/KI1~4 by code option. SEG36~39 can be defined as IOD1~4 by code option. SEG40~43 can be defined as IOE1~4 by code option. SEG44~47 can be defined as IOF1~4 by code option. SEG1~47 can be defined as COMS or Open Drain type output by code option.
IOA1-4	I/O	Input / Output port A, and can be defined as SEG24~27/CX,RFC0~2 or CX,RFC0~2/ /ELC,ELP,BZB,BZ/SDA,SCL,RXD,TXD by code option. Only one group of SEG24~27/CX,RFC0~2 and CX,RFC0~2/ELC,ELP,BZB,BZ/SDA, SCL,RXD,TXD can be defined as IOA1~ 4.
IOB1-4	I/O	Input / Output port B, and can be defined as SEG28~31/ELC,ELP,BZB,BZ by code option.
IOC1-4	I/O	Input / Output port C, and can be defined as SEG32~35/KI1~4 by code option. IOC3,4 is Signal for Serial Program/Read Mode.
IOD1~4	I/O	Input / Output port D, and can be defined as SEG36~39 by code option.
IOE1~4	I/O	Input / Output port E, and can be defined as SEG40~43 or RFC3~5,CX2/ELC,ELP, BZB,BZ/MOSI/MISO/SCK/SSB by code option. Only one group of SEG40~43 and RFC3~5,CX2/ELC/ELP,BZB,BZ/SIOX,SIOY,SCK, SSB can be defined as IOE1~4.

Name	I/O	Description
IOF1~4	I/O	Input / Output port F, and can be defined as SEG44~47 by code option.
CX,CX2 RFC0~5	I O	2 input pin and 6 output pins for RFC application. CX,RFC0~2 can be defined as SEG24~27/IOA1~4 or IOA1~4/ELC,ELP,BZB,BZ/ SDA,SCL,RXD,TXD by code option. RFC3~5,CX2 can be defined as IOE1~4/ELC,ELP,BZB,BZ/ SIOX,SIOY,SCK,SSB by code option. Only one group of SEG24~27/IOA1~4 and IOA1~4 can be defined as CX,RFC0~2.
ELC/ELP	O	Output port for EL panel driver, and can be defined as SEG28,29/IOB1,2 or CX,RFC0/IOA1,2/SCA,SCL or RFC3,4/ IOE1,2/MOSI,MISO by code option.
BZB/BZ	O	Output port for alarm, clock or single tone melody generator, and can be defined as SEG30,31 / IOB3,4 or RFC1,2/IOA3,4/RXD,TXD or RFC5,CX2/IOE3,4/SCK,SSB by code option.
KO1~KO16	O	Output port for key matrix scanning, shared with SEG1~16.
KI1~4	I	Input port for key matrix scanning, and can be defined as SEG32~35/IOC1~4 by code option.
SDA SCL	I/O O	1 input/output data pins, 1 output synchronous clock pin for I2C application, and can be defined as. CX,RFC0/IOA1,2/ELC,ELP by code option.
RXD TXD	I I/O	1 input data pins, 1 input/output data pin for UART application, and can be defined as. RFC1,2/IOA3,4/BZB,BZ by code option.
SIOX,SIOY, SCK,SSB	I/O	2 input/output data pins, 1 input/output synchronous clock pin, and 1 input/output slave select pin for SPI application, and can be defined as RFC3~5,CX2/IOE1~4/ELC,ELP, BZB,BZ by code option. SIOX,SIOY can be set as SDA,SCL/RXD,TXD pins for UART/I2C by instructon if IOA 1,2/3,4 not set to SDA,SCL/RXD,TXD.
GND	P	Negative supply voltage.

SERIAL PROGRAM/READ CONNECT PINS

VBAT, GND, BAK, VL3, RESET, IOC3, IOC4

ABSOLOUTE MAXIMUM RATINGS

GND= 0V

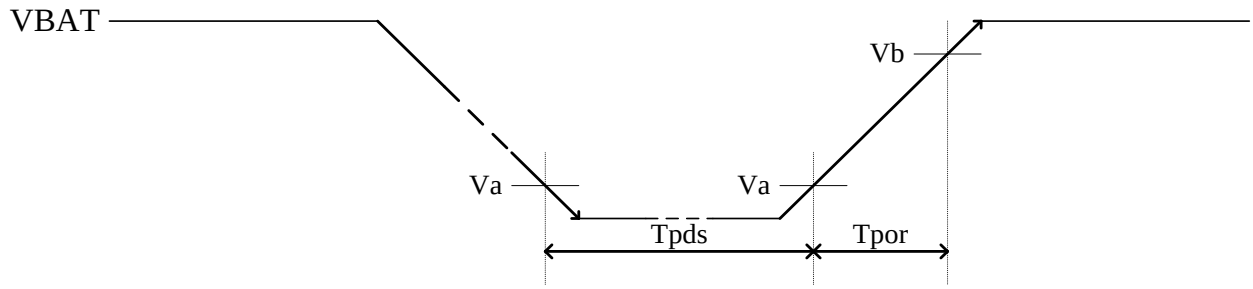
Name	Symbol	Range	Unit
Maximum Supply Voltage	VBAT	-0.3 to 3.6	V
	VL1	-0.3 to 2.1	
	VL2	-0.3 to 3.6	
	VL3	-0.3 to 6.0	
	VL4	-0.3 to 6.0	
	VL5	-0.3 to 6.0	
Maximum Input Voltage	Vin1	-0.3 to VBAT+0.3	
	Vin2	-0.3 to VL1/2+0.3	
Maximum output Voltage	Vout1	-0.3 to VBAT+0.3	
	Vout2	-0.3 to VL1/2+0.3	
	Vout3	-0.3 to VL3+0.3	
	Vout4	-0.3 to VL4+0.3	
	Vout5	-0.3 to VL5+0.3	
Maximum Operating Temperature	Topg	-40 to +80	℃
Maximum Storage Temperature	Tstg	-40 to +125	

ALLOWABLE OPERATING CONDITIONS

at#1: 1.5V Power Mode Ta=-20℃ to 70℃,GND= 0V
at#2: 3V Power Mode(BCF=0 : BAK < VBAT) , Ta=-20℃ to 70℃,GND= 0V
at#3: 3V Power Mode(BCF=0 : BAK=VBAT) , Ta=-40℃ to 80℃,GND= 0V
Crystal Mode condition : XIN&XOUT without match capacitor

Name	Symb.	Condition	Min.	Max.	Unit
Supply LCD Voltage	VL1		0.95	1.8	V
	VL2		1.8	3.6	
	VL3		1.8	5.4	
Oscillator Start-Up Voltage	BAK	Crystal Mode BCF=1 , #1	1.4		
		Crystal Mode BCF=1 , #2	1.5		
		Crystal Mode BCF=1 , #3	1.6		
Oscillator Sustain Voltage	BAK	Crystal Mode BCF=0 , #1	1.1	1.8	
		Crystal Mode BCF=0 , #2	1.1	3.6	
		Crystal Mode BCF=0 , #3	1.3		
Supply Voltage	BAK		1.2 *1	3.6	
Supply Voltage	VBAT	1.5V Power Mode without regulator	1.2 *1	1.8	
		1.5V Power Mode with regulator	1.35 *1		
		3V Power Mode without regulator BAK=VBAT for BCF=0	1.8	3.6	
		3V Power Mode without regulator BAK=VL1 for BCF=0	2.4		
		3V Power Mode with regulator VL2=VDL	2.0		
		3V Power Mode with regulator VL1=VDL	1.8		
Input “H” Voltage	Vih1	I/O,INT,RESETB,CX	0.8xVBAT	VBAT	
Input “L” Voltage	Vil1		0	0.2xVBAT	
Input “H” Voltage	Vih2	OSCIN	0.8xBAK	BAK	
Input “L” Voltage	Vil2		0	0.2xBAK	
Operating Freq	Fopg1	Crystal Mode	32		KHz
	Fopg2	RC Mode	10	4096	
	Fopg3	CF Mode	1000		
Power-down stable time before Power-on reset activation	Tpds	Va= 0.1xVBAT	1		S
Power-on reset activation power rise time	Tpor	Va/Vb= 0.1/0.9 x VBAT VBAT>=1.2V		10	mS

*1 : Crystal mode need take care Oscillator Start-Up Voltage.



ALLOWABLE OPERATING FREQUENCY

At #1 Ta= 0℃ to 80℃,GND= 0V
At #2 Ta=-20℃ to 80℃,GND= 0V
At #3 Ta=-40℃ to 80℃,GND= 0V

Condition	Maximum Operating Frequency
BAK=1.2V #1	500KHz
BAK=1.3V #2	1MHz
BAK=1.4V #3	1.5MHz
BAK=1.8V #3	4MHz
BAK=2.2V #3	6MHz

ELECTRICAL CHARACTERISTICS

Power Consumption

at Ta=-40℃ to 80℃,GND= 0V
Halt Condition : BCF=0 , 1/3Bias , 1/9Duty , LCD Alternating Frequency = PH6 , Charge Pump Cycle = PH5 ,
Only 32.768KHz Crystal oscillator operating, without loading.

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
HALT mode	IHALT1	1.5V Power Mode, VBAT=1.5V		5		uA
	IHALT2	3V Power Mode(BCF=0 => BAK=VL1), VBAT=3.0V, without regulator current		2		
	IHALT3	3V Power Mode(BCF=0 => BAK=VBAT), VBAT=3.0V, without regulator current		10		
STOP mode	ISTOP				1	
Regulator Current	IREG	3V Power Mode, VBAT=3.0V		1		
LVR Current	Ilvr	VBAT=3.0V		0.2		

Note : When RC oscillator function is operating, the current consumption will depend on the frequency of oscillation.

Internal RC Frequency Range

at #1 : Ta=0℃ to 80℃,GND= 0V
at #2 : Ta=-20℃ to 80℃,GND= 0V
at #3 : Ta=-40℃ to 80℃,GND= 0V

Option Mode	BAK	Min.	Typ.	Max.
2MHz (No Temperature Compensation)	1.2V,#1	0.5MHz	1.2MHz	2.2MHz
	1.3V,#2	0.5MHz	1.5MHz	2.5MHz
	1.4V,#3	0.6MHz	1.6MHz	2.6MHz
	1.5V,#3	0.7MHz	1.7MHz	2.7MHz
	1.8V,#3	0.9MHz	1.9MHz	2.9MHz
	2.4V,#3	1.0MHz	2.0MHz	3.0MHz
	3.0V,#3	1.0MHz	2.05MHz	3.0MHz
	3.6V,#3	1.0MHz	2.1MHz	3.0MHz
4MHz (Temperature Compensation)	1.8V,#1	-2%	4.00MHz	+4%
	1.8V,#2	-4%	4.00MHz	+4%
	1.8V,#3	-8%	4.00MHz	+4%

Input Resistance

at#1:VBAT=1.5V(1.5V Power Mode)
at#2:VBAT=3.0V(3V Power Mode)
at Ta=-40℃ to 80℃,GND= 0V

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
"L" Level Hold Tr.(IOC)	Rllh1	Vi=0.2VBAT,#1	10	40	100	KΩ
	Rllh2	Vi=0.2VBAT,#2	10	40	100	
INT,IOA('),B,C,D,E('),SCK(Normal) Pull-Down Tr.	Rnpd1	Vi=VBAT,#1	200	500	1000	
	Rnpd2	Vi=VBAT,#2	200	500	1000	
INT/IOA'/IOE'/SIO(Normal) Pull-up Tr.	Rnpu1	Vi=VBAT,#1	50	200	1000	
	Rnpu2	Vi=VBAT,#2	50	350	1000	
IOA'/IOE'/SIO(Small) Pull-up Tr.	Rspu1	Vi=VBAT,#1	10	40	100	
SCK(Small) Pull-Down Tr.	Rspu2	Vi=VBAT,#2	10	40	100	
RES Pull-Up R	Rres1	Vi= VBAT,#1	10	40	100	
	Rres2	Vi= VBAT,#2	10	40	100	

DC Output Characteristics

at#1:VBAT=1.2V
at#2:VBAT=2.4V
at Ta=-40℃ to 80℃,GND= 0V

Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output ”H” Voltage	Voh1a	Ioh=-100uA,#1	COM1~9& SEG1~23, 28~47 (for DC/OD) IOB~D,F IOE(share with SEG 40 ~43) ELC,ELP ,BZB,BZ(s hare with SEG28~31)	1.0			V
	Voh2a	Ioh=-1mA,#2		2.0			
Output ”L” Voltage	Vol1a	Iol=200uA,#1				0.2	
	Vol2a	Iol=2mA,#2				0.4	
Output ”H” Voltage	Voh1b	Ioh=-200uA,#1	SEG24~27 (for DC/ OD) IOE(share with RFC 3~5,CX2) ELC,ELP ,BZB,BZ(s hare with SIO) SCA,SCL, TXD,SIOX, SIOY,SCK, SSB IOA,RFC0 ~5,INT&CX /2(Vol only)	1.0			
	Voh2b	Ioh=-3mA,#2		2.0			
Output ”L” Voltage	Vol1b	Iol=400uA,#1				0.2	
	Vol2b	Iol=5mA,#2				0.4	
Output ”L” Voltage	Vol2c	Iol=40mA,#2	COM1~9 (for LED)			0.6	

Segment Driver Output Characteristics

at#1:VL1=1.2V
at#2:VL2=2.4V
at#3:VL1=1.05V
at#4:VL2=2.10V
at#5:VL3=2.4V

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit
Static display Mode							
Output ”H” Voltage	Voh12f	Ioh=-1uA,#1,#2	SEG-n	2.2			V
	Voh34f	Ioh=-1uA,#3		1.90			
Output ”L” Voltage	Vol12f	Iol=1uA,#1,#2				0.2	
	Vol34f	Iol=1uA,#3,#4				0.2	
Output ”H” Voltage	Voh12g	Ioh=-10uA,#1,#2	COM-n	2.2			
	Voh34g	Ioh=-10uA,#3		1.90			
Output ”L” Voltage	Vol12g	Iol=10uA,#1,#2				0.2	
	Vol34g	Iol=10uA,#3				0.2	
1/2 Bias display Mode							
Output ”H” Voltage	Voh12f	Ioh=-1uA,#1,#2	SEG-n	2.2			V
	Voh34f	Ioh=-1uA,#3		1.90			
Output ”L” Voltage	Vol12f	Iol=1uA,#1,#2				0.2	
	Vol34f	Iol=1uA,#3,#4				0.2	
Output ”H” Voltage	Voh12g	Ioh=-10uA,#1,#2	COM-n	2.2			
	Voh34g	Ioh=-10uA,#3		1.90			
Output ”M1” Voltage	Vom112g	Iol/h=+/-10uA,#1,#2		1.0		1.4	
	Vom134g	Iol/h=+/-10uA,#3		0.85		1.25	
Output ”L” Voltage	Vol12g	Iol=10uA,#1,#2				0.2	
	Vol34g	Iol=10uA,#3				0.2	
1/3 Bias display Mode							
Output ”H” Voltage	Voh12h	Ioh=-1uA,#1,#2	SEG-n	3.4			V
	Voh34h	Ioh=-1uA,#3,#4		2.95			
	Voh5h	Ioh=-1uA,#5		2.2			
Output ”M1” Voltage	Vom112h	Iol/h=+/-1uA,#1,#2		1.0		1.4	
	Vom134h	Iol/h=+/-1uA,#3,#4		0.85		1.25	
	Vom15h	*Iol/h=+/-1uA,#5*		*0.6*		*1.0*	
Output ”M2” Voltage	Vom212h	Iol/h=+/-1uA,#1,#2		2.2		2.6	
	Vom234h	Iol/h=+/-1uA,#3,#4		1.95		2.30	
	Vom25h	Iol/h=+/-1uA,#5		1.4		1.8	
Output ”L” Voltage	Vol12h	Iol=1uA,#1,#2				0.2	
	Vol34h	Iol=1uA,#3,#4				0.2	
	Vol5h	Iol=1uA,#5				0.2	
Output ”H” Voltage	Voh12i	Ioh=-10uA,#1,#2	COM-n	3.4			
	Voh34i	Ioh=-10uA,#3,#4		2.95			
	Voh5i	Ioh=-1uA,#5		2.2			
Output ”M1” Voltage	Vom112i	Iol/h=+/-10uA,#1,#2		1.0		1.4	
	Vom134i	Iol/h=+/-10uA,#3,#4		0.85		1.25	
	Vom15i	Iol/h=+/-10uA,#5		0.6		1.0	
Output ”M2” Voltage	Vom212i	Iol/h=+/-10uA,#1,#2		2.2		2.6	
	Vom234i	Iol/h=+/-10uA,#3,#4		1.90		2.30	
	Vom25i	Iol/h=+/-10uA,#5		1.4		1.8	
Output ”L” Voltage	Vol12i	Iol=10uA,#1,#2				0.2	
	Vol34i	Iol=10uA,#3,#4				0.2	
	Vol5i	Iol=10uA,#5				0.2	

Regulator & Low-Battery-Detect Circuit Characteristics

VREG & VDL <= VBAT=1.5V/3.0V for TM87ML28L/H

at Ta=-20℃ to 70℃,GND= 0V

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
VREG regulator output for BAK & initial = 1.20V	VREG	VDX4~0 = 1F	-4.5	2.75	+4.5	%
		VDX4~0 = 1E		2.70		
		VDX4~0 = 1D		2.65		
		VDX4~0 = 1C		2.60		
		VDX4~0 = 1B		2.55		
		VDX4~0 = 1A		2.50		
		VDX4~0 = 19		2.45		
		VDX4~0 = 18		2.40		
		VDX4~0 = 17		2.35		
		VDX4~0 = 16		2.30		
		VDX4~0 = 15		2.25		
		VDX4~0 = 14		2.20		
		VDX4~0 = 13		2.15		
		VDX4~0 = 12		2.10		
		VDX4~0 = 11		2.05		
		VDX4~0 = 10		2.00		
		VDX4~0 = 0F		1.95		
		VDX4~0 = 0E		1.90		
		VDX4~0 = 0D		1.85		
		VDX4~0 = 0C		1.80		
		VDX4~0 = 0B		1.75		
		VDX4~0 = 0A		1.70		
		VDX4~0 = 09		1.65		
		VDX4~0 = 08		1.60		
		VDX4~0 = 07		1.55		
		VDX4~0 = 06		1.50		
		VDX4~0 = 05		1.45		
		VDX4~0 = 04		1.40		
		VDX4~0 = 03		1.35		
		VDX4~0 = 02		1.30		
		VDX4~0 = 01		1.25		
		VDX4~0 = 00*		1.20*		
VDL regulator output for VL2 or BAK & for 3V Power Mode only & initial = 2.10V	VDL	VDL3~0 = F	-4.5	2.55	+4.5	%
		VDL3~0 = E		2.50		
		VDL3~0 = D		2.45		
		VDL3~0 = C		2.40		
		VDL3~0 = B		2.35		
		VDL3~0 = A		2.30		
		VDL3~0 = 9		2.25		
		VDL3~0 = 8		2.20		
		VDL3~0 = 7		2.15		
		VDL3~0 = 6*		2.10*		
		VDL3~0 = 5		2.05		
		VDL3~0 = 4		2.00		
		VDL3~0 = 3		1.95		
		VDL3~0 = 2		1.90		
		VDL3~0 = 1		1.85		
		VDL3~0 = 0		1.80		

VDL regulator output for VL1 & initial = 1.05V	VDL	VDL3~0 = F	-4.5	1.70	+4.5	%
		VDL3~0 = E		1.65		
		VDL3~0 = D		1.60		
		VDL3~0 = C		1.55		
		VDL3~0 = B		1.50		
		VDL3~0 = A		1.45		
		VDL3~0 = 9		1.40		
		VDL3~0 = 8		1.35		
		VDL3~0 = 7		1.30		
		VDL3~0 = 6		1.25		
		VDL3~0 = 5		1.20		
		VDL3~0 = 4		1.15		
		VDL3~0 = 3		1.10		
		VDL3~0 = 2*		1.05*		
		VDL3~0 = 1		1.00		
		VDL3~0 = 0		0.95		
VREG Stable time, BAK with 0.1uF Capacitor	TREG				600	ms
LBD voltage For 3V Power Mode only & initial = 2.4V	VLBD	LBD3~0 = F	-0.10	2.75	+0.10	V
		LBD3~0 = E		2.70		
		LBD3~0 = D		2.65		
		LBD3~0 = C		2.60		
		LBD3~0 = B		2.55		
		LBD3~0 = A		2.50		
		LBD3~0 = 9		2.45		
		LBD3~0 = 8*		2.40*		
		LBD3~0 = 7		2.35		
		LBD3~0 = 6		2.30		
		LBD3~0 = 5		2.25		
		LBD3~0 = 4		2.20		
		LBD3~0 = 3		2.15		
		LBD3~0 = 2		2.10		
		LBD3~0 = 1		2.05		
		LBD3~0 = 0		2.00		
LBD voltage For 3V Power Mode & initial = 1.95V(*2) (Spec. for LBD3~0=8~F only)	VLBD	LBD3~0 = F	-0.10	2.10	+0.10	V
		LBD3~0 = E		2.05		
		LBD3~0 = D		2.00		
		LBD3~0 = C*2		1.95*2		
		LBD3~0 = B		1.90		
		LBD3~0 = A		1.85		
		LBD3~0 = 9		1.80		
		LBD3~0 = 8		1.75		
LBD voltage For 1.5 Power Mode & initial = 1.35 (*1) (Spec. for LBD3~0=0~7 only)		LBD3~0 = 7		1.70		
		LBD3~0 = 6		1.65		
		LBD3~0 = 5		1.60		
		LBD3~0 = 4		1.55		
		LBD3~0 = 3		1.50		
		LBD3~0 = 2		1.45		
		LBD3~0 = 1		1.40		
		LBD3~0 = 0*1		1.35*1		
LBD circuit response time	TLBD				100	us

Low-Voltage-Reset Circuit Characteristics

(VBAT=3.0V for Li-B GND=0V)
at Ta=-40℃ to 80℃,GND= 0V

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
Reset Voltage	Vlvr		0.90	1.50	2.55	V

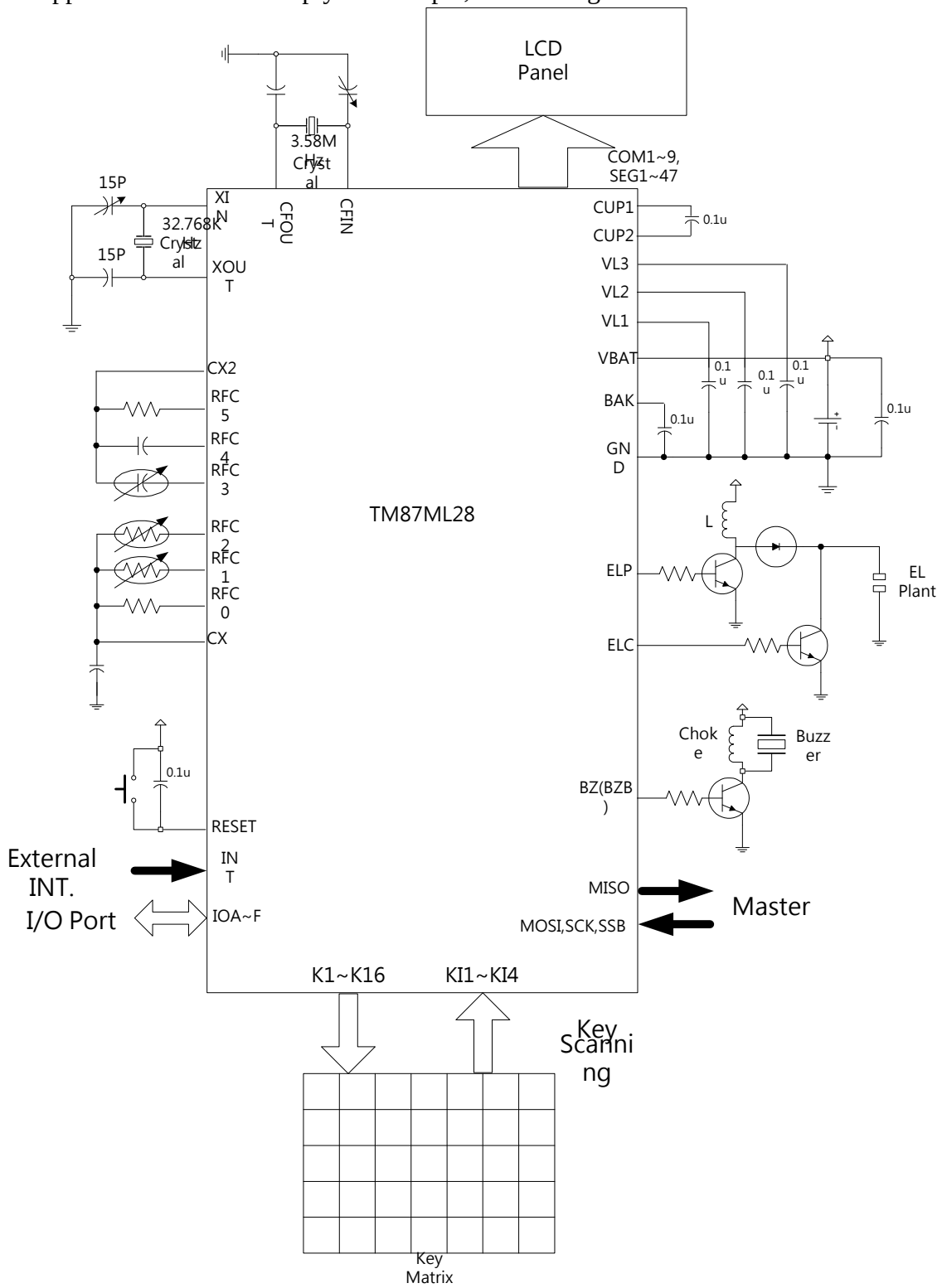
Table ROM Word Write by Instruction of PTR

at Ta=-20℃ to 80℃,GND= 0V

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
Write Voltage	BAK	BAK=VREG	2.1	2.2	2.3	V
Write Time	Tptr				50	ms

TYPICAL APPLICATION CIRCUIT

This application circuit is simply an example, and is not guaranteed to work.



Regulator used for BAK & VL mode, 1/3 Bias, 1/9 Duty

Appendix A TM87ML28 Instruction Table

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
IDC&		0000 0001 0100 1010	HL	←HL+1	
LCT	Lz,Ry	0000 001Z ZZZZ YYYY	(Lz)	← (7SEG ← (Ry))	
LCB	Lz,Ry	0000 010Z ZZZZ YYYY	(Lz)	← (7SEG ← (Ry)) Blank Zero	
LCP	Lz,Ry	0000 011Z ZZZZ YYYY	(Lz)	← (Ry) & AC	
LCD LCD#	Lz,@HL	0000 100Z ZZZZ B000	(Lz) '#' : HL	← T(@HL) ← HL+1	' ' : B3=0 '#' : B3=1
LCT LCT#	Lz,@HL	0000 100Z ZZZZ B001	(Lz) "#' : HL	← (7SEG ← (@HL)) ← HL+1	' ' : B3=0 '#' : B3=1
LCB LCB#	Lz,@HL	0000 100Z ZZZZ B010	(Lz) '#' : HL	← (7SEG ← (@HL)) ← HL+1 Blank Zero	' ' : B3=0 '#' : B3=1
LCP LCP#	Lz,@HL	0000 100Z ZZZZ B011	(Lz) '#' : HL	← (@HL) & AC ← HL+1	' ' : B3=0 '#' : B3=1
LCDX	D	0000 1000 DD00 0100	Multi-Lz D=00 D=01 D=10 D=11	← T@HL : Multi-Lz=00H~0FH : Multi-Lz=10H~1FH : Multi-Lz=20H~2FH : Multi-Lz=30H~3FH	
LCTX	D	0000 1000 DD00 0101	Multi-Lz	← (7SEG ← @HL)	
LCBX	D	0000 1000 DD00 0110	Multi-Lz	← (7SEG ← @HL) Blank Zero	
LCPX	D	0000 1000 DD00 0111	Multi-Lz	← @HL & AC	
OPA	Rx	0000 1010 0XXX XXXX	Port(A)	← (Rx)	
OPAS	Rx,D	0000 1011 DXXX XXXX	A1,2,3,4	← (Rx)0,(Rx)1,D,Pulse	
OPB	Rx	0000 1100 0XXX XXXX	Port(B)	← (Rx)	
OPC	Rx	0000 1101 0XXX XXXX	Port(C)	← (Rx)	
OPD	Rx	0000 1110 0XXX XXXX	Port(D)	← (Rx)	
OPE	Rx	0000 1110 1XXX XXXX	Port(E)	← (Rx)	
FRQ	D,Rx	0001 00DD 0XXX XXXX	FREQ D=00 D=01 D=10 D=11	← (Rx) & AC : 1/4 Duty : 1/3 Duty : 1/2 Duty : 1/1 Duty	
FRQ FRQ#	D,@HL	0001 01DD 0000 B000	FREQ '#' : HL	←T(@HL) ← HL+1	' ' : B3=0 '#' : B3=1
FRQX	D,X	0001 10DD XXXX XXXX	FREQ	← X	
MVL	Rx	0001 1100 0XXX XXXX	IDBF0~3	← (Rx)	
MVH	Rx	0001 1101 0XXX XXXX	IDBF4~7	← (Rx)	
MVU	Rx	0001 1110 0XXX XXXX	IDBF8~11	← (Rx)	
MVV	Rx	0001 1111 0XXX XXXX	IDBF12	← (Rx)0	
ADC ADC*	Rx	0010 000B 0XXX XXXX	AC '*' : (Rx)	← (Rx) + AC + CF ← AC	CF

ADC ADC# ADC* ADC*#	@HL	0010 000B 1B00 0000	AC '*' : (@HL) '#' : HL	← (@HL) + AC + CF ← AC ← HL+1	' ' : B8=0 '*' : B8=1 ' ' : B6=0 '#' : B6=1
ADC ADC# ADC* ADC*#	@HL,DA	0010 000B 1B01 0000	AC '*' : (@HL) '#' : HL	←BCD((@HL)+AC+CF) ← AC ← HL+1	
SBC SBC*	Rx	0010 001B 0XXX XXXX	AC '*' : (Rx)	← (Rx) + ACB + CF ← AC	CF ' ' : B8=0
SBC SBC# SBC* SBC*#	@HL	0010 001B 1B00 0000	AC '*' : (@HL) '#' : HL	← (@HL) + ACB + CF ← AC ← HL+1	'*' : B8=1 ' ' : B6=0 '#' : B6=1
SBC SBC# SBC* SBC*#	@HL,DA	0010 001B 1B01 0000	AC '*' : (@HL) '#' : HL	←BCD((@HL)+ACB+CF) ← AC ← HL+1	
ADD ADD*	Rx	0010 010B 0XXX XXXX	AC '*' : (Rx)	← (Rx) + AC ← AC	CF ' ' : B8=0
ADD ADD# ADD* ADD*#	@HL	0010 010B 1B00 0000	AC '*' : (@HL) '#' : HL	← (@HL) + AC ← AC ← HL+1	'*' : B8=1 ' ' : B6=0 '#' : B6=1
ADD ADD# ADD* ADD*#	@HL,DA	0010 010B 1B01 0000	AC '*' : (@HL) '#' : HL	←BCD((@HL)+AC) ← AC ←HL+1	
SUB SUB*	Rx	0010 011B 0XXX XXXX	AC '*' : (Rx)	← (Rx) + ACB + 1 ← AC	CF ' ' : B8=0
SUB SUB# SUB* SUB*#	@HL	0010 011B 1B00 0000	AC '*' : (@HL) '#' : HL	← (@HL) + ACB + 1 ← AC ← HL+1	'*' : B8=1 ' ' : B6=0 '#' : B6=1
SUB SUB# SUB* SUB*#	@HL,DA	0010 011B 1B01 0000	AC '*' : (@HL) '#' : HL	←BCD((@HL)+ACB+1) ← AC ← HL+1	
ADN ADN*	Rx	0010 100B 0XXX XXXX	AC '*' : (Rx)	← (Rx) + AC ← AC	' ' : B8=0 '*' : B8=1
ADN ADN# ADN* ADN*#	@HL	0010 100B 1B00 0000	AC '*' : (@HL) '#' : HL	← (@HL) + AC ← AC ←HL+1	' ' : B6=0 '#' : B6=1
AND	Rx	0010 101B 0XXX XXXX	AC	← (Rx) AND AC	' ' : B8=0

AND* AND AND# AND* AND*#	 @HL	 0010 101B 1B00 0000	'*' : (Rx) AC '*' : (@HL) '#' : HL	← AC ← (@HL) AND AC ← AC ←HL+1	'*' : B8=1 ' ' : B6=0 '#' : B6=1
EOR EOR* EOR EOR# EOR* EOR*#	Rx @HL	0010 110B 0XXX XXXX 0010 110B 1B00 0000	AC '*' : (Rx) AC '*' : (@HL) '#' : HL	← (Rx) EOR AC ← AC ← (@HL) EOR AC ← AC ←HL+1	' ' : B8=0 '*' : B8=1 ' ' : B6=0 '#' : B6=1
OR OR* OR OR# OR* OR*#	Rx @HL	0010 111B 0XXX XXXX 0010 111B 1B00 0000	AC '*' : (Rx) AC '*' : (@HL) '#' : HL	← (Rx) OR AC ← AC ← (@HL) OR AC ← AC ←HL+1	' ' : B8=0 '*' : B8=1 ' ' : B6=0 '#' : B6=1
ADCI	Ry,D	0011 0000 DDDD YYYY	AC	← (Ry) + D + CF	CF
ADCI*	Ry,D	0011 0001 DDDD YYYY	AC,(Ry)	← (Ry) + D + CF	CF
SBCI	Ry,D	0011 0010 DDDD YYYY	AC	← (Ry) + DB + CF	CF
SBCI*	Ry,D	0011 0011 DDDD YYYY	AC,(Ry)	← (Ry) + DB + CF	CF
ADDI	Ry,D	0011 0100 DDDD YYYY	AC	← (Ry) + D	CF
ADDI*	Ry,D	0011 0101 DDDD YYYY	AC,(Ry)	← (Ry) + D	CF
SUBI	Ry,D	0011 0110 DDDD YYYY	AC	← (Ry) + DB + 1	CF
SUBI*	Ry,D	0011 0111 DDDD YYYY	AC,(Ry)	← (Ry) + DB + 1	CF
ADNI	Ry,D	0011 1000 DDDD YYYY	AC	← (Ry) + D	
ADNI*	Ry,D	0011 1001 DDDD YYYY	AC,(Ry)	← (Ry) + D	
ANDI	Ry,D	0011 1010 DDDD YYYY	AC	← (Ry) AND D	
ANDI*	Ry,D	0011 1011 DDDD YYYY	AC,(Ry)	← (Ry) AND D	
EORI	Ry,D	0011 1100 DDDD YYYY	AC	← (Ry) EOR D	
EORI*	Ry,D	0011 1101 DDDD YYYY	AC,(Ry)	← (Ry) EOR D	
ORI	Ry,D	0011 1110 DDDD YYYY	AC	← (Ry) OR D	
ORI*	Ry,D	0011 1111 DDDD YYYY	AC,(Ry)	← (Ry) OR D	
INC* INC* INC*#	Rx @HL	0100 0000 0XXX XXXX 0100 0000 1B00 0000	AC,(Rx) AC,(@HL) '#' : HL	← (Rx) + 1 ← (@HL) + 1 ←HL+1	' ' : B6=0 '#' : B6=1 CF
DEC* DEC* DEC*#	Rx @HL	0100 0001 0XXX XXXX 0100 0001 1B00 0000	AC,(Rx) AC,(@HL) '#' : HL	← (Rx) - 1 ← (@HL) - 1 ←HL+1	' ' : B6=0 '#' : B6=1 CF
MWM	Rm,Ry	0100 0100 MMMM YYYY	Rm	← Ry	
MMW	Ry,Rm	0100 0101 MMMM YYYY	AC,Ry	← Rm	
IPA	Rx	0100 0110 0XXX XXXX	AC,(Rx)	← Port(A)	
IPB	Rx	0100 0110 1XXX XXXX	AC,(Rx)	← Port(B)	
IPC	Rx	0100 0111 0XXX XXXX	AC,(Rx)	← Port(C)	
IPD	Rx	0100 1000 0XXX XXXX	AC,(Rx)	← Port(D)	

IPE	Rx	0100 1000 1XXX XXXX	AC,(Rx)	← Port(E)	
LDS LDS#	@HL,D	0100 1001 1B00 DDDD	AC, (@HL) '#': HL	← D ← HL+1	' ' : B6=0 '#' : B6=1
MAF	Rx	0100 1010 0XXX XXXX	AC,(Rx)	← STS1	B3 : CF B2 : ZERO B1 : SCF12(CX2) *B B0 : SCF11(CX) *B
RTM2L	Rx	0100 1010 1XXX XXXX	AC,(Rx)	← TM2(0~3)	
MSB	Rx	0100 1011 0XXX XXXX	AC,(Rx)	← STS2	B3 : SCF3(DPT) B2 : SCF2(HRx) B1 : SCF1(CPT) B0 : BCF
RTM21	Rx	0100 1011 1XXX XXXX	AC,(Rx)	← TM2(4,5),1(0,1)	
MSC	Rx	0100 1100 0XXX XXXX	AC,(Rx)	← STS3	B3 : SCF7(PDV) B2 : PH15 B1 : SCF5(TM1) B0 : SCF4(INT/SIO)
RTM1H	Rx	0100 1100 1XXX XXXX	AC,(Rx)	← TM1(2~5)	
MCX	Rx	0100 1101 0XXX XXXX	AC,(Rx)	← STS3X	B3 : SCF9(RFC) *A B2 : SCF0(APT) B1 : SCF6(TM2) B0 : SCF8(SKI)
RTM3L	Rx	0100 1101 1XXX XXXX	AC,(Rx)	← TM3(0~3)	
MSD	Rx	0100 1110 0XXX XXXX	AC,(Rx)	← STS4	B3 : PGMF B2 : RFOVF B1 : WDF B0 : CSF
RTM31	Rx	0100 1110 1XXX XXXX	AC,(Rx)	← TM3(4,5), 1(0,1)	
MDX	Rx	0100 1111 0XXX XXXX	AC,(Rx)	← STS4X	B3 : SCF10(TM3) B2 : INT B1 : CX2 B0 : CX
MKI	Rx	0100 1111 1XXX XXXX	AC,Rx	← STS5(KI4~1)	
SR0	Rx	0101 0000 0XXX XXXX	ACn, (Rx)n AC3, (Rx)3	← (Rx)(n+1) ← 0	
SR1	Rx	0101 0000 1XXX XXXX	ACn, (Rx)n AC3, (Rx)3	← (Rx)(n+1) ← 1	
SL0	Rx	0101 0001 0XXX XXXX	ACn, (Rx)n AC0, (Rx)0	← (Rx)(n-1) ← 0	
SL1	Rx	0101 0001 1XXX XXXX	ACn, (Rx)n AC0, (Rx)0	← (Rx)(n-1) ← 1	
RRC RRC RRC#	Rx @HL	0101 0010 0XXX XXXX 0101 0010 1B00 0000	ACn, (Rx)n AC3, (Rx)3 CF ACn, (@HL)n AC3,(@HL)3 CF '#': HL	← (Rx)(n+1) ← CF ← (Rx)0 ← (@HL)(n+1) ← CF ← (@HL)0 ← HL+1	CF ' ' : B6=0 '#' : B6=1
RLC	Rx	0101 0011 0XXX XXXX	ACn, (Rx)n AC0, (Rx)0 CF	← (Rx)(n-1) ← CF ← (Rx)3	CF ' ' : B6=0 '#' : B6=1

RLC RLC#	@HL	0101 0011 1B00 0000	ACn, (@HL)n AC0, (@HL)0 CF '#': HL	← (@HL)(n-1) ← CF ← (@HL)3 ← HL+1	
DAA DAA* DAA* DAA*#	 Rx @HL	0101 0100 0000 0000 0101 0101 0XXX XXXX 0101 0101 1B00 0000	AC AC,(Rx) AC,(@HL) '#' : HL	← BCD(CF,AC) for add. ← BCD(CF,AC) for add. ← BCD(CF,AC) for add. ←HL+1	CF ' ' : B6=0 '#' : B6=1
DAS DAS* DAS* DAS*#	 Rx @HL	0101 0110 0000 0000 0101 0111 0XXX XXXX 0101 0111 1B00 0000	AC AC,(Rx) AC,(@HL) '#' : HL	← BCD(CF,AC) for sub. ← BCD(CF,AC) for sub. ← BCD(CF,AC) for sub. ←HL+1	CF ' ' : B6=0 '#' : B6=1
LDS	Rx,D	0101 1DDD DXXX XXXX	AC,(Rx)	← D	
LDH LDH*	Rx,@HL	0110 000B 0XXX XXXX	AC,(Rx) '*' : HL	← H(T(@HL)) ← HL + 1	' ' : B8=0 '*' : B8=1
LDL LDL*	Rx,@HL	0110 001B 0XXX XXXX	AC,(Rx) '*' : HL	← L(T(@HL)) ← HL + 1	' ' : B8=0 '*' : B8=1
MRF1	Rx	0110 0000 1XXX XXXX	AC,(Rx)	← RFC3-0	
MRF2	Rx	0110 0001 1XXX XXXX	AC,(Rx)	← RFC7-4	
MRF3	Rx	0110 0010 1XXX XXXX	AC,(Rx)	← RFC11-8	
MRF4	Rx	0110 0011 1XXX XXXX	AC,(Rx)	← RFC15-12	
STA STA STA#	Rx @HL	0110 1000 0XXX XXXX 0110 1000 1B00 0000	(Rx) (@HL) '#' : HL	← AC ← AC ← HL+1	' ' : B6=0 '#' : B6=1
LDA LDA LDA#	Rx @HL	0110 1100 0XXX XXXX 0110 1100 1B00 0000	AC AC '#': HL	← (Rx) ← (@HL) ← HL+1	' ' : B6=0 '#' : B6=1
MRA	Rx	0110 1101 0XXX XXXX	CF	← (Rx)3	
MRW MRW#	@HL,Rx	0110 1110 BXXX XXXX	AC,(@HL) '#' : HL	← (Rx) ←HL+1	' ' : B7=0 '#' : B7=1
MWR MWR#	Rx,@HL	0110 1111 BXXX XXXX	AC,(Rx) '#' : HL	← (@HL) ←HL+1	' ' : B7=0 '#' : B7=1
MRW	Ry,Rx	0111 0YYY YXXX XXXX	AC,(Ry)	← (Rx)	
MWR	Rx,Ry	0111 1YYY YXXX XXXX	AC,(Rx)	← (Ry)	
JB0	X	1000 0XXX XXXX XXXX	PC	← X	if AC0 = 1
JB1	X	1000 1XXX XXXX XXXX	PC	← X	if AC1 = 1
JB2	X	1001 0XXX XXXX XXXX	PC	← X	if AC2 = 1
JB3	X	1001 1XXX XXXX XXXX	PC	← X	if AC3 = 1
JNZ	X	1010 0XXX XXXX XXXX	PC	← X	if AC ≠ 0
JNC	X	1010 1XXX XXXX XXXX	PC	← X	if CF = 0
JZ	X	1011 0XXX XXXX XXXX	PC	← X	if AC = 0
JC	X	1011 1XXX XXXX XXXX	PC	← X	if CF = 1
CALL	X	1100 0XXX XXXX XXXX	STACK	← PC + 1	

			PC	← X	
JMP	X	1100 1XXX XXXX XXXX	PC	← X	
SRY	X	1101 0000 00XX XXXX	X5~0	:Set Ry Page (0~6,8~03Fh) for Rx 0~03FFh	Insert by Compiler
ERY	X	1101 0010 00XX XXXX	X5~0	:Enable Ry Page (0~6,8~03Fh) for Rx 0~03FFh Set & Lock	1. Before execute “CLPG (X1=1)”, Page still can be change by executing “ERY” again. 2. Between jump location, can’t have any “ERY/ERX/ELZ/CLPG” instructions. 3. Interrupt will be masked by hardware till all page set be clear by “CLPG”.
SRX	X	1101 0100 0000 0XXX	X2~0	:Set Rx Page (1~7h)	Insert by Compiler
ERX	X	1101 0110 0000 0XXX	X2~0	:Enable Rx Page (1~7h) Set & Lock	1. Before execute “CLPG (X0=1)”, Page still can be change by executing “ERX” again. 2. Between jump location, can’t have any “ERY/ERX/ELZ/CLPG” instructions. 3. Interrupt will be masked by hardware till all page set be clear by “CLPG”.
SLZ	X	1101 0100 0100 000X	X0	:Set Lz Page(1h)	Insert by Compiler
ELZ	X	1101 0110 0100 000X	X0	:Enable Lz Page(1h) Set & Lock	1. Before execute “CLPG (X2=1)”, Page still can be change by executing “ELZ” again. 2. Between jump location, can’t have any “ERY/ERX/ELZ/CLPG” instructions.

					3. Interrupt will be masked by hardware till all page set be clear by “CLPG”.
SPBK	X	1101 0110 1000 00XX	X3~0	:Set POM BANK X=00~03H	Insert by Compiler
CLPG	X	1101 0110 1010 1XXX	X2=1 X1=1 X0=1	:Release Lz Page Lock :Release Ry Page Lock :Release Rx Page Lock	
T2M3X	X	1101 0111 00XX XXXX	X5~0 SD15~12= 1011~1000 0111~0100 0011~0000 SD11~6 SD5~0	: Set Counter 17~12 (Timer3) Value :Ctm=XCLK/INT/CX2/CX :Ctm=PH13/11/7/5 :Ctm=FREQ/PH15/3/9/ : Set Counter 11~6 (Timer1) Value : Set Counter 5~0 (Timer2) Value	If TM3 is merged into TM2 Add. “SETDAT SD” to the next address if TM1 is merged into TM2 XCLK only for SIO
T1XH		1101 0111 0100 0000	SD15~12= 1010~1000 0111~0100 0011~0000 SD11~6/0	:Ctm= INT/CX2/CX :Ctm=PH13/11/7/5 :Ctm=FREQ/PH15/3/9/ : Set Counter 5/11~0 (Timer1) Value if bit1,0 of STE <>/= 01	Add. “SETDAT SD” to the next address
T2XH		1101 0111 0100 0100	SD15~12= 1011~1000 0111~0100 0011~0000 SD11~6 SD11/5~0	:Ctm= XCLK/INT/CX2/CX :Ctm=PH13/11/7/5 :Ctm=FREQ/PH15/3/9/ : Set Counter 11~6 (Timer1) Value : Set Counter 11/5~0 (Timer2) Value if bit1,0 of STE =/<> 10	Add. “SETDAT SD” to the next address if TM1 merge to TM2
T3XH		1101 0111 0100 1000	SD15~12= 1011~1000 0111~0100 0011~0000 SD11~6 SD11/5~0	:Ctm= XCLK/INT/CX2/CX :Ctm=PH13/11/7/5 :Ctm=FREQ/PH15/3/9/ : Set Counter 11~6 (Timer1) Value : Set Counter 11/5~0 (Timer3) Value if bit1,0 of STE =/<> 11	Add. “SETDAT SD” to the next address if TM1 merge to TM3
SPKXH	D	1101 0111 0100 110D	KO16~1	← SETDAT SD(16bits)	Add. “SETDAT SD” to the next address

			D=1 D=0 SD15~0	: KEY_S release by scanning cycle : KEY_S release by normal key scanning : Enable KO16~1=1	
SHLX		1101 0111 0101 1100	IDBF12~0	← SETDAT SD(16bits) SD : 0000~1FFFH	Add. “SETDAT SD” to the next address
CPHLH		1101 0111 0101 1110	(PC+2)	← force “NOP” if SETDAT SD(16bits) = IDBF12~0	Add. “SETDAT SD” to the next address Can’t set ERX/ERY/ ELZ/CLPG to PC+2
CAC	X	1101 0111 0110 XXXX	X>=AC: STACK PC(SET) PC X<AC: PC	 ← PC+X+2 ← PC+AC+1 ← SETDAT SD(16bits) ← PC+X+2	Add. “SETDAT SD” to the next X(<16) Addresses range
JAC	X	1101 0111 0111 XXXX	X>=AC: PC(SET) PC X<AC: PC	 ← PC+AC+1 ← SETDAT SD(16bits) ← PC+X+2	Add. “SETDAT SD” to the next X(<16) Addresses range
T1TH T1TH#	@HL	1101 0111 1000 B000	Timer1 ‘#’ : HL TD15~12= 1010~1000 0111~0100 0011~0000 TD11~6/0	← T(@HL)16bits ← HL+2 :Ctm= INT/CX2/CX :Ctm=PH13/11/7/5 :Ctm=FREQ/PH15/3/9/ : Set Counter 5/11~0 (Timer1) Value if bit1,0 of STE =/<> 10	‘ ‘ : B3=0 ‘#’ : B3=1
T2TH T2TH#	@HL	1101 0111 1001 B000	Timer2(2->1) ‘#’ : HL TD15~12= 1011~1000 0111~0100 0011~0000 TD11~6 TD11/5~0	← T(@HL)16bits ← HL+2 :Ctm= XCLK/INT/CX2/CX :Ctm=PH13/11/7/5 :Ctm=FREQ/PH15/3/9/ : Set Counter 11~6 (Timer1) Value : Set Counter 11/5~0 (Timer2) Value if bit1,0 of STE =/<> 11	‘ ‘ : B3=0 ‘#’ : B3=1 if TM1 merge to TM2
T3TH T3TH#	@HL	1101 0111 1010 B000	Timer3(3->1)	← T(@HL)16bits	‘ ‘ : B3=0 ‘#’ : B3=1

			'#' : HL TD15~12= 1011~1000 0111~0100 0011~0000 TD11~6 TD11/5~0	← HL+2 :Ctm= XCLK/INT/CX2/CX :Ctm=PH13/11/7/5 :Ctm=FREQ/PH15/3/9/ : Set Counter 11~6 (Timer1) Value : Set Counter 11/5~0 (Timer3) Value	if TM1 merge to TM3
SPK**T**H SPK**T**H#	D,@HL	1101 0111 1011 B00D	KO16~1 '#' : HL D=1 D=0 TD15~0	← T(@HL)16bits ← HL+2 : KEY_S release by scanning cycle : KEY_S release by normal key scanning : Enable KO16~1=1	' ' : B3=0 '#' : B3=1
RVL	Rx	1101 1000 0XXX XXXX	AC,(Rx)	← IDBF0~3	
RVH	Rx	1101 1001 0XXX XXXX	AC,(Rx)	← IDBF4~7	
RVU	Rx	1101 1010 0XXX XXXX	AC,(Rx)	← IDBF8~11	
RVV	Rx	1101 1011 0XXX XXXX	AC,(Rx)0	← IDBF12	
TM3	Rx	1101 1100 0XXX XXXX	Timer3	← (Rx) & AC	
TM3 TM3#	@HL	1101 1101 0000 B000	Timer3 '#' : HL	← T(@HL) ← HL+1	' ' : B3=0 '#' : B3=1
TM3X	X	1101 111X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer3 Value	
TMS	Rx	1110 0000 0XXX XXXX	AC3,2 = 11 AC3,2 = 10 AC3,2 = 01 AC3,2 = 00 AC1,0,PB3~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TMS TMS#	@HL	1110 0001 0000 B000	Timer1 '#' : HL	← T(@HL) ← HL+1	' ' : B3=0 '#' : B3=1
TMSX	X	1110 001X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	

TM2	Rx	1110 0100 0XXX XXXX	Timer2	← (Rx) & AC	
TM2 TM2#	@HL	1110 0101 0000 B000	Timer2 '#' : HL	← T(@HL) ← HL+1	' ' : B3=0 '#' : B3=1
TM2X	X	1110 011X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer2 Value	
SHE	X	1110 1000 X0XX XXX0	X7 X5 X4 X3 X2 X1	: Enable HEF7 : Enable HEF5 : Enable HEF4 : Enable HEF3 : Enable HEF2 : Enable HEF1	TMR3 KEY_S TMR2 PDV INT/SIO TMR1
SIE*	X	1110 1001 XXXX XXXX	X7 X6 X5 X4 X3 X2 X1 X0	: Enable IEF7 : Enable IEF6 : Enable IEF5 : Enable IEF4 : Enable IEF3 : Enable IEF2 : Enable IEF1 : Enable IEF0	TMR3 RFC KEY_S TMR2 PDV INT/SIO TMR1 A,C,DPT
PLC	X	1110 101X XXXX XXXX	X8 X7-0	: Reset PH15~11 : Reset HRF7-0	
SRF	X	1110 1100 00XX XXXX	X5~0 X5 X4 X3 X2 X1 X0	:Enable RFC5~0 Output : Enable CX Control : Enable TM2 Control : Enable Counter : Enable RFC2 Output : Enable RFC1 Output : Enable RFC0 Output	<TYPE B for RFC> <TYPE A for RFC> RFC2=RH RFC1=RT RFC0=RR
SRE	X	1110 1101 0X0X X000	X6 X4 X3	:Enable SRF6(A port) :Enable SRF4(C port) :Enable SRF3(D port)	
FAST	(X)	1110 1110 0000 0XXX	B/SCLK X=7 X=6 X=5 X=4 X=3 X=2 X=1 X=0 or None	: High Speed Clock :B/SCLK=FTOSC/128 :B/SCLK=FTOSC/64 :B/SCLK=FTOSC/32 :B/SCLK=FTOSC/16 :B/SCLK=FTOSC/8 :B/SCLK=FTOSC/4 :B/SCLK=FTOSC/2 :B/SCLK=FTOSC	
SLOW		1110 1110 1000 0000	SCLK	: Low Speed Clock	
CPHL	X	1110 1111 XXXX XXXX	(PC+1)	← force "NOP" if X7~0=IDBF7~0	Can't set ERX/ERY/ELZ/CLPG to PC+1
SPK	Rx	1111 0000 0XXX XXXX	KO1~16	← (Rx) & AC	
SPK SPK#	@HL	1111 0001 0000 B000	KO1~16 '#' : HL	← T (@HL) ← HL+1	' ' : B3=0 '#' : B3=1

SPKX	X	1111 0010 XXXX XXXX	X6=1 X6=0 X7,5,4=000 X7,5,4=001 X7,5,4=010 X7,5,4=10X X7,5,4=110 X7,5,4=111	: KEY_S release by scanning cycle : KEY_S release by normal key scanning : Set one of KO1~16 =1 by X3~0 : Set all = 1 : Set all Hi-z : Set eight of KO1~16 =1 by X3 X3=0 => KO1~8 X3=1 => KO9~16 : Set four of KO1~16 =1 by X3,2 X3,2=00 => KO1~4 X3,2=01 => KO5~8 X3,2=10 => KO9~12 X3,2=11 => KO13~16 : Set two of KO1~16 =1 by X3,2,1 X3~1=000=>KO1,2 X3~1=001=>KO3,4 X3~1=010=>KO5,6 X3~1=011=>KO7,8 X3~1=100=>KO9,10 X3~1=101=>KO11,12 X3~1=110=>KO13,14 X3~1=111=>KO15,16	
RTS		1111 0100 0000 0000	PC	← STACK (CALL Return)	
MRI MRI#	X	1111 0100 0001 B0XX	X1,0=00 X1,0=01 X1,0=10 X1,0=11 '#' : HL	: (RILH)3~0 ←(@HL) : (RILH)7~4 ←(@HL) : (RILH)11~8 ←(@HL) : (RILH)15~12 ←(@HL) : ← HL+1	' ' : B3=0 '#' : B3=1
SBZ	X	1111 0100 0010 00XX	 X1=0 X1=1 X0=0 X0=1	<set BZB Pad> :BZB :FREQB only <set BZ Pad> :BZ :FREQ only	 Initial Initial
SRP	X	1111 0100 0010 1XXX	X2 X1 X0	: Enable Timer3 repeat set if RL3=1 : Enable Timer2 repeat set if RL2=1 : Enable Timer1 repeat set if RL1=1	
STM	X	1111 0100 0011 00XX	X1,0=00 X1,0=01 X1,0=10 X1,0=11	:TM1,2,3 is independent : TM2(2=>1) : TM3(3=>1) : TM2(2=>1=>3)	Initial(X1,0=00)
DISTM	X	1111 0100 0011 1XXX	X2~0	: Disable TM3~1 Count	

SCNT	X	1111 0100 01XX XX00	X5=0 X5=1 X4=0 X4=1 X3,2=00 X3,2=01 X3,2=10 X3,2=11	: Enable CX set : Enable CX2 set Counter clock source for not CX/2 control Mode : CX/2 : FREQ Control Mode : Software : TM2 : CX/2 – One Cycle : CX/2 – High Level	<TYEP B for RFC> initial
SCC	X	1111 0100 1XXX XXXX	X6 = 1 X6 = 0 X5 = 1 X4 = 1 X3 = 1 X2,1,0=001 X2,1,0=010 X2,1,0=100	: Cfq = XCLK : Cfq = PH0 :Set P(A) Cch : Set P(C) Cch : Set P(D) Cch : Cch = PH10 : Cch = PH8 : Cch = PH6	
SCA	X	1111 0101 00XX X000	X5 X4 X3	: Enable SEF5(A1-4) : Enable SEF4(C1-4) : Enable SEF3(D1-4)	
SPE	X	1111 0101 010X XXXX	X4 X3~0	: Set E4-1 Pull-Low : Set E4-1 I/O	
SCX	X	1111 0101 0110 00XX	X1 X0	: Enable SEF1(CX2) : Enable SEF0(CX)	<TYEP B for RFC>
SXCLK	X	1111 0101 0110 01XX	X1 X0	: Force clock source of RFC 16bits counter to XCLK : .0/1 to set XCLK=BCLK/CFOSC	
STE	X	1111 0101 0110 1XXX	X2 X1,0=00 X1,0=01 X1,0=10 X1,0=11	: Replace timer1 read of RTM by extension bits & replace timer2 read of RTM by timer1 bits if X1,0=01 : TM1,2,3 is normal 6bits : TM1=>12bits(STM:00) : TM2=>12bits(STM:X0) : TM3=>12bits(STM:0X)	Initial(X2~0=000)
ST3OV	X	1111 0101 0111 01XX	X1 X0	: Mask one cycle of Ctm2 when Timer3 overflow : Mask one cycle of Cfq when Timer3 overflow	
ADJ	X	1111 0101 0111 1XXX	X2 X1,0=00 X1,0=01 X1,0=10 X1,0=11	: 0/1 to inc./dec. one PH0 cycle for PDV when Timer overflow set by X1,0 : Normal PDV : Adjust PDV by TM1 : Adjust PDV by TM2 : Adjust PDV by TM3	

SPA	X	1111 0101 100X XXXX	X4 X3~0	: Set A4-1 Pull-Low : Set A4-1 I/O	
SPB	X	1111 0101 101X XXXX	X4 X3~0	: Set B4-1 Pull-Low : Set B4-1 I/O	
SPC	X	1111 0101 110X XXXX	X4 X3-0	: Set C4-1 Pull-Low / Low-Level-Hold : Set C4-1 I/O	
SPD	X	1111 0101 111X XXXX	X4 X3-0	: Set D4-1 Pull-Low : Set D4-1 I/O	
SF	X	1111 0110 XXXX XXXX	X7 X6 X5 X4 X3 X2 X1 X0	: Reload 1 Set : Reload 3 Set : Enable all Timer Counter update & latch : WDT Enable : HALT after EL : EL LIGHT On : BCF Set : CF Set	
RF	X	1111 0111 XXXX 0XXX	X7 X6 X5 X4 X2 X1 X0	: Reload 1 Reset : Reload 3 Reset : Disable all Timer Counter latch : WDT Reset : EL LIGHT Off : BCF Reset : CF Reset	
ELC	X	1111 10XX XXXX XXXX	(ELP) X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=000 X9,5,4=101 X9,5,4=100 X9,5,4=x11 X9,5,4=x10 X9,5,4=001 X9,5,4=000 (ELC) X3,2=11 X3,2=10 X3,2=01 X3,2=00 X1,0=11 X1,0=10 X1,0=01 X1,0=00	 BCLK/8 BCLK/4 BCLK/2 BCLK FREQB PH0 2/3 3/4 1/1 1/2 1/3 1/4 PH5 PH6 PH7 PH8 1/1 1/2 1/3 1/4	
ALM	X	1111 110X XXXX XXXX	X8,7,6=111 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000	: FREQ : DC1 : PH3 : PH4 : PH5 : DC0	

			X5~0	← PH15~10	
SF2	X	1111 1110 0XXX XXXX	X6 X5 X3 X2 X1 X0	:Enable CX2 Counter :Enable CX Counter : Enable INT powerful Pull-low : Close all Segments : Dis-ENX Set : Reload 2 Set	*B *B
RF2	X	1111 1110 1XXX XXXX	X6 X5 X3 X2 X1 X0	:Disable CX2 Counter :Disable CX Counter : Disable INT powerful Pull-low : Release Segments : Dis-ENX Reset : Reload 2 Reset	*B *B
HALT		1111 1111 0000 0000	Halt Operation		
PTR		1111 1111 0111 1111	T(@HL)	←RILH	
STOP		1111 1111 1000 0000	Stop Operation		

*A : TYPE A for RFC
*B : TYPE B for RFC

Symbol Description

AC : Accumulator
ACB : Invert of Accumulator
ACn : Accumulator bit n
X : Address or Set data
Rx : Address of Data RAM
(Rx)n : Bit n of (Rx)
Ry : Address of working register
BCF : Back-up Flag
IEFn : Interrupt Enable Flag
HRFn : HALT Release Flag
HEFn : HALT Release Enable Flag
TMR : Timer Overflow Release Flag
Ctm : Clock Source of Timer
Lz : Address of LCD data
RFOVF : RFC Overflow Flag
MUI : Multiplication Input Register
@HL : Address assigned by Index Register
D : Immediate Data
DB : Invert of Immediate Data
PC : Program Counter
CF : Carry Flag
ZERO : Zero Flag
WDF : Watch-Dog Timer Enable Flag
PDV : Pre-Divider
BCLK : System clock stop only in STOP condition
SEFn : Switch Enable Flag
SRFn : STOP Release Enable Flag
SCFn : Start Condition Flag
Cch : Clock Source of Chattering Detector
Cfq : Clock Source of Frequency Generator
FREQ : Frequency Generator setting Value
( ) : Content of Address Register
MU : Multiplication High nibble Result Register
HL : Index Register
H(T@HL): High Nibble of Index ROM data L(T@HL): Low Nibble of Index ROM Data
IDBF : Content of Index Register
T@HL : Index ROM address assigned by Index Register
CSF : Clock Source Flag
FTOSC : Fast Oscillation clock
DA : BCD for result
PGMF : Program BUSY or WR-FAIL Flag

(@HL) : 4bits data type for Data RAM
T(@HL) : 8 bits data type for Index ROM
T(@HL)16bits : 16 bits data type for Index ROM
HL+1 : +1 to index address bit0
HL+2 : mask index address bit0, and +1 to bit1

MWM/MMW Rm Assignment

Rm	R/W	Instruction	BIT3	BIT2	BIT1	BIT0
0	R	MMW Ry,0	IPF3	IPF2	IPF1	IPF0
	W	MWM 0,Ry	OPF3	OPF2	OPF1	OPF0
1	W	MWM 1,Ry	SPF3	SPF2	SPF1	SPF0
2	R	MMW Ry,2	SDAT3	SDAT2	SDAT1	SDAT0
	W	MWM 2,Ry				
3	R	MMW Ry,3	SDAT7	SDAT6	SDAT5	SDAT4
	W	MWM 3,Ry				
4	W	MWM 4,Ry	SCR3	SCR2	SCR1	SCR0
5	<W> I2C UART SPI	MWM 5,Ry	<SCTL3> I2CEN UARTEN SPIEN	<SCTL2> STRSTP REN MSTR	<SCTL1> START RENRLS BIDIROE	<SCTL0> STOP TB8 LSBF
6	<R> I2C UART SPI	MMW Ry,6	<SSTA3> ACTF RCVOVF /TXOF RCVOVF	<SSTA2> ACKF RCVBF /TXSF RCVBF	<SSTA1> EAF RB8F SSI	SBUSY
	<W> I2C UART SPI	MWM 6,Ry	<SUTI3> SDOCHK TXDCHK TXOCHK	<SUTI2> ACKOSTP CLRXF CLRXF	<SUTI1> WTACKI0 RXCK SSOE	<SUTI0> MKACKI TXCK FSNSS0
7	<R> I2C UART SPI	MMW Ry,7	<SSCF3> IRQF RXSF MSF	<SSCF2> EROF RXBF WCOF/EROF	<SSCF1> TRBF TXBF TRBF	INTF
	<W> I2C UART SPI	MWM 7,Ry	<SSRE3> IRQFEN RXSFEN MSFEN	<SSRE2> EROFEN RXBFEN WCOFEN /EROFEN	<SSRE1> TRBFEN TXBFEN TRBFEN	INTFEN
8	W	MWM 8,Ry	SIOTYP2	SIOTYP1	DSIOPHL	SPLF
9	R	MMW Ry,9	-	-	VDX4	LBF
	W	MWM 9,Ry	0	0		ENLBD
A	R	MMW Ry,A	VDL3	VDL2	VDL1	VDL0
	W	MWM A,Ry				
B	R	MMW Ry,B	LBD3	LBD2	LBD1	LBD0
	W	MWM B,Ry				
C	<W> I2C UART SPI	MWM C,Ry	<SIO3> 0 0 1	<SIO2> 0 1 CPOL	<SIO1> 0 TRB8 CPHA	<SIO0> 1 UART1W SPBIR
D,E	Don't Use					
F	R	MMW Ry,F	VDX3	VDX2	VDX1	VDX0
	W	MWM F,Ry				

IPF3~0 : IOF4~1 input Data.
OPF3~0 : set IOF4~1 output data.
SPF3~0 : 1 for set IOF4~1 to Output(initial value = 0000).
SPLF : 1 for enable IOF4~1 Pull-low(initial value = 1).

SDAT7~0 : SIO Transmit and Receive Data.
Read SDAT7~4 register will clear RCVOVF & RCVBF.
Write data to SDAT7~4 register will start a transfer in master mode.

SCR3~0 : SIO clock source(no initial value).
SCR3=0 : enable set SXCLK Clock Rate by SCR2~0
000 => XCLK/2(XCLK/4 for I2C)
001 => XCLK/4(XCLK/8 for I2C)
010 => XCLK/8(XCLK/16 for I2C)
011 => XCLK/16(XCLK/32 for I2C)
100 => XCLK/32(XCLK/64 for I2C)
101 => XCLK/64(XCLK/128 for I2C)
110 => XCLK/128(XCLK/256 for I2C)
111 => XCLK/256(XCLK/2 for I2C)
SCR3,2=10(11) : enable set TX&RX(set RX independently in UART mode) clock by SCR1,0 (SPI & I2C don't care RX clock)
00 => SXCLK(baud rate = Fsxclk for I2C , Fsxclk/16 for UART , Fsxclk for SPI))
01 => FREQ(baud rate = Ffreq/2 for I2C , Ffreq/16 for UART , Ffreq for SPI)
10 => TM2(baud rate = Ftm2ov/2 for I2C , Ftm2ov/16 for UART , Ftm2ov for SPI)
11 => TM3(baud rate = Ftm3ov/2 for I2C , Ftm3ov/16 for UART , Ftm3ov for SPI)
SCR3,2=11(RX) is no use for I2C & SPI.
tm2ov : timer2 overflow rate = F(Ctm2) / (timer2 set value+1)
tm3ov : timer3 overflow rate = F(Ctm3) / (timer3 set value+1)

If no use FREQ/TM2/TM3 for SCR of SIO & active for other function, set SCR before enter SIO Mode to sure save current.
When set SCR=FREQ, disable FREQ for other function before enter SIO mode to save current & control FREQ by SIO, execute FRQ(X) instruction to set Cfq=XCLK for synchronizing with instruction timing & initial state before enable SIO mode.
Before set SCR=TM2/TM3, set Ctm2/Ctm3=XCLK to force TMRL2/3=1 & synchronizing with instruction timing & control TM2/3 by SIO

<SCTL3~0> : enable & options for SIO(initial value = 0000)
<SCTL0> : 1 for set I2C(STOP) if I2CEN=1.
: used for UART(TB8) to set 9th transmit data bit in the mode of TRB8=1
: 1/0 for set SPI(LSBF) to set data transfer first by LSB/MSB
<SCTL1> : 1 for set I2C(START) if I2CEN=1.
for set UART(RENRLS)=1 to disable receive interrupt received if "stop bit" / "9th data bit" is 0 in the mode of TRB8=0/1.
for set SPI(BIDIROE)=1 to enable MOSI/MISO output for Master/Slave Mode in the Bidirectional mode of operation (SPBIR=1).
<SCTL2> : 1 for set I2C(STRSTP) if I2CEN=1.
for set UART(REN)=1 to enable receive by RXD/TXD pin when UART1W=0/1.
for set SPI(MSTR)=1/0 to enter Master/Slave mode
<SCTL3> : 1 for enable I2C/UART/SPI mode

<SCTL2~0> for I2C (SCTL3=1) :

STRSTP	START	STOP	Description
X	0	0	Nothing
0	0	1	Sent STOP bit after ACKI/ACKO bit by WDATH/RDATH for write/read mode.
0	1	0	Sent START bit before MSB of data by WDATH
0	1	1	Sent START bit before MSB of data by WDATH & sent STOP bit after ACKI/ACKO bit for LSB of data =0/1.
1	0	1	Direct sent STOP bit
1	1	0	Direct sent START bit & force to Write Mode(don't care LSB=1) after write SDAT7~4.
1	1	1	Direct sent START & STOP bits

SBUSY : SIO BUSY Flag(Read Only & set by H/W when a SIO transfer in in progress)

<SSTA1> : for I2C(EAF) to read external active flag by IRQ or others master active.(Need to sure IRQ output delay > 1/2 cycle of SCL after SDA:0->1 @ SCL=1 for SIOTYP=11 mode)
for UART RB8 Flag if set TRB8=1.
for SPI(SSI) to read SSB input invert state.

ACKF : for I2C ACKI Flag, and ACKF=1 if ACKI fail. H/W auto-sent stop bit & set EROF=1 by EROFEN=1 if ACKF=1 & MKACKI=0.

ACTF : for I2C Active Flag, and ACTF=1 from start to stop.

RCVBF : for UART/SPI Receive Buffer Full Flag(Set by H/W at the end of a data transfer, and set SCTL3=0 or write CLRBF=1 or read the register of SDAT7~4 will clear this flag). In UART mode, enable this flag by set TXDCHK=0.

RCVOVF : for UART/SPI Receive Buffer Overrun Flag(Set by H/W at the end of a data transfer, and set SCTL3=0 or write CLROVF=1 or read the register of SDAT7~4 will clear this flag). In UART mode, enable this flag by set TXDCHK=0.

TXSF : for UART TXD Start Flag (Set by H/W if TXD have falling edge happen when TX in standby state & REN=0 in UART1W=1 mode, and set SCTL3=0 or write CLRXF=1 or write the register of SDAT7~4 will clear this flag.), only enable this flag by set TXDCHK=1 in UART mode.

TXOF : for UART TXD Output Fail Flag(Set by H/W if output data & start bit don't match with TXD pin, and set SCTL3=0 or write CLRXF=1 or write the register of SDAT7~4 will clear this flag.), only enable this flag by set TXDCHK=1 in UART mode.

<SUTI3~0> : Utility option & function for SIO(initial value = 0000)

<SUTI0> : for set I2C(MKACKI)=1 to disable generate STOP bit & EROF if ACKI=High, but still make ACKF=1.
for UART(TXCK), set 1 to enable transmit clock always, set TXCK=1 can make all transmit on same trace of Baud Rate if RX count of target IC can't auto-reset by each START bit, TXCK=1 also can avoid error TXOF by race between TX start and SIO clock if RX and TX set same clock source.
for SPI(FSNSS0), set 1 to force SSB pin output low always if SSOE=1.

<SUTI1> : for set I2C(WTACKI0)=1 to wait ACKI=0.
for set UART(RXCK)=1 to enable RX clock always for reduce error START to make RXSF=1 by majority detect.
1 for SPI(SSOE) enable SSB output in master mode.

<SUTI2> : for set I2C(ACKOSTP)=1 to generate STOP bit replace ACKO bit.
for set UART(CLRXF)=1 to clear RCVBF/TXSF & RCVOVF/TXOF
for set SPI(CLRXF)=1 to clear RCVBF & RCVOVF.

<SUTI3> : for set I2C(SDOCHK)=1 to enable EROF function .
for set UART(TXDCHK)=1 to change enable RCVBF/RCVOVF to TXSF/TXOF function, set TXCK=1 to avoid error TXOF=1 if RX and TX have same clock source & one condition of RXCK=1 and SBUSY=1 by RX at start TX.
for set SPI(TXOCHK)=1 to change WCOF to EROF function .

INTF : INT pin interrupt/halt release flag

<SSCF1> : I2C&SPI(TRBF) interrupt/halt release flag for the end of byte data transfer. Read/write SDAT7~4 or set SCTL3=0 or set SSRE1=0 will clear this flag
UART(TXBF) transmit interrupt/halt release flag for the end of byte data transmit, disable by TXOF=1 or TXSF=1. Write SDAT7~4 or set SCTL3=0 or set SSRE1=0 will clear this flag
Enable SSCF1 by set SSRE1=1

<SSCF2> : I2C(EROF) transmit error interrupt/halt release flag for transmit data or ACKO(ACKOSTP=0) no match to SDA. Write SDAT7~4 or set SCTL3=0 or set SSRE2=0 will clear this flag.
UART(RXBF) receive interrupt/halt release flag for the end of byte data receive. Read SDAT7~4 or set SCTL3=0 or set SSRE2=0 will clear this flag.
SPI(WCOF) write collision interrupt/halt release flag by set TXOCHK=0 for writing data to SDAT7~4 when SBUSY=1. Write SDAT7~4 or set SCTL3=0 or set SSRE2=0 will clear this flag.
SPI(EROF) transmit error interrupt/halt release flag by set TXOCHK=1 for transmit data no match to MOSI/MISO output pin. Write SDAT7~4 or set SCTL3=0 or set SSRE2=0 will clear this flag.
Enable SSCF2 by set SSRE2=1.

<SSCF3> : for I2C(IRQF) IRQ(Interrupt Request) interrupt/halt release flag for SDA pin receive falling edge at SCL pin = High when ACTF=0. Write SDAT7~4 or set SCTL3=0 or set SSRE3=0 will clear this flag.
for UART(RXSF) receive start interrupt/halt release flag for start bit of receive . Read SDAT7~4

or set SCTL3=0 or set SSRE3=0 will clear this flag.

for SPI(MSF) is used as :

a. mode fault interrupt/halt release flag with falling edge of SSB in master mode & SSOE=0, auto change to slave mode immediately by H/W.
b. other master active start&stop interrupt/halt release flag with falling & rising edge of SSB in master mode & SSOE=1
c. slave SSB start&stop interrupt/halt release flag with falling&rising edge of SSB at SBUSY=0 in slave mode.
d. slave fault interrupt/halt release flag with rising edge of SSB at SBUSY=1 in slave mode. Auto disable output immediately by H/W. Clear SBUSY & re-work by re-enable SPI.
e. slave SCK start interrupt/halt release flag with first edge of SCK at SBUSY=0 in slave mode & SSB pin no use.

set SCTL3=0 or set SSRE3=0 will clear this flag.

Enable SSCF3 by set SSRE3=1

INTFEN : 1 for enable INT pin interrupt/halt release(initial value = 0).

<SSRE3~1> : SSRE3~1 is forced to 0 when SCTL3=0(initial value = 000).

<SSRE1> : 1 for enable I2C/SPI(TRBF) interrupt/halt release at the end of byte data transfer.
1 for enable UART(TXBF) interrupt/halt release at the end of byte data transmit.

<SSRE2> : 1 for enable I2C(EROFEN) interrupt/halt release if transmit data or ACKO(ACKOSTP=0) no match to SDA
1 for enable UART(RXBF) interrupt/halt release at the end of byte data receive.
1 for enable SPI(WCOFEN) interrupt/halt release(by set TXOCHK=0) if write data to SDAT7~4 when SBUSY=1.
1 for enable SPI(EROFEN) interrupt/halt release(by set TXOCHK=1) if transmit data no match to MOSI/MISO output pin.

<SSRE3> : 1 for I2C(IRQEN) to enable interrupt/halt release by SDA pin receive falling edge at SCL pin = High when ACTF=0.
1 for UART(RXSF) to enable interrupt/halt release by start bit of receive.
1 for SPI(MSFEN) to enable interrupt/halt release by edge of SSB or first edge of SCK if SSB no use.

SIOTYP2,1 : I2C/UART/SPI pins input/output type.

SIOTYP2,1		00(initial)	01	10	11
I2C	SDA(I/O) ,SCL(O)	NOD(I/O) , NOD(O) (standard & for Multi-Master)	NOD(I/O) ,NOD(O) (for Multi-Master)	DC(O)/NOD(I) ,DC(O) (For Single-Master)	DC(I/O) ,DC(O) (For Single-Master)
UART	TXD(I/O) ,RXD(I)	NPOD(O)/NOD(I) ,NOD(I) (standard)	NOD(I/O) ,NOD(I) (For Multi-Master)	DC(O)/NOD(I) ,NOD(I) (For Single-Master & Multi-Slave)	DC(I/O) ,DC(I) (For Single-Master & Single-Slave)
SPI		(standard & for Sub-Master)	(For Multi-Master)	(For Single-Master & Multi-Slave)	(For Single-Master & Single-Slave)
(Master)	MISO(I) ,MOSI(I/O) ,SCK(O) SSB(I/O)	NOD(I) ,NOD(I/O) ,NOD/POD(O) ,DC(I/O)	NOD(I) NOD(I/O) , NOD/POD(O) ,NOD(I/O)	NOD(I) ,NOD(I/O) ,DC(O) ,DC(I/O)	DC(I) ,DC(I/O) ,DC(O) ,DC(I/O)
(Slave)	MISO(I/O) ,MOSI(I) ,SCK(I) ,SSB(I)	NOD(I/O) NOD(I) ,NOD/POD(I) ,DC(I)	NOD(I/O) NOD(I) , NOD/POD(I) ,NOD(I)	NOD(I/O) ,NOD(I) ,DC(I) DC(I)	DC(I/O) ,DC(I) ,DC(I) ,DC(I)*SPI-1

POD : P-type Normal Open Drain.
NOD : N-type Normal Open Drain.
NPOD : N-type Pseudo Open Drain.
DC : CMOS output.

DSIOPHL : 1 for disable I2C/UART/SPI Pull-High/Low Resistance(initial value=0). Control Pull-High/Low Resistance turn on/off by hardware if DSIOPHL=0.

<SIO3~0> : I2C/UART/SPI select & Option (initial value = 0000)
SIO3~0=0001 : for I2C Mode(Master Only)
SIO3~2=01 : for UART Mode & set TRB8/UART1W by SIO1/0
TRB8 : 0/1 for 8/9bits UART.
UART1W : 0/1 for transmit & receive by TXD&RXD / TXD only
In SIOTYP=11 mode, before set REN=1 need to sure input-High start to avoid error by floating.

SIO3=1 : for SPI Mode & set CPOL/CPHA/SPBIR by SIO2/1/0
CPOL : 0/1 for SCK is low/high in idle mode
CPHA : 0/1 for Data sampled on first/second edge of SCK period
SPBIR : 1 for enable Bidirectional mode of operation(SPBIR=1 only enable MOSI/MISO(=>MOMI/SISO) one pin active in Master/Slave mode. In this mode, input is always enable, but output is enable by BIDIROE=1).

LBF : Low Battery Detect Flag.
ENLBD : 1 for generating pulse to enable Low Battery Detect(initial value = 0).

VDL3~0 : Set VDL regulator output voltage.
±50mV for one step voltage.
<VDL for VL2>
Initial value=6h for VDL=2.10V.
VDL=2.55/1.80V for VDL3~0=F/0h.
<VDL for VL1>
Initial value=2h for VDL=1.05V.
VDL=1.70/0.95V for VDL3~0=F/0h.

LBD3~0 : Set Low Battery Detect Voltage.
±50mV for one step voltage.
<LBD for Normal 3V range>
Initial value=8h for LBD=2.40V.
LBD=2.75/2.00V for LBD3~0=F/0h.
<LBD for Low 3V range>
Initial value=Ch for LBD=1.95V.
LBD=2.10/1.75V for LBD3~0=F/8h.
<LBD for 1.5V>
Initial value=0h for LBD=1.35V.
LBD=1.70/1.35V for LBD3~0=7/0h.

VDX4~0 : Set VREG regulator output voltage.
Initial value=00h for VREG=1.20V.
VREG=2.75/1.20V for VDX4~0=1F/00h.