TM57M5620

TM57M5625

TM57M5640

TM57M5645

DATA SHEET

Rev 0.96

AMENDMENT HISTORY

Version	Date	Description
0.90	Sep, 2019	New Release.
0.91	Feb, 2020	Add information about wake up function in Features chapter Add more information in Die pad list. Add SSOP48 package.
0.92	Apr, 2020	M5625 / M5645 under the Feature and Electrical Characteristics chapter, the working voltage LVR ~ 1.8V is changed to LVRC ~ 1.8V
0.93	May, 2020	1. Remove PD3 ~ PD0, PB3 ~ PB0 open-drain function 2. Corrected some package pin information
0.94	Jun, 2020	Added SRC 1.5V, 1.3V electrical characteristics information
0.95	Nov, 2020	1. Modify SRC electrical characteristics information 2. Add LBD suggested delay time
0.96	Sep, 2021	1. Disable SIRC after power-on (p.29) 2. Timer0 block diagram errata (p.40)

CONTESTS

FAMILY OVERVIEW

P/N	Typ. V_{BAT}	MTP ROM	RAM (bytes)	I/O (Max.)	RFC	Timers	8-bit PWM	LCD S x C (Max.)	LCD Bias	Time-piece current
TM57M5610	3.0V	1Kx14	96	12	3-ch	8-bit x1 21-bit x1	x1	12 x 3 11 x 4	1/2	1uA
TM57M5615	1.5V									1.5uA
TM57M5620	3.0V	2Kx14	176	16	4-ch	8-bit x2 21-bit x1	x2	28 x 4	1/3	3uA
TM57M5625	1.5V							26 x 4	1/2, 1/3	2uA
TM57M5640	3.0V	4Kx14	336	20	4-ch	8-bit x2 21-bit x1	x2	44 x 4	1/3	3uA
TM57M5645	1.5V							42 x 4	1/2, 1/3	2uA

Note: No matter V_{BAT}=3V or V_{BAT}=1.5V, the typical LCD bias voltage is:
1/2 bias: VL1=1.5V, V_{LCD}=3V
1/3 bias: VL1=1.0V, VL2=2.0V, V_{LCD}=3V

FEATURES

1. **Operating Voltage :**

   M5620: V_{BAT}= LVR~3.6V

   M5625:V_{BAT}= LVRC~1.8V

   M5640:V_{BAT}= LVR~3.6V

   M5645:V_{BAT}= LVRC~1.8V

Note: Power on VBAT must exceed the LVR and then set LVROFF=0x37 (disable LVR) to obtain lowest VBAT operating. LVRC (ROM error reset, follow the minimum operating voltage) is always enabled. Refer to the "**LVR v.s. SXT32K Min. Operating Voltage**" curve of Characteristic Graphs Section,

2. **Timepiece Current (CPU Off, LCD On, 32K crystal oscillating) :**

   M5620: 5uA @V_{DD}=3V, V_{BAT}=3V, without power saving

   M5620: 3uA @V_{DD}=1.5V, V_{BAT}=3V, with power saving

   M5625: 2uA(1/2bias) or 4uA(1/3bias) @V_{DD}=1.5V, V_{BAT}=1.5V

   M5640: 5uA @V_{DD}=3V, V_{BAT}=3V, without power saving

   M5640: 3uA @V_{DD}=1.5V, V_{BAT}=3V, with power saving

   M5645: 2uA(1/2bias) or 4uA(1/3bias) @V_{DD}=1.5V, V_{BAT}=1.5V

3. **Program ROM:**

   M5620: 2K x 14 bit MTP (Multi Time Programmable ROM)

   M5625: 2K x 14 bit MTP (Multi Time Programmable ROM)

   M5640: 4K x 14 bit MTP (Multi Time Programmable ROM)

   M5645: 4K x 14 bit MTP (Multi Time Programmable ROM)

4. **RAM:**

   M5620: 176 bytes

   M5625: 176 bytes

   M5640: 336 bytes

   M5645: 336 bytes

5. **STACK: 6 Levels**

6. **I/O ports:**

   - Open-Drain Output
   - CMOS Push-Pull Output
   - Schmitt Trigger Input with pull-up resistor option
   - 8 wakeup pin in PB[7:0]

7. **System Oscillation Sources (Fsys) :**

   - Fast-clock
     - FIRC (Fast Internal RC) : 3.8MHz @V_{DD}=3V; 1.3MHz @V_{DD}=1.5V

- Slow-clock
  - SIRC (Slow Internal RC) : 45KHz @V_{DD}=3V; 32KHz @V_{DD}=1.5V
  - SXT (Slow Crystal) : 32768 Hz
- System Oscillation Sources can be divided by 1/2/4/8 as System Clock (Fsys)
- Dual System Clock Switching between Fast-clock and Slow-clock
  - FIRC + SIRC
  - FIRC + SXT

8. Power Saving Operation Mode

- FAST Mode: CPU running at Fast-clock
- SLOW Mode: CPU running at Slow-clock
- IDLE Mode: Fast-clock and CPU stop; Slow-clock, Timer2 and LCD keep running
- STOP Mode: All clocks stop

9. Resistance to Frequency Converter (RFC)

10. Three Independent Timers

- Timer0 (TM0)
  - 8-bit timer with divided by 1~256 pre-scale option, counter/reload/interrupt/stop/capture function
  - Clock sources: Fsys or Slow-clock /1/4/16/64 (SIRC/SXT)
- Timer1 (TM1)
  - 8-bit timer with divided by 1~256 pre-scale option, reload/interrupt/stop/capture/clear function
  - Clock source: Fsys
- Timer2 (T2)
  - 21-bit timer with 4 interrupt time period options (60s/1s/0.5s/0.125s)
  - Clock sources: Fsys /128 or Slow-clock (SIRC/SXT)
  - IDLE mode wake-up, if clock source is Slow-clock

11. Interrupts

- Three External Interrupt pins (INT0~INT2)
  - Rising or falling edge triggered interrupt
- Timer0/Timer1/Timer2 Interrupts
- PWM0 Interrupt
- RFC overflow Interrupt

12. Wake up

- External Interrupt pins (INT0~INT2) can wake up CPU in IDLE/STOP mode.
- PB [7:0] low-level can wake up CPU in IDLE/STOP mode.
- Timer2 Interrupt can wake up CPU in IDLE mode if Timer2 clock source is Slow-clock.
- PWM0 Interrupt can wake up CPU in IDLE mode if PWM0 clock source is Slow-clock.

13. LCD Controller / Driver

- 1/3 or 1/4 Duty
- 4 steps brightness adjustable for V_{LCD} (only for 1/3 LCD Bias)

  M5620:

  - Max: 4 COM x 28 SEG or 3 COM x 29 SEG
  - 1/3 LCD Bias voltage, typical VL1=1.0V, VL2=2.0V, and V_{LCD}=3.0V

  M5625:

  - Max: 4 COM x 26 SEG or 3 COM x 27 SEG
  - 1/2 LCD Bias voltage, typical VL1=1.5V and V_{LCD}=3.0V
  - 1/3 LCD Bias voltage, typical VL1=1.0V, VL2=2.0V, and V_{LCD}=3.0V

  M5640:

  - Max: 4 COM x 44 SEG or 3 COM x 45 SEG
  - 1/3 LCD Bias voltage, typical VL1=1.0V, VL2=2.0V, and V_{LCD}=3.0V

  M5645:

  - Max: 4 COM x 42 SEG or 3 COM x 43 SEG
  - 1/2 LCD Bias voltage, typical VL1=1.5V and V_{LCD}=3.0V
  - 1/3 LCD Bias voltage, typical VL1=1.0V, VL2=2.0V, and V_{LCD}=3.0V
-

14. Watchdog Timer (WDT)

- Clocked by system clock with 2 adjustable reset times, 2^{16}/Fsys or 2^{15}/Fsys
  - 1.4s/0.7s @V_{DD}=3V (Fsys = SIRC)
  - 2.0s/1.0s @V_{DD}=1.5V (Fsys = SIRC)
- Watchdog timer is disabled in IDLE/STOP mode

15. Two 8-bit PWMs for Buzzer / IR application (PWM0&PWM1)

- Adjustable Period & Clock Pre-scale
- Clock sources: Fast-clock or Slow-clock

16. Four types Reset

- Power On Reset
- Watchdog Reset
- Low Voltage Reset (LVR):

  M5620:1.6V@25℃

  M5625:1.1V@25℃

  M5640:1.6V@25℃,

  M5645:1.1V@25℃
- External Pin Reset

17. Low Battery Detector (LBD) by BandGap Voltage Reference

M5620: Detect V_{BAT} from 2.4V to 3.0V

M5625: Detect V_{BAT} from 1.2V to 1.5V @LCDON=1

M5640: Detect V_{BAT} from 2.4V to 3.0V

M5645: Detect V_{BAT} from 1.2V to 1.5V @LCDON=1

18. Operating Temperature Range :

M5620: -40℃ to + 85℃

M5625: -20℃ to + 85℃

M5640: -40℃ to + 85℃

M5645: -20℃ to + 85℃

19. Package Type :

M5620: Dice-form / SSOP48

M5625: Dice-form / SSOP48

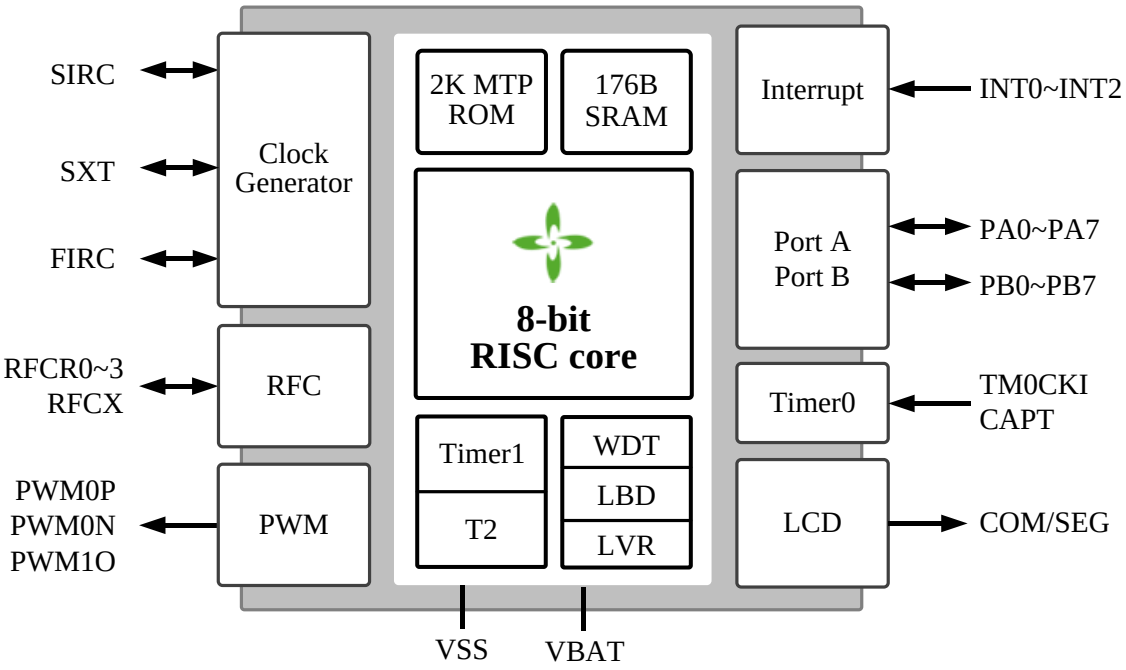
M5640: Dice-form / LQFP48 / LQFP64

M5645: Dice-form / LQFP48 / LQFP64

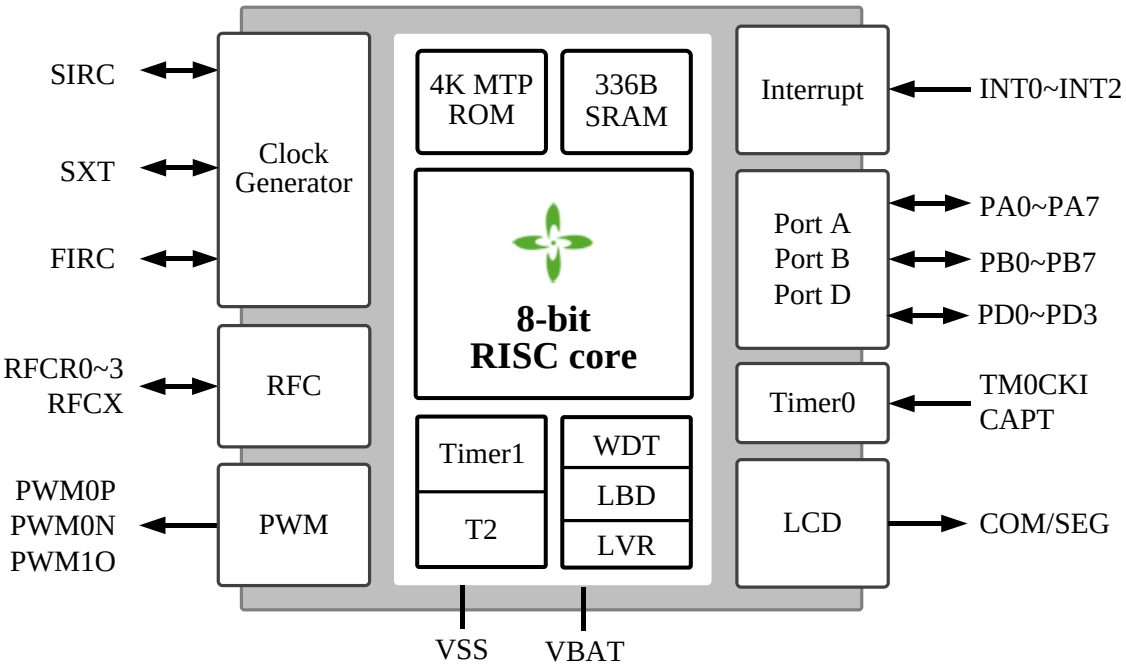
20. Supported EV board on ICE

EV board: EV8228

BLOCK DIAGRAM



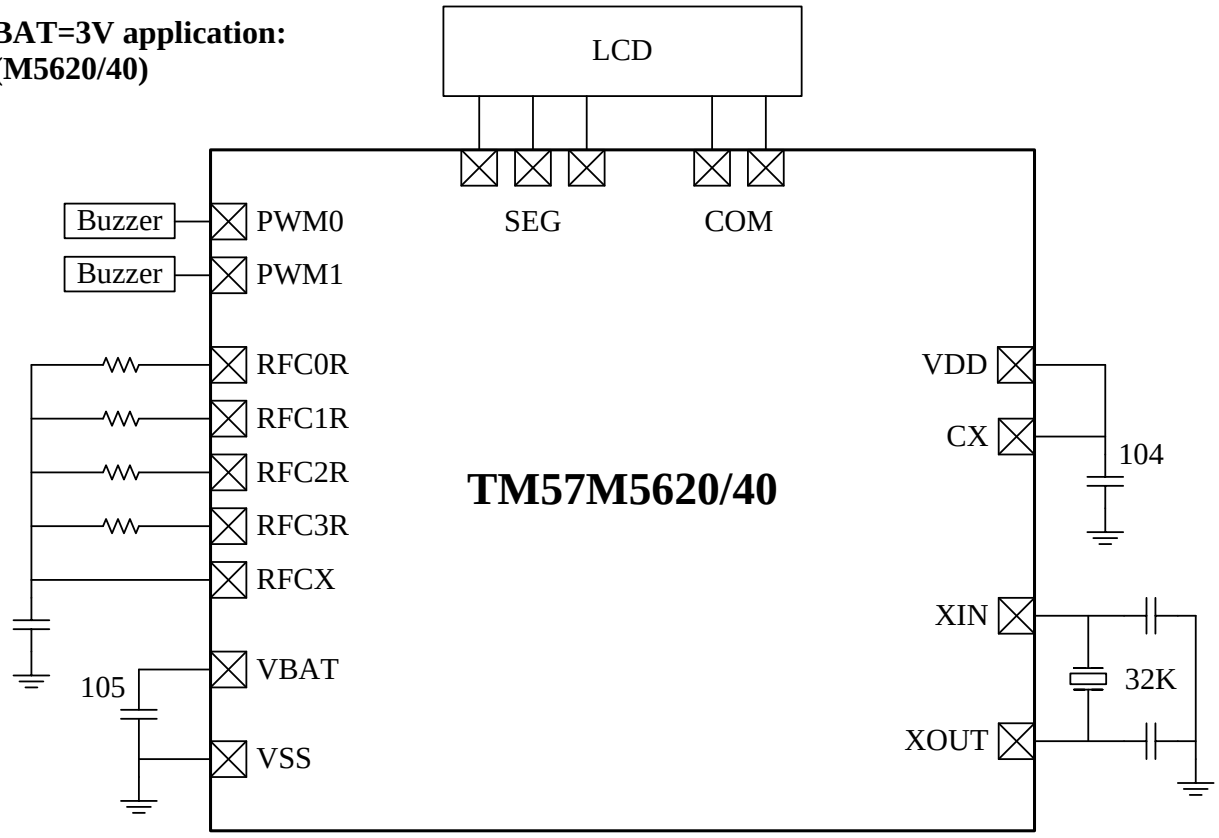
TM57M5620/25 Block Diagram



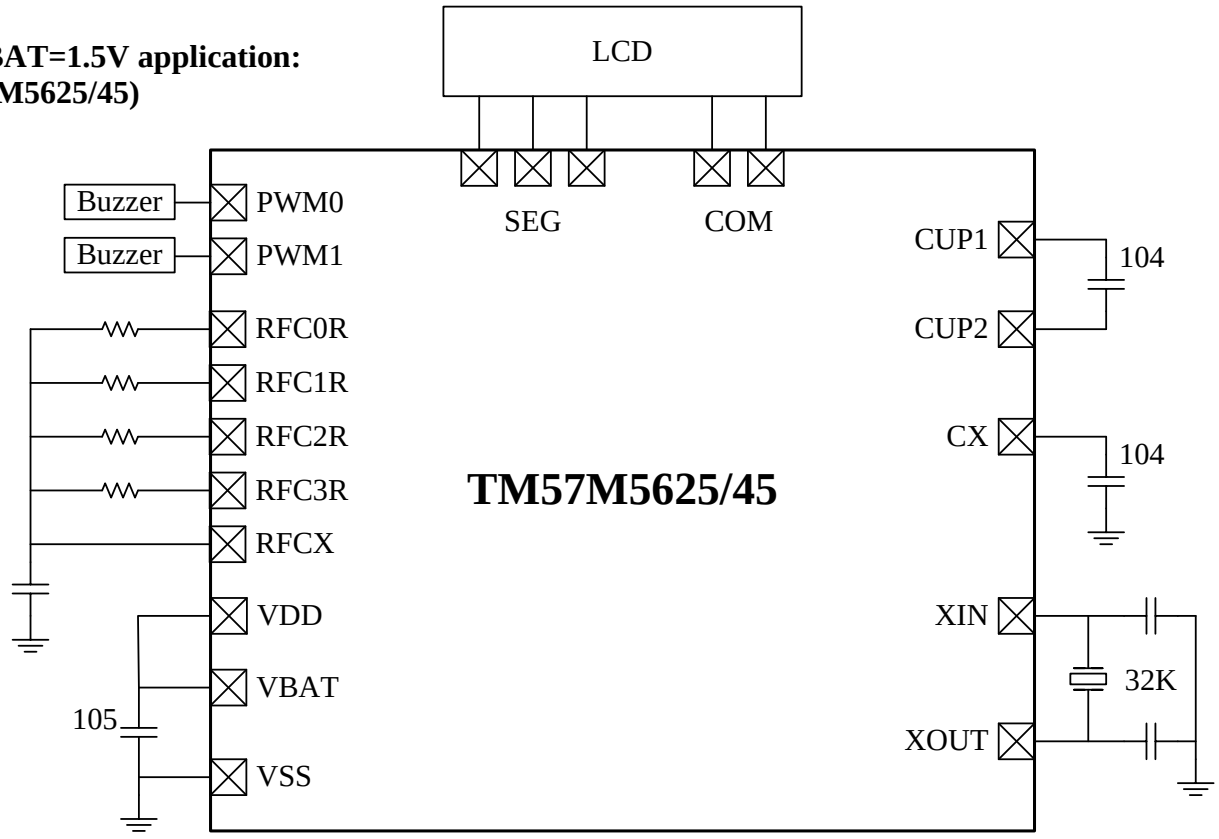
TM57M5640/45 Block Diagram

APPLICATION CIRCUIT

VBAT=3V application:
(M5620/40)

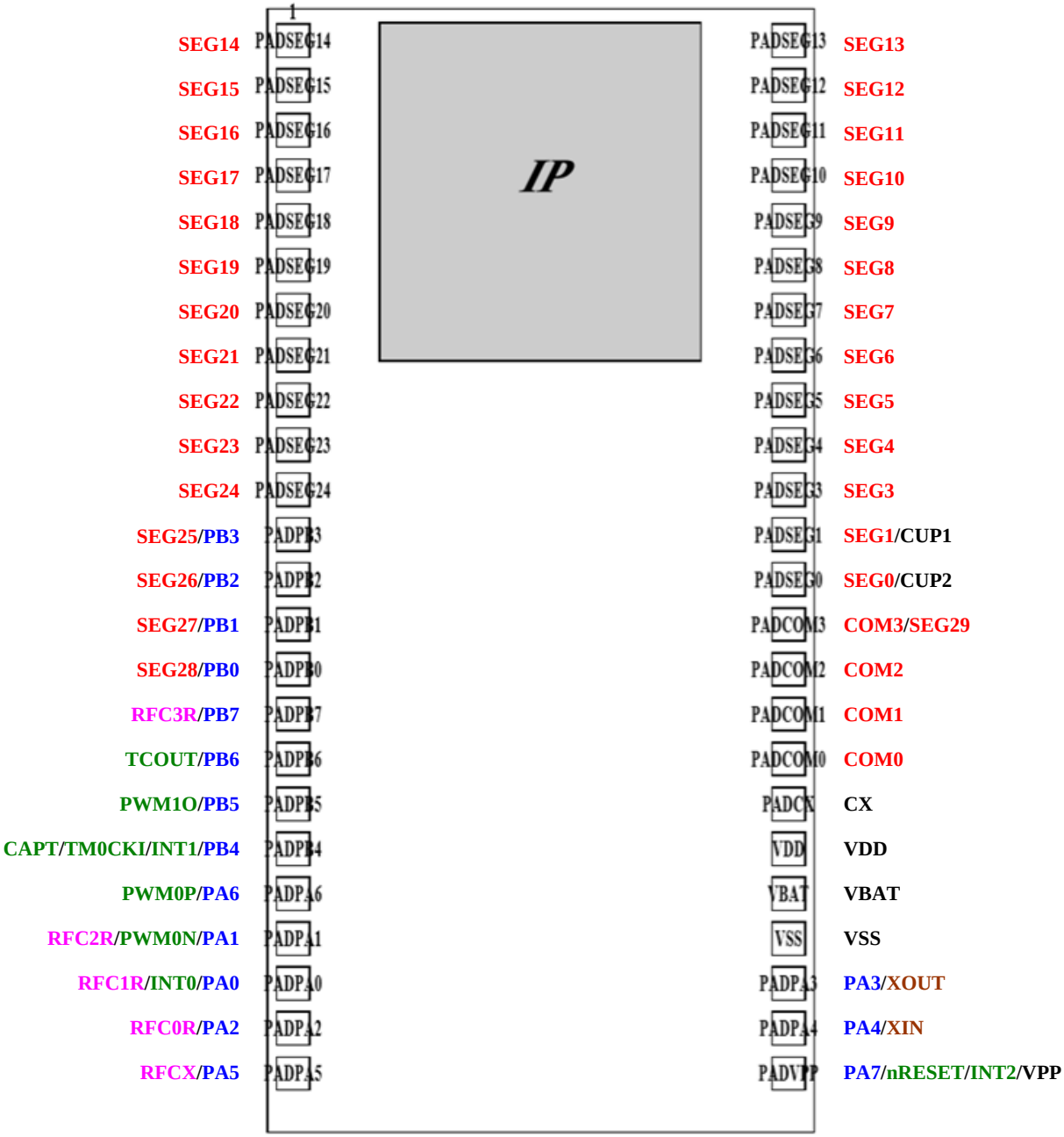


VBAT=1.5V application:
(M5625/45)

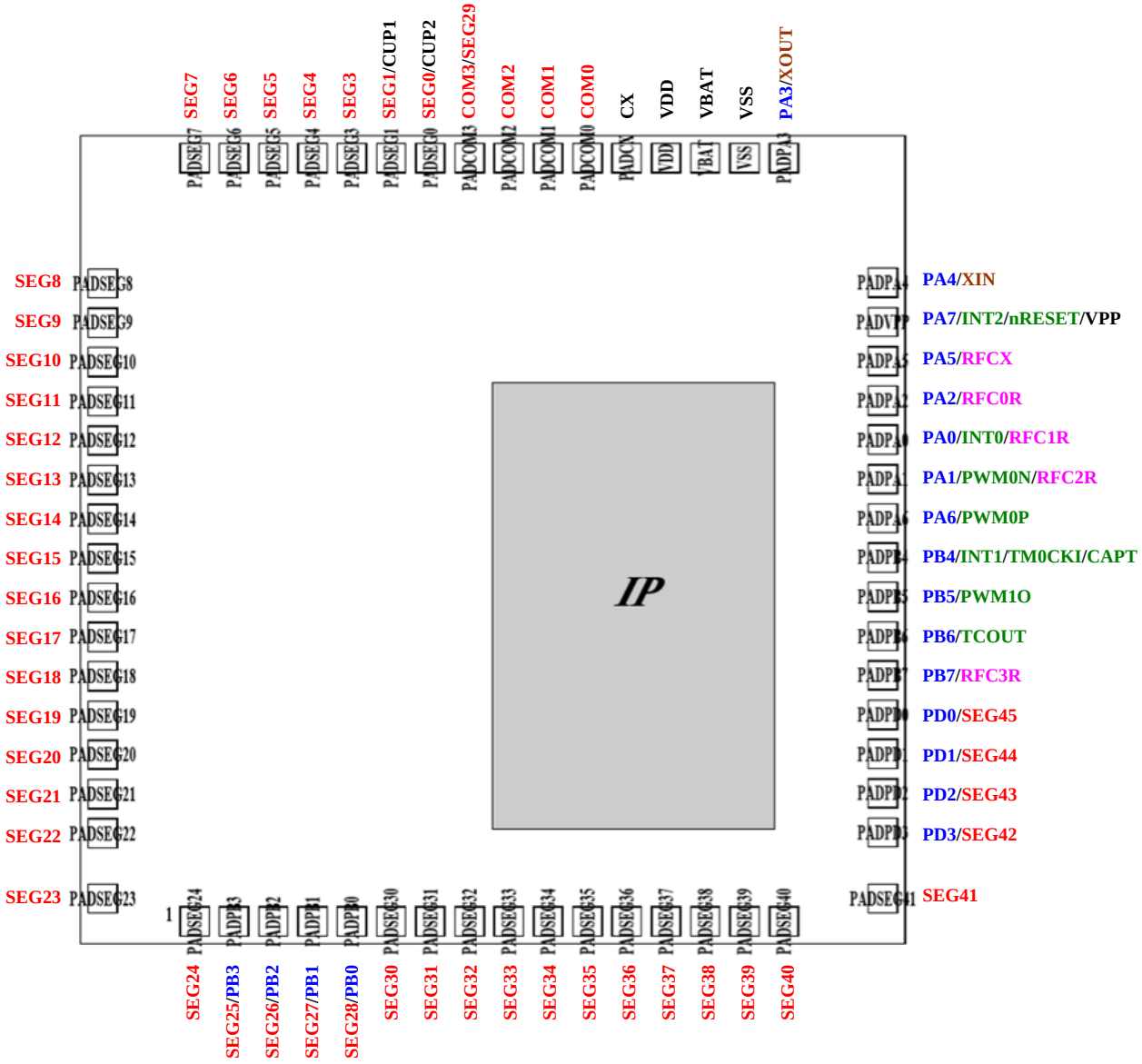


DIE PAD LIST

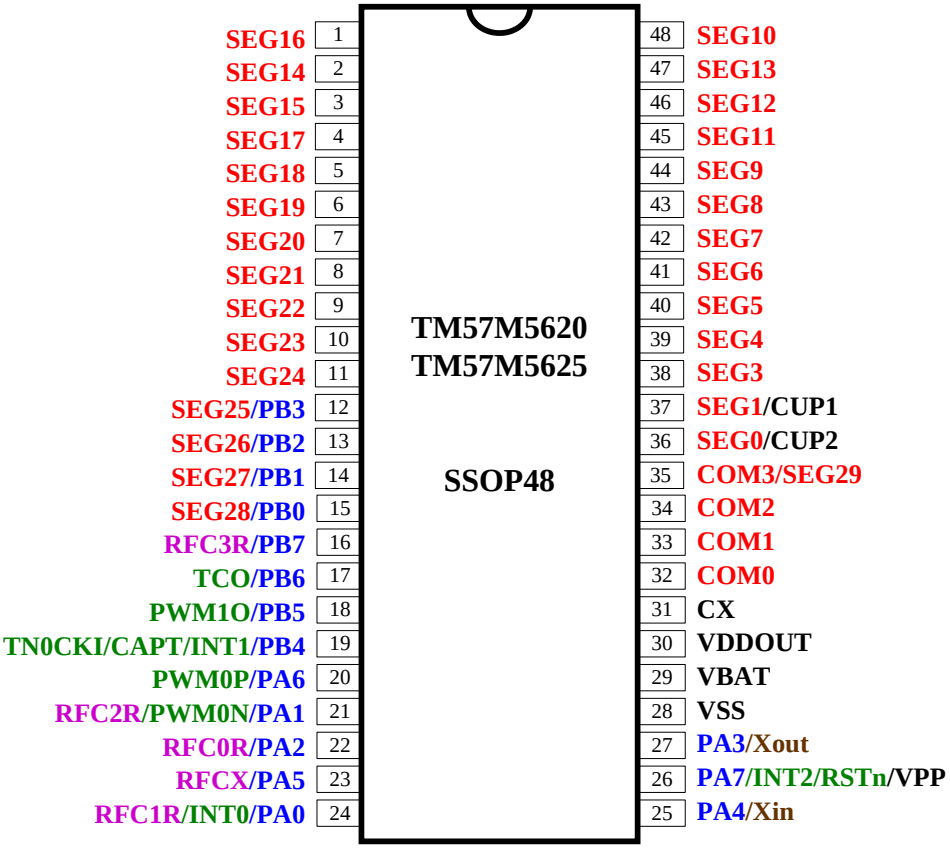
TM57M5620/TM57M5625:

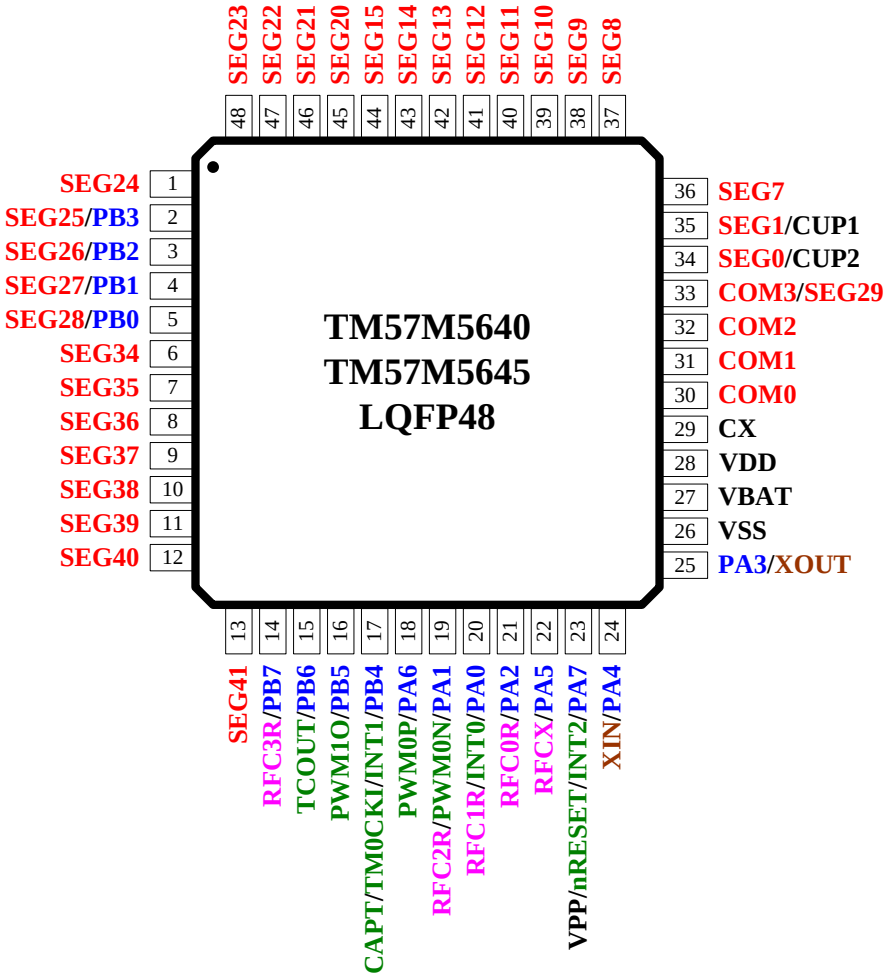


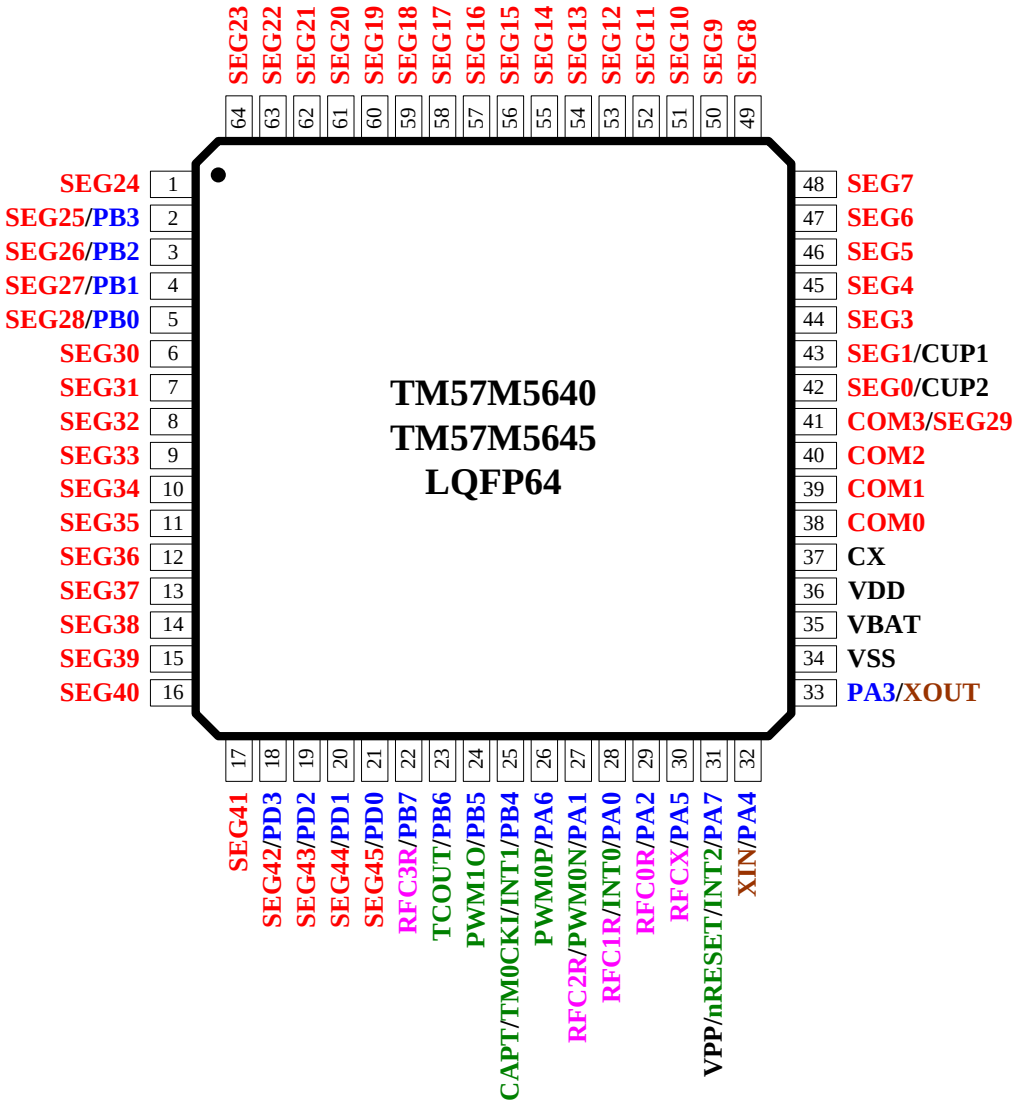
TM57M5640/TM57M5645:



PIN ASSIGNMENT




TM57M5640
TM57M5645
LQFP48
1 SEG24
2 SEG25/PB3
3 SEG26/PB2
4 SEG27/PB1
5 SEG28/PB0
6 SEG34
7 SEG35
8 SEG36
9 SEG37
10 SEG38
11 SEG39
12 SEG40
13 SEG41
14 RFC3R/PB7
15 TCOUT/PB6
16 PWM1O/PB5
17 CAPT/TM0CKI/INT1/PB4
18 PWM0P/PA6
19 RFC2R/PWM0N/PA1
20 RFC1R/INT0/PA0
21 RFC0R/PA2
22 RFCX/PA5
23 VPP/nRESET/INT2/PA7
24 XIN/PA4
25 PA3/XOUT
26 VSS
27 VBAT
28 VDD
29 CX
30 COM0
31 COM1
32 COM2
33 COM3/SEG29
34 SEG0/CUP2
35 SEG1/CUP1
36 SEG7
37 SEG8
38 SEG9
39 SEG10
40 SEG11
41 SEG12
42 SEG13
43 SEG14
44 SEG15
45 SEG20
46 SEG21
47 SEG22
48 SEG23


SEG23 64
SEG22 63
SEG21 62
SEG20 61
SEG19 60
SEG18 59
SEG17 58
SEG16 57
SEG15 56
SEG14 55
SEG13 54
SEG12 53
SEG11 52
SEG10 51
SEG9 50
SEG8 49
SEG24 1
SEG25/PB3 2
SEG26/PB2 3
SEG27/PB1 4
SEG28/PB0 5
SEG30 6
SEG31 7
SEG32 8
SEG33 9
SEG34 10
SEG35 11
SEG36 12
SEG37 13
SEG38 14
SEG39 15
SEG40 16
TM57M5640
TM57M5645
LQFP64
48 SEG7
47 SEG6
46 SEG5
45 SEG4
44 SEG3
43 SEG1/CUP1
42 SEG0/CUP2
41 COM3/SEG29
40 COM2
39 COM1
38 COM0
37 CX
36 VDD
35 VBAT
34 VSS
33 PA3/XOUT
17 SEG41
18 SEG42/PD3
19 SEG43/PD2
20 SEG44/PD1
21 SEG45/PD0
22 RFC3R/PB7
23 TCOUT/PB6
24 PWM1O/PB5
25 CAPT/TM0CKI/INT1/PB4
26 PWM0P/PA6
27 RFC2R/PWM0N/PA1
28 RFC1R/INT0/PA0
29 RFC0R/PA2
30 RFCX/PA5
31 VPP/nRESET/INT2/PA7
32 XIN/PA4

PIN DESCRIPTIONS

Name	In/Out	Pin Description
PA0–PA6	I/O	Bit-programmable I/O port for Schmitt-trigger input, “CMOS push-pull” output or “Open-Drain” output. Pull-up Resistors are assignable by software.
PA7	I/O	Bit-programmable I/O port for Schmitt-trigger input, or “Open-Drain” output. Pull-up resistors are assignable by software.
PB0–PB3	I/O	Bit-programmable I/O port for Schmitt-trigger input without pull-up, “CMOS push-pull”output
PB4–PB7	I/O	Bit-programmable I/O port for Schmitt-trigger input, “CMOS push-pull” output or “Open-Drain” output. Pull-up Resistors are assignable by software.
PD0–PD3	I/O	Bit-programmable I/O port for Schmitt-trigger input without pull-up, “CMOS push-pull”output
nRESET	I	External active low reset with internal pull-high
INT0–INT2	I	External interrupt input
TCOUT	O	Instruction cycle clock output. The instruction clock frequency is system clock frequency divided by two (Fsys/2)
TM0CKI	I	Timer0’s input in counter mode
CAPT	I	Timer0/Timer1 Capture input
RFC0R~RFC3R	O	RFC resistor connection pin
RFCX	I	RFC clock input pin
COM0~COM3	O	LCD common output
SEG0~SEG1, SEG3~SEG45	O	LCD segment output
PWM0P, PWM0N	O	8-bit PWM0 output
PWM1O	O	8-bit PWM1 output
CX, CUP1, CUP2	–	LCD bias capacitor connection pin
XIN, XOUT	–	Crystal / Resonator oscillator connection for system clock.
VDD	P	Internal voltage pin
VPP	I	MTP programming high voltage input
VBAT, VSS	P	Power Voltage input pin and ground

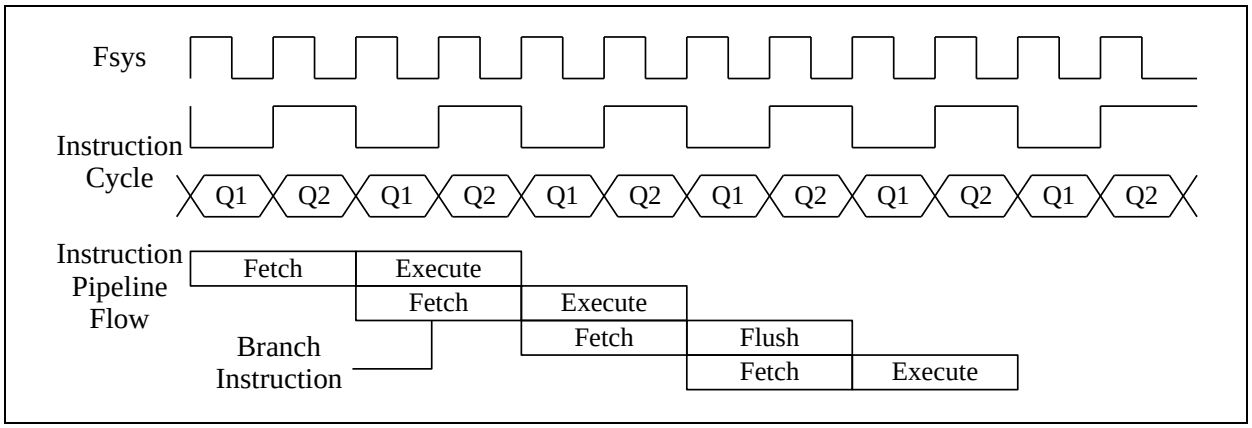
Note: Programming pins are list below. It is better to remove the PCB components connected to these pins during In-Circuit-Programming.
7 wire mode: VBAT/VSS/PA0/PA1/PA2/PA3/PA7 (VPP)
5 wire mode: VBAT/VSS/PA0/PA1/PA7 (VPP)

FUNCTIONAL DESCRIPTION

1. CPU Core

1.1 Clock Scheme and Instruction Cycle

The system clock is internally divided by two to generate Q1 state and Q2 state for each instruction cycle. The Programming Counter (PC) is updated at Q1 and the instruction is fetched from program ROM and latched into the instruction register in Q2. It is then decoded and executed during the following Q1-Q2 cycle. Branch instructions take two cycles since the fetch instruction is 'flushed' from the pipeline, while the new instruction is being fetched and then executed.



1.2 ALU and Working (W) Register

The ALU is 8-bit wide and capable of addition, subtraction, shift and logical operations. In two-operand instructions, typically one operand is the W register, which is an 8-bit non-addressable register used for ALU operations. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either W register or a file register. Depending on the instruction executed, the ALU may affect the values of Carry (C), Digit Carry (DC), and Zero (Z) Flags in the STATUS register. The C and DC flags operate as a /Borrow and /Digit Borrow, respectively, in subtraction.

Note: /Borrow represents inverted of Borrow register.

/Digit Borrow represents inverted of Digit Borrow register.

1.3 Programming Counter (PC) and Stack

The Programming Counter is 12-bit wide capable of addressing a 2K x 14 (M5620/M5625) or 4K x 14 (M5640/ M5645) MTP ROM. As a program instruction is executed, the PC will contain the address of the next program instruction to be executed. The PC value is normally increased by one except the followings. The Reset Vector (000h) and the Interrupt Vector (001h) are provided for PC initialization and Interrupt. For CALL / GOTO instructions, PC loads 12 bits address from instruction word. For RET / RETI / RETLW instructions, PC retrieves its content from the top level STACK. For the other instructions updating PC [7:0], the PC [11:8] keeps unchanged. Therefore, the data of a lookup table must be located with the same PC [11:8].

The STACK is 12-bit wide and 6-level in depth. The CALL instruction and hardware interrupt will push STACK level in order. While the RET / RETI / RETLW instructions pop the STACK level in order.

For table lookup, the device offers the powerful table read instructions TABRL, TABRH to return the 14-bit ROM data into W register by setting the DPTR = {DPH, DPL} registers in F-Plane.

◇Example: To look up the MTP data located "TABLE"

```
            ORG     000H        ; Reset Vector
            GOTO    START       ; Goto user program address
START:
            MOVLW   00H
            MOVWF   INDEX       ; Set lookup table's address (INDEX)
LOOP:
            MOVFW   INDEX       ; Move INDEX value to W register
            CALL    TABLE       ; To Lookup data (W = 55H when INDEX = 00H)
            …
            INCF    INDEX, 1    ; Increment the INDEX for next address
            …
            GOTO    LOOP        ; Goto LOOP label

            ORG     X00H        ; X = 1, 2, 3, …, E, F
TABLE:
            ADDWF   PCL, 1      ; (Addr = X00H) Add the W with PCL, the result
                                ; back in PCL
            RETLW   55H         ; W = 55H when return
            RETLW   56H         ; W = 56H when return
            RETLW   58H         ; W = 58H when return
```

Note: The chip defines 256 ROM addresses as one page, so that ROM has sixteen pages, 000H~0FFH, 100H~1FFH, 200H~2FFH, …, and F00H~FFFH. On the other words, PC[11:8] can be defined as page. A lookup table must be located at the same page to avoid getting wrong data. Thus, the lookup table has maximum 255 data for above example with starting a lookup table at X00H (X = 1, 2, 3, …, E, F). If a lookup table has fewer data, it needs not setting the starting address at X00H, but only confirms all lookup table data are located at the same page.

◇Example: To look up the MTP data located “TABLE” by TABRL and TABRH instructions

```
        ORG     000H            ; Reset Vector
        GOTO    START           ; Goto user program address
START:
        MOVLW   (TABLE >>8) & 0xff  ; Get high byte address of TABLE label
        MOVWF   DPH             ; DPH (F1E.3~0) = 02H
        MOVLW   (TABLE) & 0xff  ; Get low byte address of TABLE label
        MOVWF   DPL             ; DPL (F1D.7~0) = 80H
LOOP:
        TABRL                   ; W = 86H when DTPR = {DPH, DPL} = 0280H
        TABRH                   ; W = 19H when DTPR = {DPH, DPL} = 0280H
        …
        INCF    DPL, 1          ; Increment the DPL for next address
        …
        GOTO    LOOP            ; Goto LOOP label

        ORG     280H
TABLE:
        DT      0x1986          ; 14-bit ROM data
        DT      0x3719          ; 14-bit ROM data
```

F02	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCL	PCL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F02.7~0 **PCL:** Low-byte of Program Counter (PC[7:0])

F0A	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCH	–	–	–	–	PCH			
R/W	–	–	–	–	R	R	R	R
Reset	–	–	–	–	0	0	0	0

F0A.3~0 **PCH:** 4 MSBs of Program Counter (PC[11:8])

F1D	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F1D.7~0 **DPL:** Table read low address, data ROM pointer (DPTR[7:0])

F1E	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	–	–	–	–	DPH			
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

F1E.3~0 **DPH:** 4 MSBs of Table read high address, data ROM pointer (DPTR[11:8])

1.4 STATUS Register (F-Plane 03H)

This register contains the arithmetic status of ALU and the reset status. The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the STATUS register because these instructions do not affect those bits.

F03	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	GB2	GB1	RAMBK	TO	PD	Z	DC	C
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W

Bit	Description	
7	**GB2**: General Purpose Bit 2	
6	**GB1**: General Purpose Bit 1	
5	**RAMBK:** RAM Bank Selection 0: FRAM Bank0 1: FRAM Bank1	
4	**TO**: Time Out Flag 0: after Power On Reset, LVR Reset, or CLRWDT/SLEEP instruction 1: WDT time out occurs	
3	**PD**: Power Down Flag 0: after Power On Reset, LVR Reset, or CLRWDT instruction 1: after SLEEP instruction	
2	**Z**: Zero Flag 0: the result of a logic operation is not zero 1: the result of a logic operation is zero	
1	**DC**: Decimal Carry Flag or Decimal/Borrow Flag	
	ADD instruction	SUB instruction
	0: no carry 1: a carry from the low nibble bits of the result occurs	0: a borrow from the low nibble bits of the result occurs 1: no borrow
0	**C**: Carry Flag or/Borrow Flag	
	ADD instruction	SUB instruction
	0: no carry 1: a carry occurs from the MSB	0: a borrow occurs from the MSB 1: no borrow

◇Example: Write immediate data into STATUS register

```
MOVLW   00H
MOVWF   STATUS          ; Clear STATUS register
```

◇Example: Bit addressing set and clear STATUS register

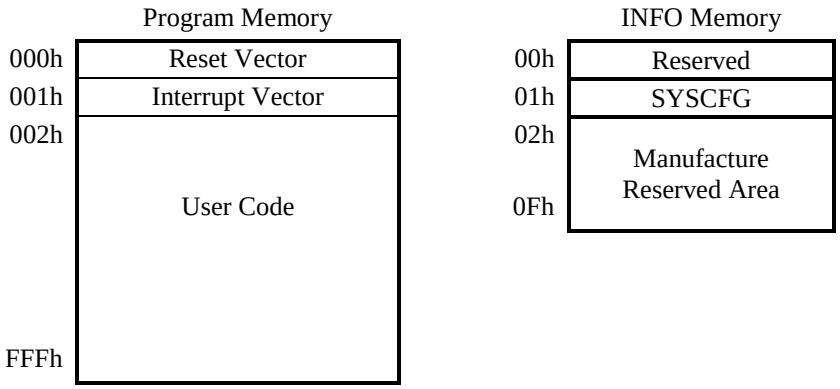
```
BSF     STATUS, 0       ; Set C = 1
BCF     STATUS, 0       ; Clear C = 0
```

◇Example: Determine the C flag by BTFSS instruction

```
BTFSS   STATUS, 0       ; Check the C flag
GOTO    LABEL_1         ; If C = 0, goto LABEL_1 label
GOTO    LABEL_2         ; If C = 1, goto LABEL_2 label
```

2. Program ROM (MTP)

Take 4K ROM as an example, The MTP Program ROM of this device is 4K words, with an extra INFO area to store the SYSCFG and manufacture data. The MTP ROM can be written multi-times and can be read as long as the PROTECT bit of SYSCFG is not set. The SYSCFG can be read no matter PROTECT is set or cleared, but can be written only when PROTECT is cleared or MTP ROM is blank. That is, unprotect the PROTECT bit can be done only if the Program ROM area is blank. The tenx certified writer can do the above actions with the sophisticated software.



The System Configuration Register (SYSCFG) is located at MTP INFO area. The SYSCFG determines the option for initial condition of MCU. It is written by MTP Writer only. User can select chip operation mode by SYSCFG register.

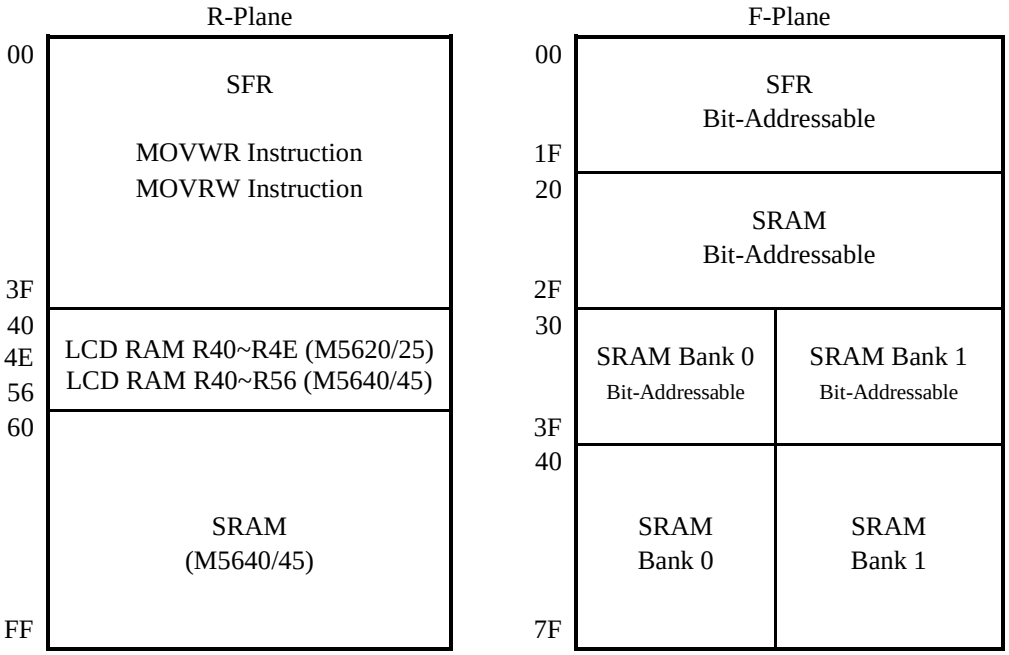
Bit	Description	
13	**PROTECT**: Code protection selection	
	1	Enable
	0	Disable
12	**XRSTE**: External Pin (PA7) Reset Enable	
	1	Enable
	0	Disable (PA7 as input I/O pin)
11	**LVR**: Low Voltage Reset	
	1	LVR 1.1V and Disable in IDLE/STOP Mode (for M5625/45)
	0	LVR 1.6V and Disable in IDLE/STOP Mode (for M5620/40)
9	**WDTE**: WDT Reset Enable	
	1	Enable in FAST/SLOW Mode and Disable in IDLE/STOP Mode
	0	Disable
8~0	Tenx Reserved	

3. Data Memory (RAM and SFR)

There are two Data Memory Planes in the chip, F-Plane and R-Plane.

The lower locations of F-Plane are reserved for Special-Function-Register (SFR). Above the SFR is General Purpose Data Memory, implemented as static RAM. F-Plane can be addressed directly or indirectly. Indirect Addressing is made by INDF register. The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a pointer). The first half of F-Plane is bit-addressable, while the second half of F-Plane is not bit-addressable.

R-Plane can also be addressed directly or indirectly. Indirect Addressing is made by INDR register. The INDR register is not a physical register. Addressing INDR actually addresses the register whose address is contained in the RSR register (RSR is a pointer). The R-Plane is not bit-addressable and only supports the MOVWR, MOVRW byte operating instructions.



F-Plane	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
00h	INDF	TM0	PCL	STATUS	FSR	PAD	PBD	PDD
08h	INTIE	INTIF	PCH	CLKCTL	MF0C	PWM0D	LBDCTL	RFCTL
10h	LCDCTL	RFCNTH	RFCNTL	PWM1D	TM1	PWMCLR		
18h					RSR	DPL	DPH	

R-Plane	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
00h	INDR	TM0RLD	TM0CTL	PWRDN	WDTCLR	PAMODH	PAMODL	PBMODH
08h	PBMODL	PDMODL	PWM0CTL	PWM0PRD	PWM1CTL	PWM1PRD		
10h	TM1RLD	TM1CTL	PBWKEN					
18h								LVROFF
40h	LCDRAM							
48h	LCDRAM							
50h	LCDRAM							

◇ Example: Write immediate data into R-Plane register

```
        MOVLW   AAH             ; Move immediate AAH into W register
        MOVWR   05H             ; Move W value into R-Plane location 05H
```

◇ Example: Move R-Plane location 20H data into W register

```
        MOVRW   20H             ; To get a content of R-Plane location 20H to W
```

◇ Example: Clear R-Plane by indirectly addressing mode

```
        MOVLW   20H             ; W = 20H
        MOVWF   RSR             ; Set R-Plane address to RSR register
LOOP:
        MOVLW   00H
        MOVWR   INDR            ; Clear R-Plane 20H
```

◇ Example: Clear F-Plane RAM data by indirectly addressing mode

```
        MOVLW   20H             ; W = 20H (SRAM start address)
        MOVWF   FSR             ; Set start address of user SRAM into FSR register
LOOP:
        MOVLW   00H
        MOVWF   INDF            ; Clear user SRAM data
        INCF    FSR, 1          ; Increment the FSR for next address
        MOVLW   80H             ; W = 80H (SRAM end address)
        XORWF   FSR, 0          ; Check the FSR is end address of user SRAM?
        BTFSS   STATUS, Z       ; Check the Z flag
        GOTO    LOOP            ; If Z = 0, goto LOOP label
        …                       ; If Z = 1, exit LOOP
```

F00	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INDF	INDF							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	–	–	–	–	–

F00.7~0 **INDF:** Not a physical register, addressing INDF actually point to the F-Plane register whose address is contained in the FSR register

F04	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSR	GB3	FSR						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F04.7 **GB3:** General purpose bit 3

F04.6~0 **FSR:** F-Plane file select register, indirect address mode pointer

F1C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR	RSR							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

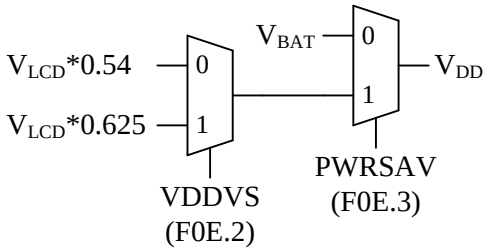
F1C.7~0 **RSR:** R-Plane file select register, indirect address mode pointer

R00	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INDR	INDR							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	–	–	–	–	–

R00.7~0 **INDR:** Not a physical register, addressing INDR actually point to the R-Plane register whose address is contained in the RSR register

4. Power Management (only for M5620/40)

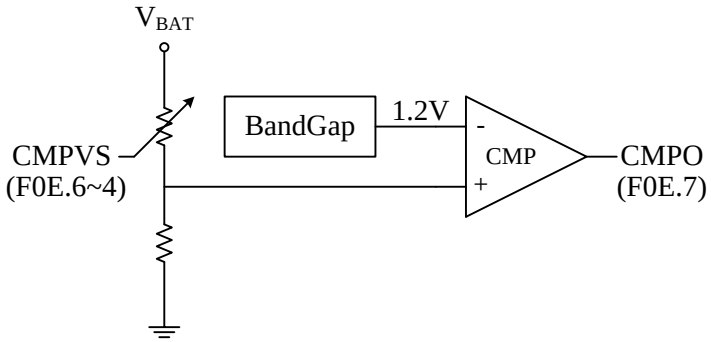
V_{BAT} is the power supply for this chip. The typical condition is V_{BAT}=3V. V_{DD} is the internal voltage level for chip operation. Only M5620/M5640 can use PWRSAV (F0E.3) function to reduce VDD for power-saving. When PWRSAV enable, VDD is related to V_{LCD}, more information about V_{LCD} can see the chapter of LCD Driver.



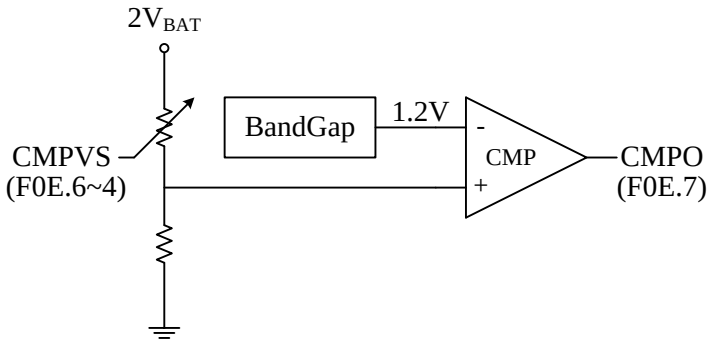
Power-save function

The internal 1.2V BandGap module provides accuracy voltage reference for the Low Battery Detector (LBD). V_{BAT} (M5620/40) or $2V_{BAT}$ (M5625/45) is divided by resistors to a certain level then compare to the BandGap voltage, M5625/45 must keep LCDON=1 during using LBD function. The BandGap and Comparator consume un-neglect current, so user should not use them too often. Because V_{BAT} voltage level changes very slowly, user can detect it once an hour or once a day to reduce current consumption. See the picture below.

M5620/40:



M5625/45: (LCDON=1)



F0E	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LBDCTL	CMPO	CMPVS			PWRSAV	VDDVS	PUMPCKS	LVRPDF
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset	–	0	0	0	0	0	0	–

F0E.7 **CMPO:** Low Battery Detector (LBD) result. CMP=0 means VBAT value is lower than the boundary selected by CMPVS.

Note: M5625/45 must turn on LCD for this function.

F0E.6~4 **CMPVS:** Select V_{BAT}/V_{LCD} resistor divider for Comparator input to compare with the 1.2V Bandgap reference voltage.

M5620/40:

000: Comparator and Bandgap Disable
001: detect if V_{BAT}>2.4V
010: detect if V_{BAT}>2.5V;
011: detect if V_{BAT}>2.6V;
100: detect if V_{BAT}>2.7V;
101: detect if V_{BAT}>2.8V;
110: detect if V_{BAT}>2.9V;
111: detect if V_{BAT}>3.0V;

M5625/45:

000: Comparator and Bandgap Disable
001: detect if V_{BAT}>1.20V
010:; detect if V_{BAT}>1.25V
011: detect if V_{BAT}>1.30V
100: detect if V_{BAT}>1.35V
101: detect if V_{BAT}>1.40V
110: detect if V_{BAT}>1.45V
111: detect if V_{BAT}>1.50V

F0E.3 **PWRSAV:** Power saving control for M5620/40. ***Note:*** M5625/45 must keep PWRSAV=0
0: Disable, $V_{DD}=V_{BAT}$
1: Enable, $V_{DD}=V_{LCD}$*0.54 or V_{LCD}*0.625

F0E.2 **VDDVS:** V_{DD} voltage selection. It actives while PWRSAV=1.
0: $V_{DD}=V_{LCD}$*0.54
1: $V_{DD}=V_{LCD}$*0.625

5. Reset

This device can be reset in four ways. The TO and PD flags at status register (STATUS) can indicate system reset status. The SYSCFG controls the Reset functionality.

- Power-On-Reset (POR)
- Low Voltage Reset (LVR)
  M5620/40: 1.6V;
  M5625/45: 1.1V
  Default enable, can be disable by FW setting
- External Pin Reset (PA7)
- Watchdog Reset (WDT)
  Clocked by system clock
  1.4 second or 0.7 second @V_{DD}=3V
  2.0 second or 1.0 second @V_{DD}=1.5V (Fsys = SIRC)
  Run in FAST/SLOW mode; Stop in IDLE/STOP mode.

F03	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	GB2	GB1	RAMBK	TO	PD	Z	DC	C
R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W
Reset	0	0	0	–	–	0	0	0

F03.4 **TO:** WDT Time Out Flag
0: after Power On Reset, LVR Reset, or CLRWDT / SLEEP instructions
1: WDT time out occurs

F03.3 **PD:** Power Down Flag
0: after Power On Reset, LVR Reset, or CLRWDT instruction
1: after SLEEP instruction

R04	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTCLR	WDTCLR							
R/W	W							
Reset	–	–	–	–	–	–	–	–

R04.7~0 **WDTCLR:** Write this register to clear WDT (=CLRWDT instruction)

R0A	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0CTL	PWM0CKS	T2PSC		PWM0PSC			PWM0NOE	WDTPSC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

R0A.0 **WDTPSC:** WDT Prescaler, 0: fsys/65536 1:fsys/32768

R1F	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVROFF	LVROFF							
R/W	W							R/W
Reset	–	–	–	–	–	–	–	0

R1F.7~0 **LVROFF (W):** Write this register with 0x37 to force LVR disable
R1F.0 **LVROFF (R):** Flag indicates LVR is forced to disable or not
1: LVR is forced to disable

6. Clock Circuitry and Operation Mode

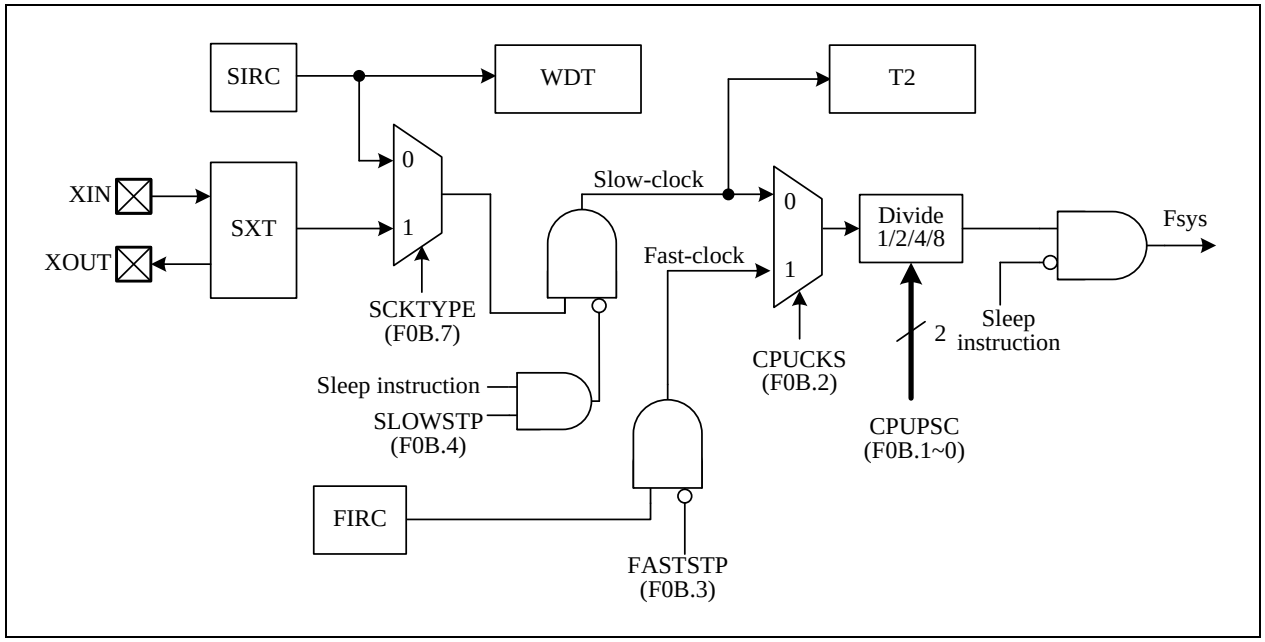
It is required to disable SIRC (Internal Slow RC). It is recommended to execute the following procedures immediately after power-on:

```
    bcf    faststp    //enable fast clock
    bsf    cpucks     //select fast clock
    call   INITIAL    //initial, clear ram …
    bsf    scktype    //slow clock = sxt
    call   WAIT       //wait sxt freq stable,
                      //0.5~1.5 sec, depend on Crystal's vendor
    bcf    cpucks     //select slow clock
```

There are three kinds of system clock source.

- **SIRC** (Slow Internal RC, 45KHz @V_{DD}=3V, 32KHz @V_{DD}=1.5V)
- **SXT** (Slow Crystal, 32768Hz)
- **FIRC** (Fast Internal RC, 3.8MHz @V_{DD}=3V, 1.3MHz @V_{DD}=1.5V)

The device is designed with dual-clock system. During runtime, user can directly switch the System clock between Fast-clock (FIRC) and Slow-clock (SIRC or SXT). It also can directly select a clock divider of 1, 2, 4, or 8. The CLKCTL (F0B) SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow-clock type in Fast mode. Never to write both FASTSTP=1 & CPUCKS=1. It is recommended to write this SFR bit by bit.



Clock Scheme Block Diagram

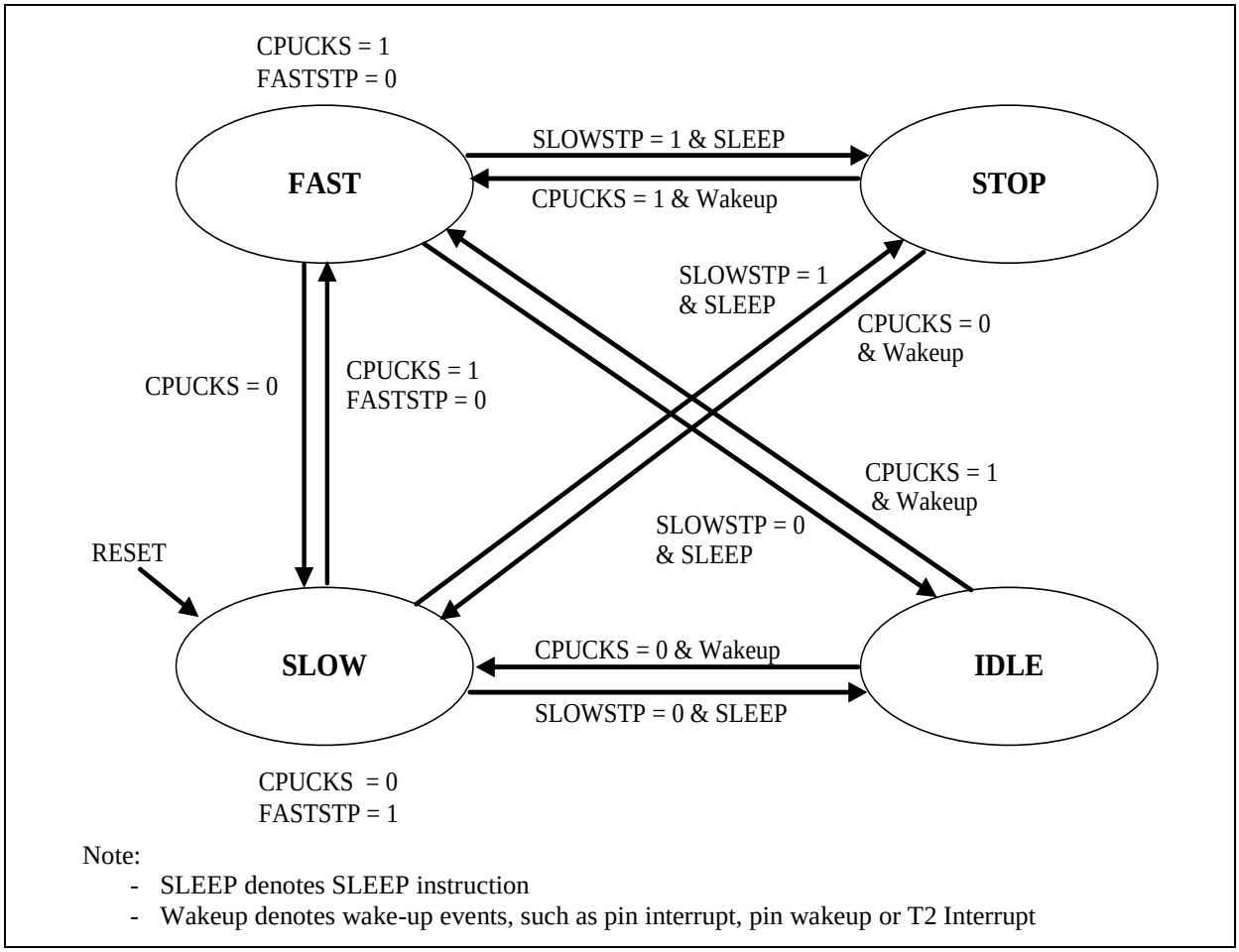
There are four operation modes for this device.

SLOW Mode: After power-on or reset, device enters SLOW mode. In this mode, the Fast-clock should be stopped (by FASTSTP=1, for power saving) and Slow-clock is enabled. The default Slow-clock is SIRC.

FAST Mode: In this mode, the program is executed using Fast-clock as CPU clock.

IDLE Mode: If Slow-clock is enabled (SLOWSTP=0) and T2CKS=0 before executing the SLEEP instruction, the CPU enters the IDLE mode. In this mode, the Slow-clock source keeps T2 block running. CPU stop fetching code and all blocks are stop except T2 related circuits. Idle mode is terminated by Reset or enabled Interrupts wake up.

STOP Mode: If Slow-clock is disabled (SLOWSTP=1) and LCD driver is closed (LCDON=0) before executing the SLEEP instruction, every block is turned off and the device enters the STOP mode after executing the SLEEP instruction. Stop Mode can be terminated by Reset or pin wake up.



CPU Operation Block Diagram

◇Example: Switch operating mode from SLOW mode to FAST mode

```
BCF     FASTSTP     ; Enable Fast-clock
BSF     CPUCKS      ; Switch system clock source to Fast-clock
```

◇Example: Switch operating mode from FAST mode to SLOW mode

```
BCF     SLOWSTP     ; Enable Slow-clock
BCF     CPUCKS      ; Switch system clock source to Slow-clock
BSF     FASTSTP     ; Stop Fast-clock
```

◇Example: Switch operating mode to IDLE mode

```
BCF     SLOWSTP     ; Enable Slow-clock
SLEEP               ; Enter IDLE mode
```

◇Example: Switch operating mode to STOP mode

```
BSF     SLOWSTP     ; Stop Slow-clock
SLEEP               ; Enter STOP mode
```

F0B	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCTL	SCKTYPE	SXTGAIN		SLOWSTP	FASTSTP	CPUCKS	CPUPSC	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	1	1	0	1	0	1	1

F0B.7 **SCKTYPE:** Slow-clock type, this bit can be changed only in Fast mode (CPUCKS =1).
0: SIRC
1: SXT, also set PA3 and PA4 as crystal oscillator pins.
Note: In SXT mode, user should set the PA3 and PA4 pins as Input with Pull-up (Mode 0).

F0B.6~5 **SXTGAIN:** 32768 SXT oscillator gain, 3=Highest gain, 0=Lowest gain. Higher gain can shorten the Crystal oscillation warm-up time. Lower gain can reduce oscillation current.

F0B.4 **SLOWSTP:** Slow-clock Stop control
0: Slow-clock run
1: Slow-clock stop

F0B.3 **FASTSTP:** Fast-clock Stop control, This bit can be changed only when CPUCKS=0
0: Fast-clock run
1: Fast-clock stop

F0B.2 **CPUCKS:** System clock (Fsys) selection, This bit can be changed only when FASTSTP=0
0: Slow-clock
1: Fast-clock

F0B.1~0 **CPUPSC:** System clock source prescaler.
00: divided by 8
01: divided by 4
10: divided by 2
11: divided by 1

R03	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWRDN	PWRDN							
R/W	W							
Reset	–	–	–	–	–	–	–	–

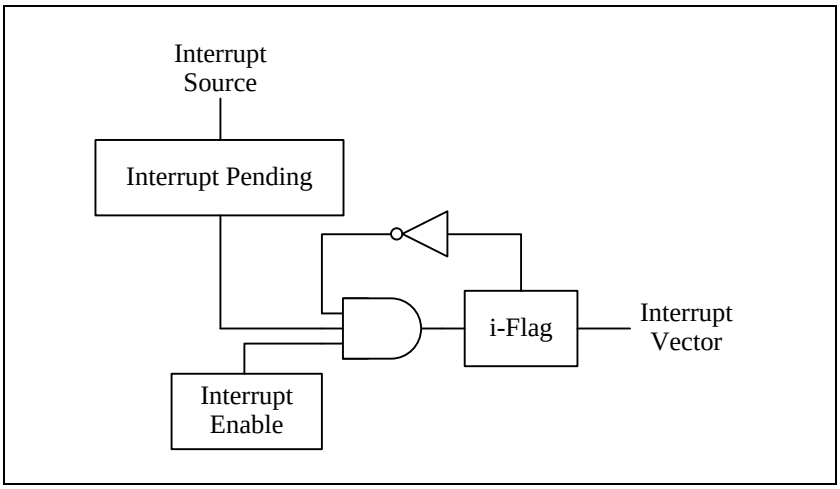
R03.7~0 **PWRDN:** Write this register (=SLEEP instruction) to enter IDLE or STOP Mode

7. Interrupt

This device has 1 level, 1 vector and 8 interrupt sources. Each interrupt source has its own enable control bit. An interrupt event will set its individual pending flag, no matter its enable control bit is 0 or 1.

If the corresponding interrupt enable bit has been set (INTIE), it would trigger CPU to service the interrupt. CPU accepts interrupt in the end of current executed instruction cycle. In the mean while, a "CALL 001" instruction is inserted to CPU, and i-flag is set to prevent recursive interrupt nesting.

The i-flag is cleared in the instruction after the "RETI" instruction. That is, at least one instruction in main program is executed before service the pending interrupt. The interrupt event is level triggered. F/W must clear the interrupt event register while serving the interrupt routine.



F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.7 **PWM0IE:** PWM0 interrupt enable
0: disable
1: enable

F08.6 **TM1IE:** Timer1 interrupt enable
0: disable
1: enable

F08.5 **RFCIE:** RFC interrupt enable
0: disable
1: enable

F08.4 **TM0IE:** Timer0 interrupt enable
0: disable
1: enable

F08.3 **T2IE:** T2 interrupt enable
0: disable
1: enable

F08.2 **INT2IE:** INT2 (PA7) interrupt enable
0: disable
1: enable

F08.1 **INT1IE:** INT1 (PB4) interrupt enable
0: disable

1: enable

F08.0 **INT0IE:** INT0 (PA0) interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.7 **PWM0IF:** PWM0 interrupt event pending flag
Set by H/W while PWM0 period completes, clear by S/W writing 0x7F to INTIF

F09.6 **TM1IF:** Timer1 interrupt event pending flag
Set by H/W while Timer1 overflows, clear by S/W writing 0xBF to INTIF

F09.5 **RFCIF:** RFC counter overflow interrupt event pending flag
Set by H/W while RFC counter overflow, clear by S/W writing 0xDF to INTIF

F09.4 **TM0IF:** Timer0 interrupt event pending flag
Set by H/W while Timer0 overflows, clear by S/W writing 0xEF to INTIF

F09.3 **T2IF:** T2 interrupt event pending flag
Set by H/W while T2 overflows, clear by S/W writing 0xF7 to INTIF

F09.2 **INT2IF:** INT2 (PA7) pin interrupt pending flag
Set by H/W at INT2 pin's falling/rising edge, clear by S/W writing 0xFB to INTIF

F09.1 **INT1IF:** INT1 (PB4) pin interrupt pending flag
Set by H/W at INT1 pin's falling/rising edge, clear by S/W writing 0xFD to INTIF

F09.0 **INT0IF:** INT0 (PA0) pin interrupt pending flag
Set by H/W at INT0 pin's falling/rising edge, clear by S/W writing 0xFE to INTIF

F0C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MF0C	T2CLR	T2CKS	TM0STP	TM1STP	TM1CLR	INT2EDG	INT1EDG	INT0EDG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0C.2 **INT2EDG:** INT2 pin (PA7) interrupt trigger edge select
0: falling edge to trigger
1: rising edge to trigger

F0C.1 **INT1EDG:** INT1 pin (PB4) interrupt trigger edge select
0: falling edge to trigger
1: rising edge to trigger

F0C.0 **INT0EDG:** INT0 pin (PA0) interrupt trigger edge select
0: falling edge to trigger
1: rising edge to trigger

8. I/O Port

I/O pins can be used as Schmitt-trigger input, CMOS push-pull output, or Open-drain output. The pull-up resistor is assignable to PA0~7, PB4~PB7 by S/W setting. To use the pin in Schmitt-trigger input mode, S/W needs to set the I/O pin to Mode0 or Mode1 and the corresponding port data PxD=1. Reading the pin data (PxD) has different meaning. In "Read-Modify-Write" instruction, CPU actually reads the output data register. In the others instructions, CPU reads the pin state. The so-called "Read-Modify-Write" instruction includes BSF, BCF and all instructions using F-Plane as destination.

The operations of four pin modes are listed as below.

PA0~PA6, PB4~PB7 supports all 4 pin modes,

PB0~PB3, PD0~PD3 supports Mode 1 (only Input without Pull-up, not include Open Drain function) and Mode2~3

PA7 only supports Mode 0~1.

Pin Mode	PxD SFR data	Pin State	Pull-up Resistor	Digital Input	Pin function
Mode 0	0	Drive Low	N	N	Open Drain output low without pull-high
	1	Pull-High	Y	Y	Input with pull-high
Mode 1	0	Drive Low	N	N	Open Drain output low without pull-high
	1	Hi-Z	N	Y	Input without pull-high
Mode 2	0	Drive Low	N	N	CMOS push-pull output
	1	Drive High	N	N	
Mode 3	1	–	N	N	Alternative function, such as LCD, PWM and RFC

I/O Pin Function Table (except PA7)

CFGWH.12	Pin Mode PA7MOD	PAD[7] SFR data	Pin State	Pull-up Resistor	Pin function
0	0	0	Drive Low	N	open-drain output low without pull-high
0	0	1	Pull-High	Y	Input with pull-high
0	1	0	Drive Low	N	open-drain output low without pull-high
0	1	1	Hi-Z	N	Input without pull-high
1	0	1	Pull-High	Y	Reset input with pull-high

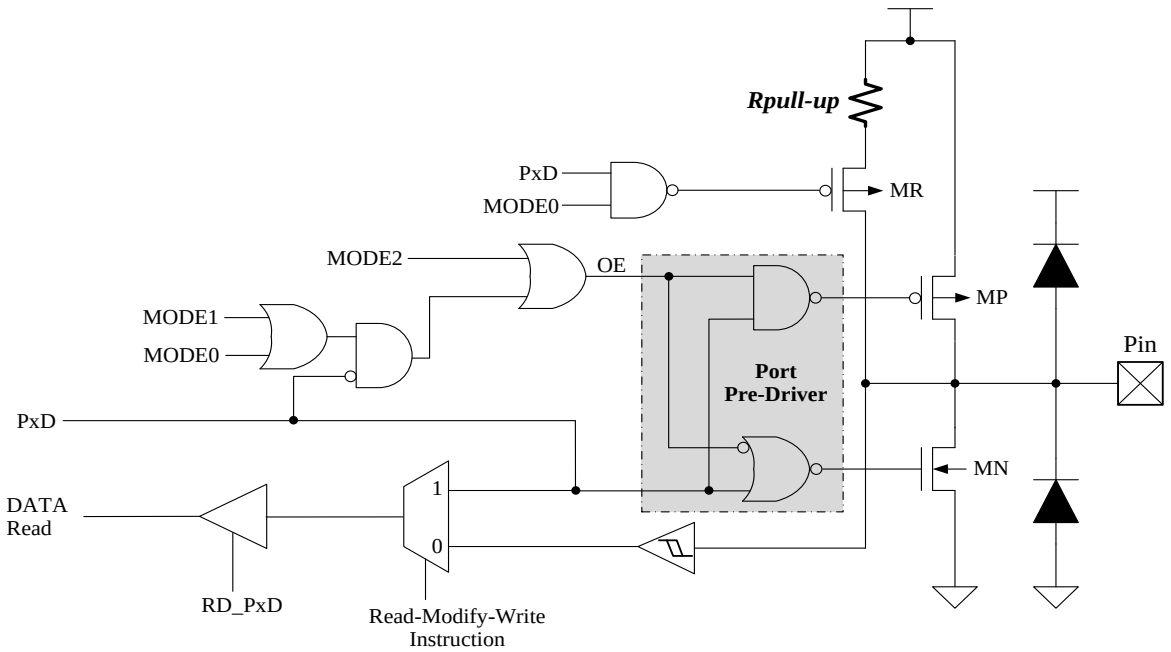
PA7 Pin Function Table

Beside general purposed I/O port function, each pin may have one or more alternative functions.

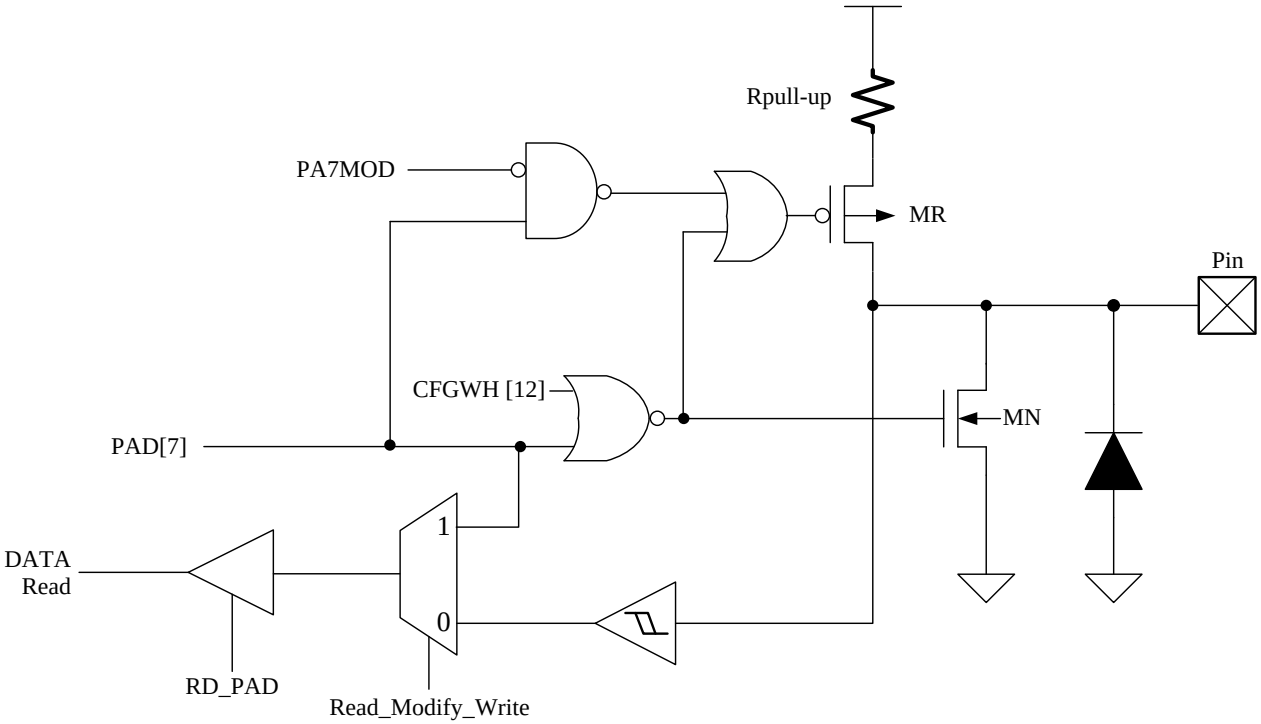
Pin Name	Interrupt	Wake-up	LCD	RFC	Others	Mode3
PA0	INT0			RFC1R		RFC1R
PA1				RFC2R	PWM0N	RFC2R
PA2				RFC0R		RFC0R
PA3					XOUT	
PA4					XIN	
PA5				RFCX		RFCX
PA6					PWM0P	PWM0P
PA7	INT2				nRESET	
PB0		Y	SEG28			SEG28
PB1		Y	SEG27			SEG27
PB2		Y	SEG26			SEG26
PB3		Y	SEG25			SEG25
PB4	INT1	Y			TM0CKI/CAPT	
PB5		Y			PWM1O	PWM1O
PB6		Y			TCOUT	TCOUT
PB7		Y		RFC3R		RFC3R
PD0			SEG45			SEG45
PD1			SEG44			SEG44
PD2			SEG43			SEG43
PD3			SEG42			SEG42

I/O Pin multi-function Table

Note: In SXT mode, user should set the PA3 and PA4 pins as Input with Pull-up (Mode 0).

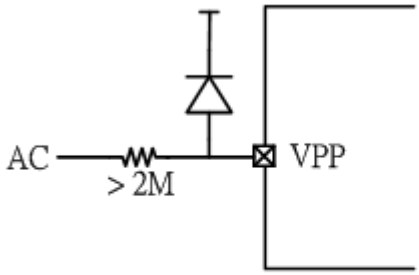


I/O Port Structure (except PA7)



PA7 Structure

Note: PA7(VPP) has no high voltage protection diode, need an external diode and resistor to achieve AC zero corssing detection. The reference circuit is shown below.



Zero crossing detector circuit for VPP pin

F05	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAD	PAD							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

F05.7~0 **PAD:** PA7~PA0 data

R05	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAMODH	–	PA7MOD	PA6MOD		PA5MOD		PA4MOD	
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	0	0	1	0	1	0	1

R05.6 **PA7MOD:** PA7 pin mode
0: Mode0, open-drain I/O with internal pull-up
1: Mode1, open-drain I/O without internal pull-up

R05.5~4 **PA6MOD:** PA6 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, PWM0P CMOS push pull output

R05.3~2 **PA5MOD:** PA5 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, RFCX input

R05.1~0 **PA4MOD:** PA4 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output

R06	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAMODL	PA3MOD		PA2MOD		PA1MOD		PA0MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

R06.7~6 **PA3MOD:** PA3 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output

R06.5~4 **PA2MOD:** PA2 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, RFC0R output

R06.3~2 **PA1MOD:** PA1 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, RFC2R output

R06.1~0 **PA0MOD:** PA0 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, RFC1R output

F06	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

PBD	PBD							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

F06.7~0 **PBD:** PB7~PB0 data

R07	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBMODH	PB7MOD		PB6MOD		PB5MOD		PB4MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

R07.7~6 **PB7MOD:** PB7 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, RFC3R output

R07.5~4 **PB6MOD:** PB6 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, TCOUT output

R07.3~2 **PB5MOD:** PB5 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, PWM1O output

R07.1~0 **PB4MOD:** PB4 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output

R08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBMODL	PB3MOD		PB2MOD		PB1MOD		PB0MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

R08.7~6 **PB3MOD:** PB3 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG25 output

R08.5~4 **PB2MOD:** PB2 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG26 output

R08.3~2 **PB1MOD:** PB1 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG27 output

R08.1~0 **PB0MOD:** PB0 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG28 output

F07	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDD	–	–	–	–	PDD			
R/W	–	–	–	–	R/W	R/W	R/W	R/W

Reset	1	1	1	1	1	1	1	1

F07.3~0 **PDD:** PD3~PD0 data

R09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDMODL	PD3MOD		PD2MOD		PD1MOD		PD0MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

R09.7~6 **PD3MOD:** PD3 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG42 output

R09.5~4 **PD2MOD:** PD2 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG43 output

R09.3~2 **PD1MOD:** PD1 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG44 output

R09.1~0 **PD0MOD:** PD0 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG45 output

R12	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBWKEN	PBWKEN							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R12.7~0 **PBWKEN:** PB7~PB0 low level wakeup
0: disable
1: enable

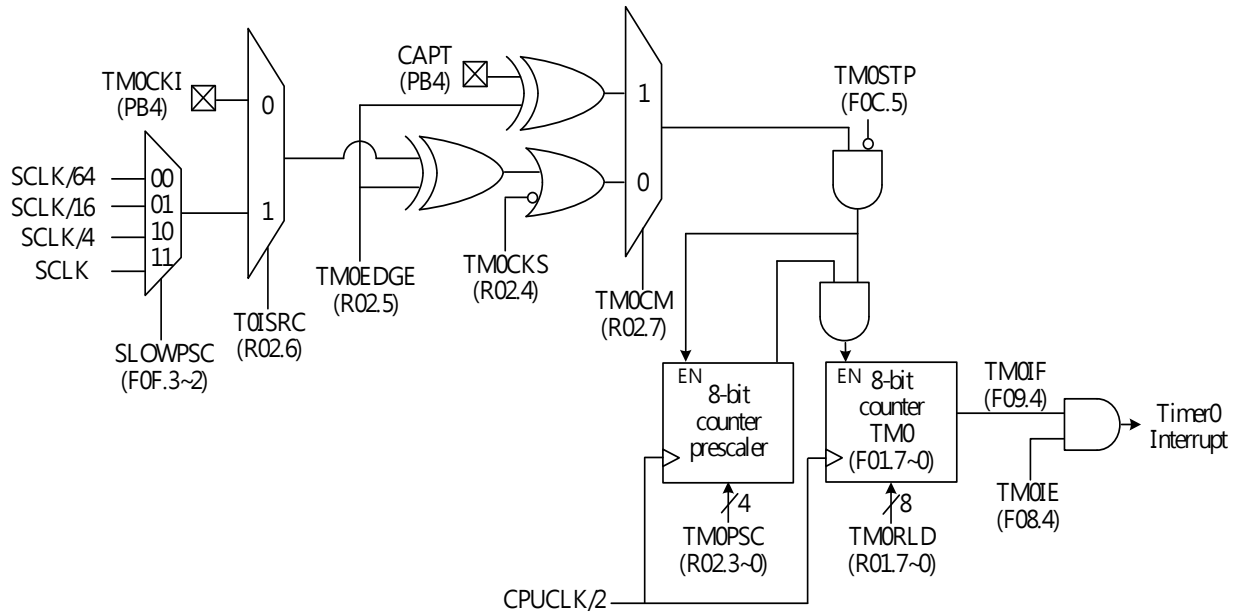
R0A	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0CTL	PWM0CKS	T2PSC		PWM0PSC			PWM0NOE	WDTPSC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

R0A.1 **PWM0NOE:** PWM0N output to PA1 pin
0: disable
1: enable

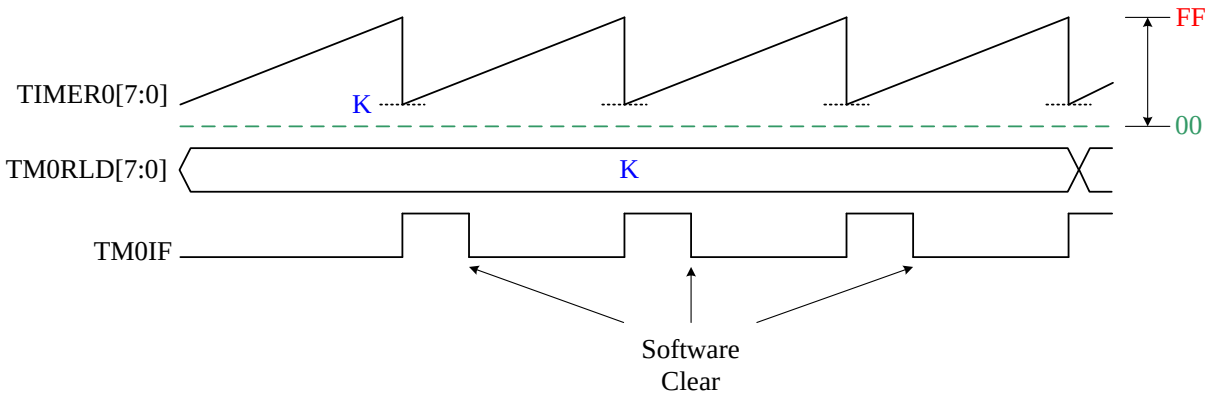
9. Timers

9.1 Timer0

The Timer0 is an 8-bit wide register of F-Plane 01h (TM0). It can be read or written the same way as any other register of F-Plane. Besides, Timer0 increases itself according to the pre-scaled clock source, which comes from the instruction cycle (Fsys/2) or Slow-clock divided by 1/4/16/64. The Timer0 increase rate is determined by "Timer0 Pre-Scale" (TM0PSC). The Timer0 sets TM0IF flag and reloads itself with TM0RLD when Timer0's count overflows. It generates Timer0 Interrupt if (TM0IE) is set. Timer0 can be stopped counting if the TM0STP bit is set.



Timer0 Block Diagram



Timer0 Timing Diagram

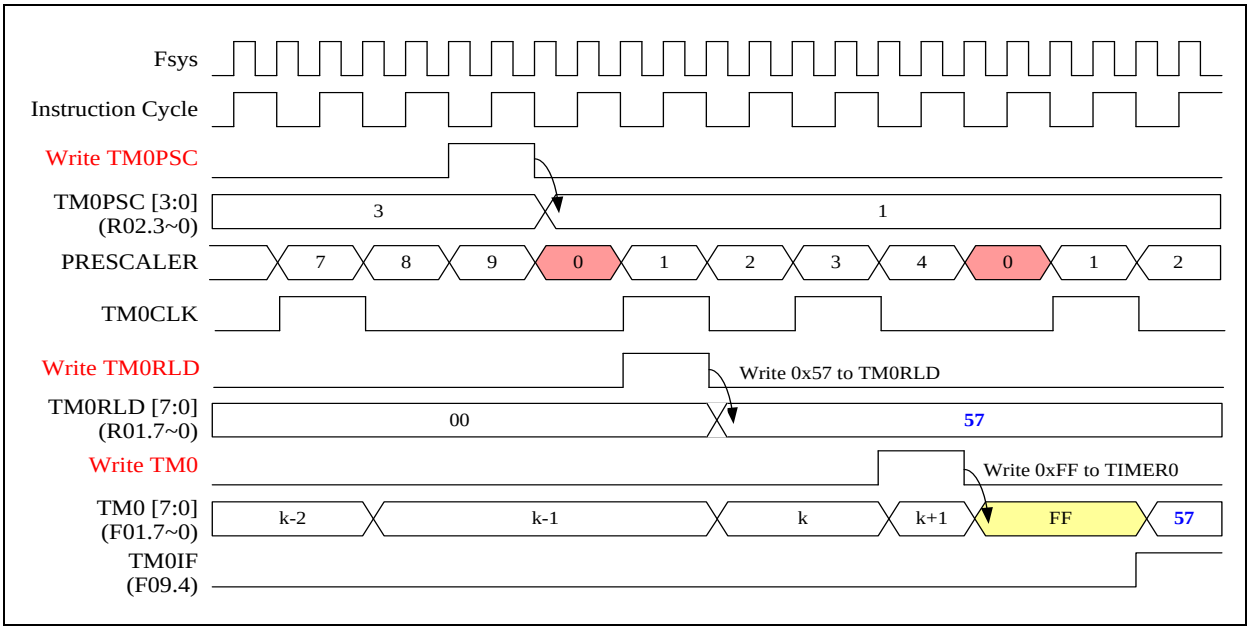
	Capture mode CAPT (PB4)	Timer mode	Counter mode TM0CKI (PB4)	Counter mode SCLK/1/4/16/64
TM0CM	1	0	0	0
TM0CKS	x	0	1	1
T0ISRC	x	x	0	1

Timer0 mode control signal table

Timer mode:

If TM0CM=0 and TM0CKS=0, Timer0 is in Timer mode.

When the Timer0 prescaler (TM0PSC) is written, the internal 8-bit prescaler will be cleared to 0 to make the counting period correct at the first Timer0 count. TM0CLK is the internal signal that causes the Timer0 to increase by 1 at the end of TM0CLK. TM0WR is also the internal signal that indicates the Timer0 is directly written by instruction; meanwhile, the internal 8-bit prescaler will be cleared. When Timer0 counts from FFh to TM0RLD, TM0IF will be set to 1 and generate interrupt if TM0IE is set.



Timer0 works in Timer mode (TM0CKS=0)

The equation of TM0 interrupt time value is as following:

TM0 interrupt frequency = (Fsys/2) / TM0PSC / (256-TM0)

◇ Example: Setup TM0 work in Timer mode

```
; Setup TM0 clock source and divider
        MOVLW   0000 0101B      ; R02.4 = 0, Setup TM0 clock=  Fsys/2
        MOVWR   R02             ; R02.3~0=5 (TM0PSC)
```

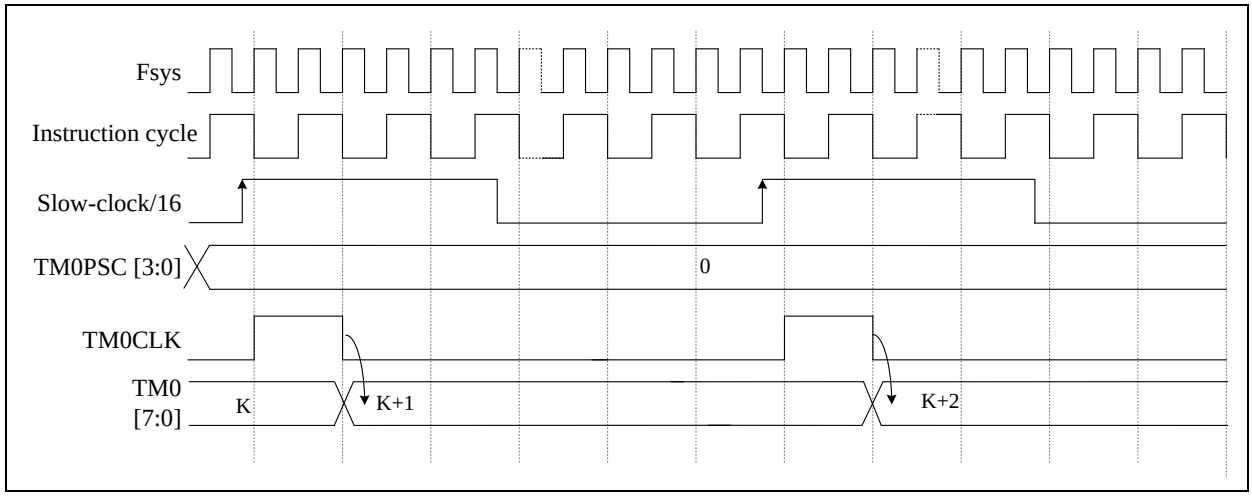
```
                                    ; TM0 clock prescaler = Fsys/64
; Set TM0 timer.
        BSF     TM0STP      ; Disable TM0 counting (Default "0").
        MOVLW   156
        MOVWF   TM0         ; Write 156 into TM0 register of F-Plane. (F01)
        MOVLW   124
        MOVWR   TM0RLD      ; Write 124 into TM0RLD register of R-Plane. (R01)

; Enable TM0 timer and interrupt function.
        MOVLW   1110 1111B  ; Clear TM0 request interrupt flag by byte operation
        MOVWF   INTIF       ; F-Plane 09H
        MOVLW   0001 0000B  ; Enable TM0 interrupt function
        MOVWF   INTIE       ; F-Plane 08H
        BCF     TM0STP      ; Enable TM0 counting (Default “0”).
```

Counter mode:

If TM0CM=0 and TM0CKS=1, Timer0 is in counter mode.

There are two kinds of counter mode source in this chip. If T0ISRC=0, Timer0’s counter mode source is TM0CKI (PB4). If T0ISRC=1, Timer0’s counter mode source is “Slow-clock divided by 1/4/16/64”.These sources are synchronized by instruction cycle (Fsys/2). That means the instruction cycle (Fsys/2) must be faster than counter mode source for proper operation.



TM0CKS=1, Timer0 clock source is Slow-clock/16

Capture mode:

If TM0CM=1, Timer0 is in capture mode.

User can measure the signal on CAPT pin by Timer0 capture mode and Timer1 capture mode. More introduction about capture mode lists in the chapter of Timer1.

F01	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0	TM0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset	0	0	0	0	0	0	0	0

F01.7~0 **TM0:** Timer0 data

F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.4 **TM0IE:** Timer0 interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.4 **TM0IF:** Timer0 interrupt event pending flag
Set by H/W while Timer0 overflows, clear by S/W writing 0xEF to INTIF

F0C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MF0C	T2CLR	T2CKS	TM0STP	TM1STP	TM1CLR	INT2EDG	INT1EDG	INT0EDG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0C.5 **TM0STP:** Timer0 counter stop
0: Timer0 is counting
1: Timer0 stop counting

F0F	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCTL	RFCLR	T1STPRFC	T0STPRFC	RFCSTP	SLOWPSC		RFCHS	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	1	1	1	0	0

F0F.3~2 **SLOWPSC:** slow clock divider for Timer0
00: divided by 64
01: divided by 16
10: divided by 4
11: divided by 1

R01	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0RLD	TM0RLD							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R01.7~0 **TM0RLD:** Timer0 Overflow Reload Data

R02	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0CTL	TM0CM	T0ISRC	TM0EDGE	TM0CKS	TM0PSC			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

R02.7 **TM0CM:** Timer0 Capture mode enable
0: Timer mode or Counter mode
1: Capture mode

R02.6 **T0ISRC:** Timer0 Counter mode source
0: TM0CKI pin (PB4)
1: Slow-clock div 1/4/16/64 sets by SLOWPSC(F0F.3~2)

R02.5 **TM0EDGE**:
If TM0EDGE=1, TM0CKI/CAPT input data will be reversed.

Timer0 prescaler counting edge for Counter mode
0: Rising edge
1: Falling edge
Timer0 capture level for Capture mode
0: High level capture
1: Low level capture
Timer1 capture edge for Capture mode
0: Falling edge capture
1: Rising edge capture

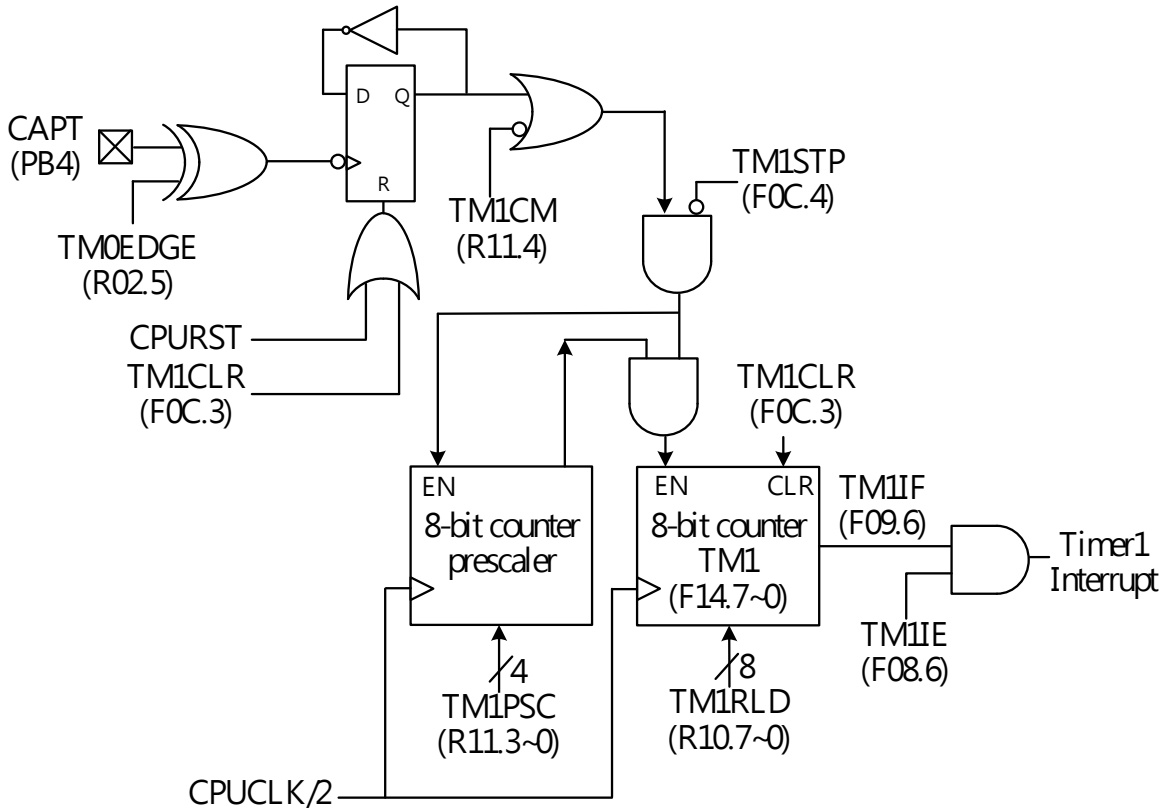
R02.4 **TM0CKS:** Timer0 mode select
0 : Timer mode (Fsys/2)
1 : Counter mode (SCLK divided 1/4/16/64 or T0CKI(PB4))

R02.3~0 **TM0PSC:** Timer0 clock source prescaler. Clock source is divided by

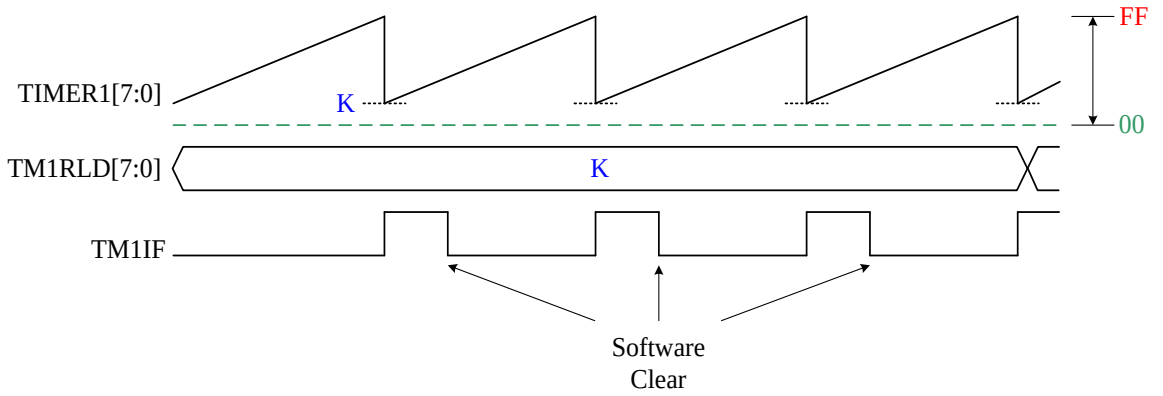
0000: Fsys/2	0101: Fsys/64
0001: Fsys/4	0110: Fsys/128
0010: Fsys/8	0111: Fsys/256
0011: Fsys/16	1xxx: Fsys/512
0100: Fsys/32	

9.2 Timer1

Timer1 is an 8-bit register of F-Plane. It can be read or written as any other register of F-Plane. There are two kinds of mode. One is timer mode, another one is capture mode. It is almost the same as Timer0, except Timer1 doesn't have Counter Mode and Timer1's Capture mode capture event is different from Timer0. Timer1 increases itself periodically and automatically rolls over based on the pre-scaled instruction cycle (Fsys/2). Timer1's increasing rate is determined by TM1PSC. Timer1 can generate interrupt flag TM1IF and also reload the new data from TM1RLD when it rolls over. It generates Timer1 interrupt if the TM1IE bit is set. Timer1 can be paused if TM1STP bit is set.



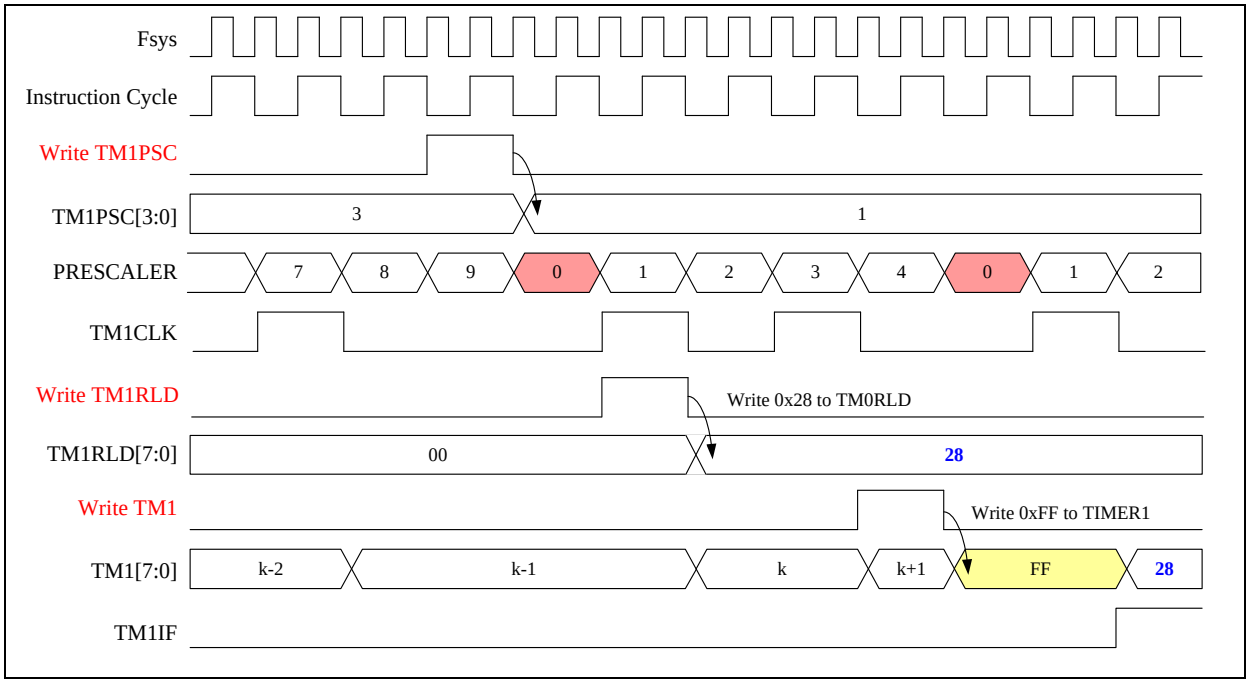
Timer1 Block Diagram



Timer1 Reload Diagram

Timer mode:

If TM1CM=0, Timer1 is in timer mode.

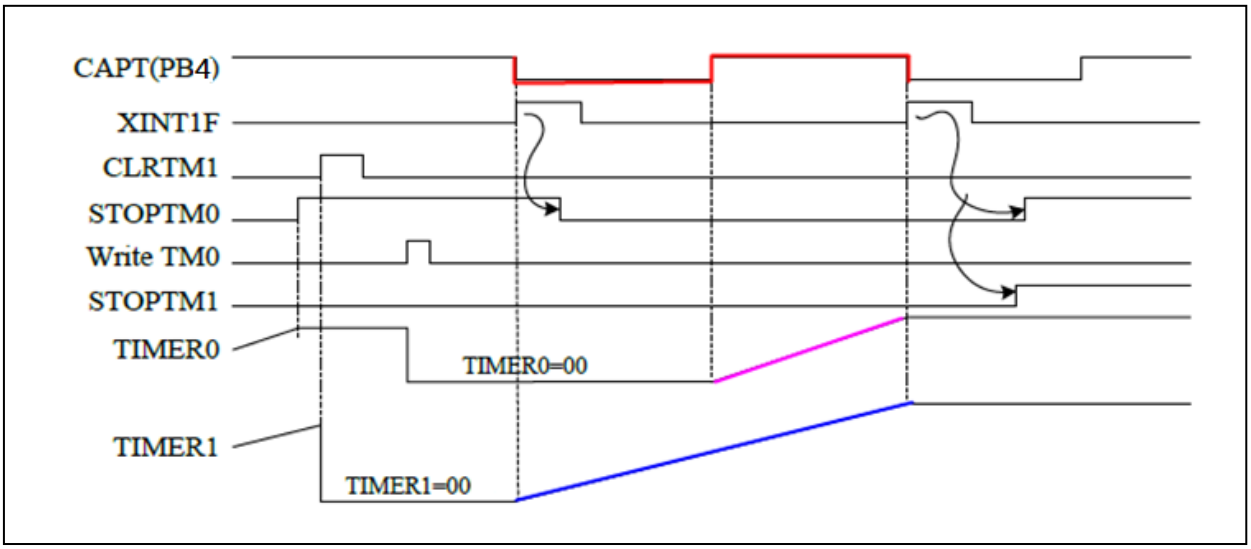


Timer1 Timing Diagram

Capture mode:

If TM1CM=1, Timer1 is in capture mode.

User can measure the signal on CAPT pin by Timer0 capture mode and Timer1 capture mode. If TM0EDGE=0, Timer0 is running when CAPT is high level, Timer1 counter pauses/resumes when CAPT is falling edge. If TM0EDGE=1, Timer0 is running when CAPT is low level, Timer1 counter pauses/resumes when CAPT is rising edge. See the figure below.



Timer0 and Timer1 used to measure the signal on CAPT pin

F14	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1	TM1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F14.7~0 **TM1:** Timer1 data

F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.6 **TM1IE:** Timer1 interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.6 **TM1IF:** Timer1 interrupt event pending flag
Set by H/W while Timer1 overflows, clear by S/W writing 0xBF to INTIF

F0C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MF0C	T2CLR	T2CKS	TM0STP	TM1STP	TM1CLR	INT2EDG	INT1EDG	INT0EDG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0C.4 **TM1STP:** Timer1 counter stop
0: Timer1 is counting
1: Timer1 stop counting

F0C.3 **TM1CLR:** Timer1 clear and hold when this bit is "1" in timer mode/capture mode

R02	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0CTL	TM0CM	T0ISRC	TM0EDGE	TM0CKS	TM0PSC			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

R02.5 **TM0EDGE**:
If TM0EDGE=1, TM0CKI/CAPT input data will be reversed.

Timer0 prescaler counting edge for Counter mode
0: Rising edge
1: Falling edge
Timer0 capture level for Capture mode
0: High level capture
1: Low level capture
Timer1 capture edge for Capture mode
0: Falling edge capture
1: Rising edge capture

R10	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1RLD	TM1RLD							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

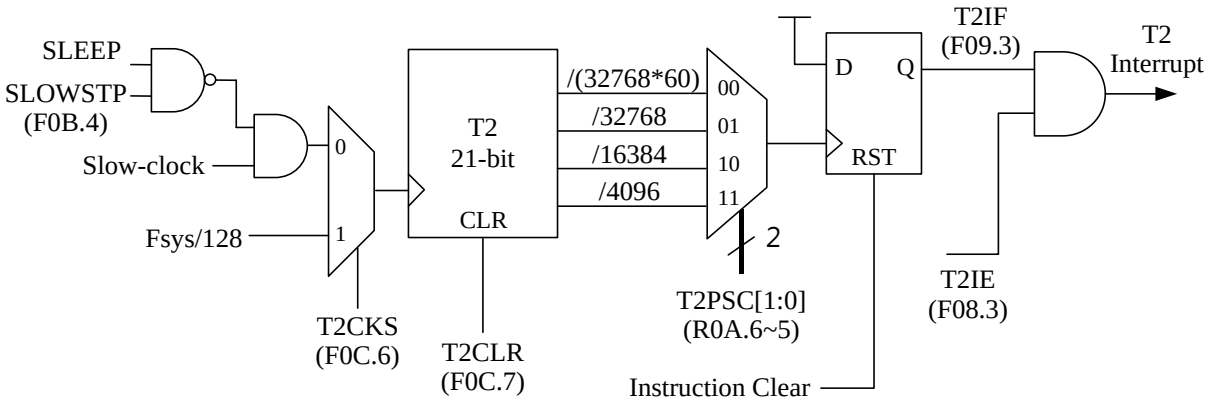
R10.7~0 **TM1RLD:** Timer1 Overflow Reload Data

R11	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1CTL	-	-	-	TM1CM	TM1PSC			
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset	-	-	-	0	0	0	0	0

R11.4 **TM1CM:** Timer1 Capture mode
0: Timer mode
1: Capture mode
R11.3~0 **TM1PSC:** Timer1 clock source prescaler. Clock source is divided by
0000: 1
0001: 2
0010: 4
0011: 8
0100: 16
0101: 32
0110: 64
0111: 128
1xxx: 256

9.3 Timer2

Timer2 (T2) is a 21-bit timer and the clock sources are from either Fsys/128 or Slow-clock. The clock source is used to generate time base interrupt and T2 module clock. It is selected by T2CKS (F0C.6). The T2's 21-bit content cannot be read by instructions. It generates interrupt flag T2IF (F09.3) with the clock divided by 32768*60, 32768, 16384, or 4096 depends on the T2PSC[1:0] (R08.6~5) bits. The following figure shows the block diagram of T2.



T2 Block Diagram

◇ Example: CPU is running at FAST mode, Fsys=Fast-clock=FIRC, Slow-clock source is SXT

```
; Setup T2 clock source and divider
        BCF     T2CKS       ; T2CKS=0, T2 clock source is Slow-clock
        MOVLW   0 01 00000B
        MOVWR   R0A         ; T2PSC=01b, divided by 32768
        BSF     T2CLR       ; T2CLR=1, clear T2 counter

; Enable T2 interrupt function
        MOVLW   1111 0 111B
        MOVWF   INTIF       ; Clear T2 request interrupt flag
        BSF     T2IE        ; Enable T2 interrupt function
```

T2 clock source is Slow-clock = 32 KHz, T2 divided by 32768
T2 interrupt period =1 second

F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.3 **T2IE:** T2 interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.3 **T2IF:** T2 interrupt event pending flag
Set by H/W while T2 overflows, clear by S/W writing 0xF7 to INTIF

F0C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MF0C	T2CLR	T2CKS	TM0STP	TM1STP	TM1CLR	INT2EDG	INT1EDG	INT0EDG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0C.7 **T2CLR**: T2 counter clear
0: T2 is counting
1: T2 is cleared, this bit is auto cleared by H/W

F0C.6 **T2CKS:** T2 clock source selection
0: Slow-clock
1: Fsys/128

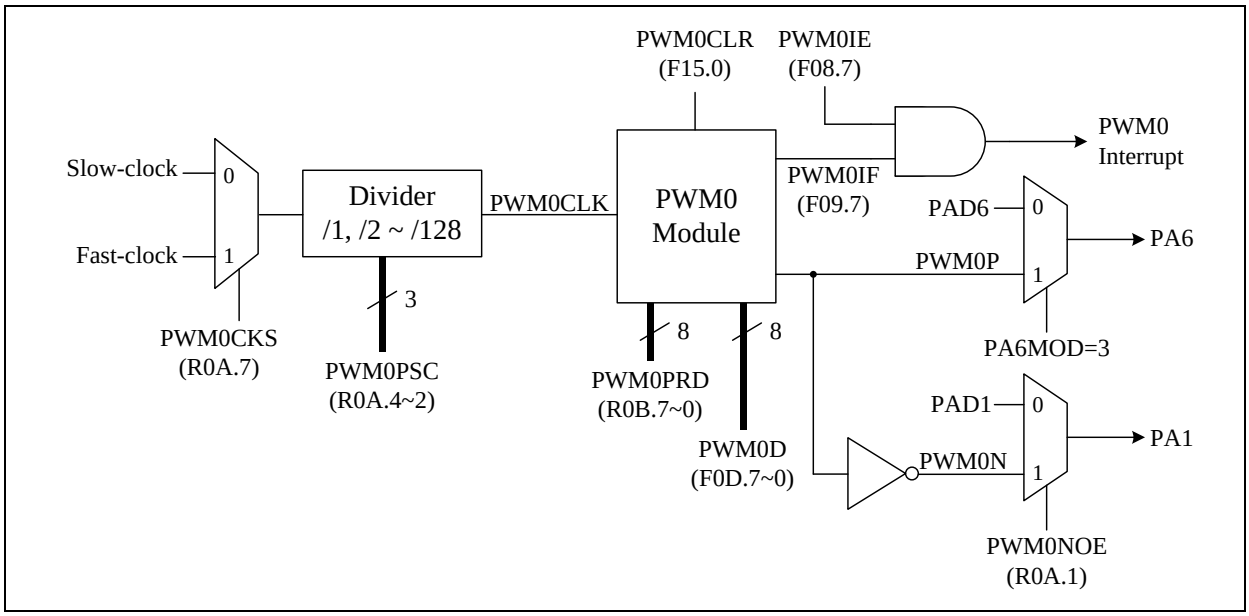
R0A	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0CTL	PWM0CKS	T2PSC		PWM0PSC			PWM0NOE	WDTPSC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

R0A.6~5 **T2PSC:** T2 prescaler. T2 interrupt is T2 clock is divided by
00: (32768*60)
01: 32768
10: 16384
11: 4096

10. PWM

10.1 PWM0

The PWM0 can select Fast-clock or Slow-clock as its clock source, with divided by 1~128 prescaler. The PWM0 period is adjustable by PWM0PRD and its 256 step duty cycle is controlled by PWM0D. The PWM0P and PWM0N are positive and negative CMOS output pairs to pins.



PWM0 Block Diagram

◇ Example: Slow-clock = SXT 32768Hz

```
; Setup PWM0P a 512Hz, 50% duty cycle output
        MOVLW   0001110 0B      ; PWM0CKS=0, PWM0PSC=111
        MOVWR   PWM0CTL         ; PWM0CLK=Slow-clock/1=32768Hz

        MOVLW   63
        MOVWR   PWM0PRD         ; Set PWM0 period = 63 + 1 = 64

        MOVLW   32
        MOVWF   PWM0D           ; Set PWM0 duty = 32

        MOVLW   0011 0000B      ; PA6MOD=3
        MOVWR   PAMODH          ; PWM0P output to PA6 pin
```

PWM0 clock frequency = Slow-clock / PWM0PSC = 32768Hz / 1 = 32768Hz
PWM0 output frequency = PWM0CLK / (PWM0PRD + 1) = 32768Hz / (63 + 1) = 512 Hz
PWM0 duty cycle = PWM0D / (PWM0PRD + 1) = 32 / (63 + 1) = 50%

F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.7 **PWM0IE:** PWM0 interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.7 **PWM0IF:** PWM0 interrupt event pending flag
Set by H/W while PWM0 period completes, clear by S/W writing 0x7F to INTIF

F15	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCLR							PWM1CLR	PWM0CLR
R/W							R/W	R/W
Reset							0	0

F15.0 **PWM0CLR:** PWM0 clear and hold
0: PWM0 running 1: PWM0 clear and hold

R0A	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0CTL	PWM0CKS	T2PSC		PWM0PSC			PWM0NOE	WDTPSC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

R0A.7 **PWM0CKS:** PWM0 clock source select
0: Slow-clock
1: Fast-clock

R0A.4~2 **PWM0PSC**: PWM0 clock prescaler
000: PWM0 clock is Slow/Fast clock divided by 128
001: PWM0 clock is Slow/Fast clock divided by 64
010: PWM0 clock is Slow/Fast clock divided by 32
011: PWM0 clock is Slow/Fast clock divided by 16
100: PWM0 clock is Slow/Fast clock divided by 8
101: PWM0 clock is Slow/Fast clock divided by 4
110: PWM0 clock is Slow/Fast clock divided by 2
111: PWM0 clock is Slow/Fast clock divided by 1

R0A.1 **PWM0NOE:** PWM0N output to PA1 pin
0: disable
1: enable

F0D	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0D	PWM0D							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

F0D.7~0 **PWM0D**: PWM0 duty, 0=0 PWM0CLK, 80h=128 PWM0CLK, FFh=255 PWM0CLK

R09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

PWM0PRD	PWM0PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

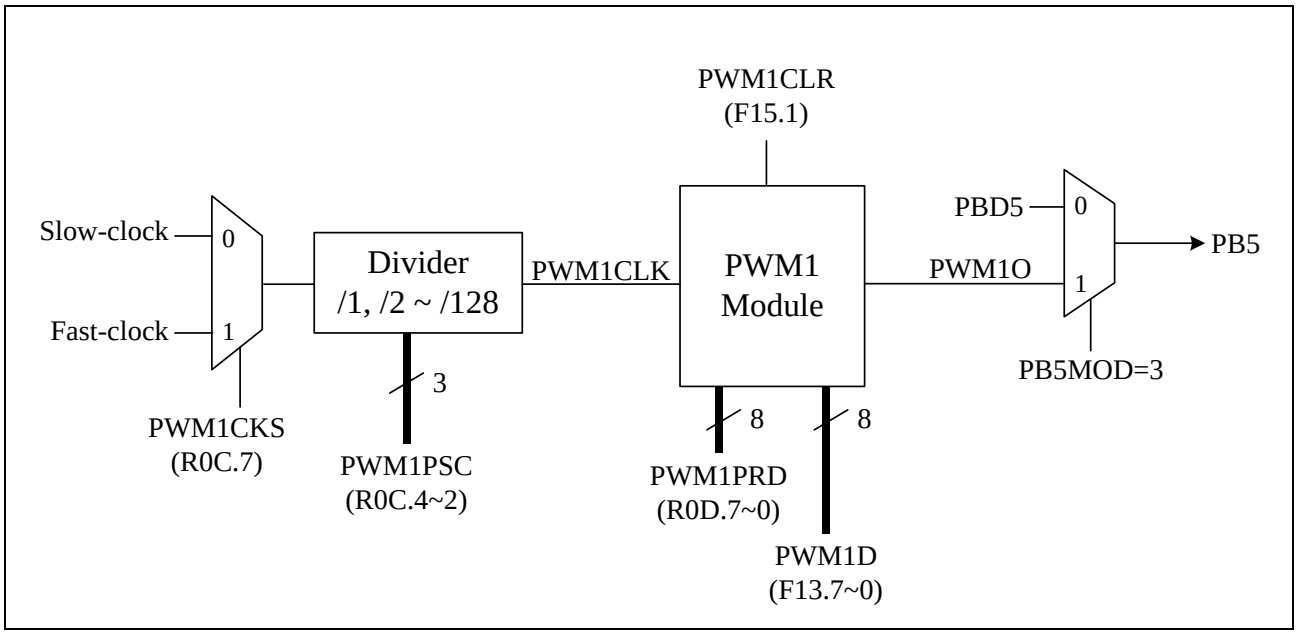
R09.7~0 **PWM0PRD**: PWM0 period, FFh=256 PWM0CLK, 7Fh=128 PWM0CLK

R05	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAMODH	–	PA7MOD	PA6MOD		PA5MOD		PA4MOD	
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	0	0	1	0	1	0	1

R05.5~4 **PA6MOD:** PA6 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, PWM0P CMOS push pull output

10.2 PWM1

The PWM1 can select Fast-clock or Slow-clock as its clock source, with divided by 1~128 prescaler. The PWM1 period is adjustable by PWM1PRD and its 256 step duty cycle is controlled by PWM1D. The PWM1O is positive CMOS output to pin.



PWM1 Block Diagram

R0C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1CTL	PWM1CKS	–	–	PWM1PSC			–	–
R/W	R/W	–	–	R/W	R/W	R/W	–	–
Reset	1	–	–	0	0	0	–	–

R0C.7 **PWM1CKS:** PWM1 clock source select
0: Slow-clock
1: Fast-clock

R0C.4~2 **PWM1PSC**: PWM1 clock prescaler
000: PWM1 clock is Slow/Fast clock divided by 128
001: PWM1 clock is Slow/Fast clock divided by 64
010: PWM1 clock is Slow/Fast clock divided by 32
011: PWM1 clock is Slow/Fast clock divided by 16
100: PWM1 clock is Slow/Fast clock divided by 8
101: PWM1 clock is Slow/Fast clock divided by 4
110: PWM1 clock is Slow/Fast clock divided by 2
111: PWM1 clock is Slow/Fast clock divided by 1

F13	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1D	PWM1D							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

F13.7~0 **PWM1D**: PWM1 duty, 0=0 PWM1CLK, 80h=128 PWM1CLK, FFh=255 PWM1CLK

F15	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCLR							PWM1CLR	PWM0CLR
R/W							R/W	R/W
Reset							0	0

F15.1 **PWM1CLR:** PWM1 clear and hold
0: PWM1 running 1: PWM1 clear and hold

R0D	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRD	PWM1PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

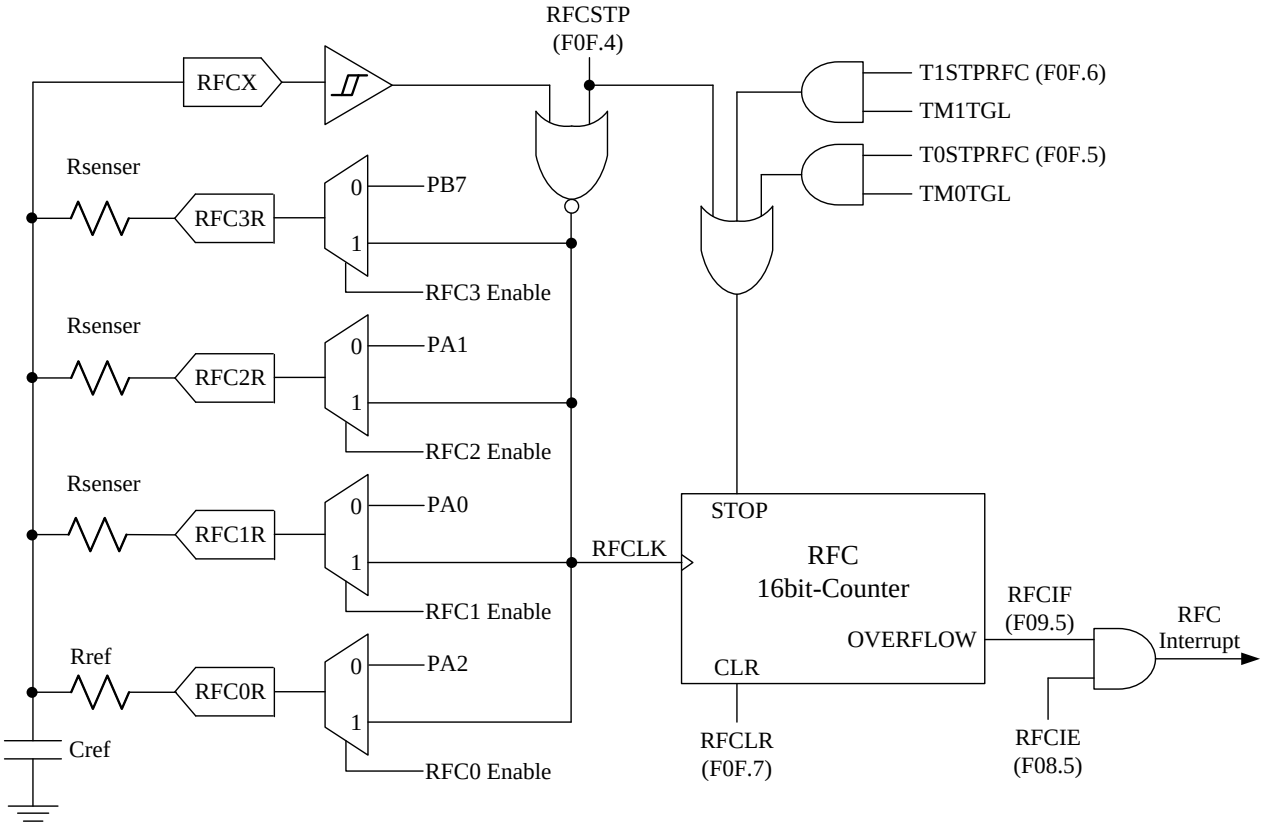
R0D.7~0 **PWM1PRD**: PWM1 period, FFh=256 PWM1CLK, 7Fh=128 PWM1CLK

R07	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBMODH	PB7MOD		PB6MOD		PB5MOD		PB4MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

R07.3~2 **PB5MOD:** PB5 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, PWM1O CMOS push pull output

11. Resistance to Frequency Converter (RFC)

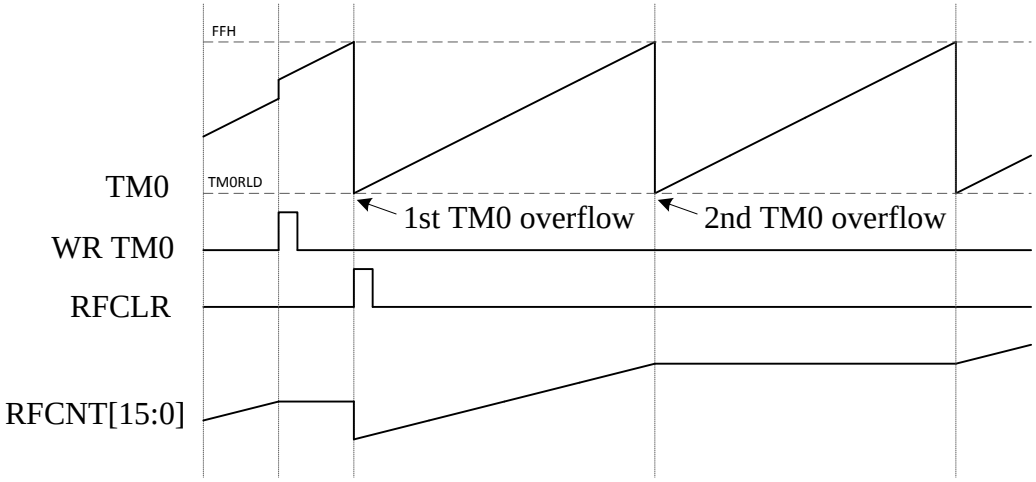
The RFC module contains RC oscillator and RFC counter. The RFC-clock comes from the oscillation circuitry built by RFCX pin and RFC0R, RFC1R, RFC2R or RFC3R pins.



RFC Block Diagram

The 16-bit RFC counter can stop by Timer0 or Timer1's overflow control. This function helps the RFC counter to count the RFC clock with more accuracy by H/W automatically start and stop. The steps of this usage are described below.

1. RFCSTP=0, T0STPRFC=1, T1STPRFC=0
2. Write Timer0 to setup a suitable overflow. Meanwhile, HW auto set TM0TGL=1 and RFCNT stops.
3. Clear RFCNT[15:0] by RFCLR=1
4. After the 1st Timer0 overflow, TM0TGL=0 and RFCNT start counting
5. Wait for the 2nd Timer0 overflow, TM0TGL=1 and RFCNT stops again, then read RFCNT data.



TM0 control RFC

F0F	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCTL	RFCLR	T1STPRFC	T0STPRFC	RFCSTP	SLOWPSC		RFCHS	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	1	1	1	0	0

F0F.7 **RFCLR:** clear RFC counter
0: RFC counter run
1: RFC counter clear

F0F.6 **T1STPRFC:** Timer1 overflow toggle signal (TM1TGL) to stop RFC counter
0: disable
1: enable

F0F.5 **T0STPRFC:** Timer0 overflow toggle signal (TM0TGL) to stop RFC counter
0: disable
1: enable

F0F.4 **RFCSTP:** S/W stop RFC counter and oscillator
0: RFC counter and oscillator run
1: RFC counter and oscillator stop

F0F.1~0 **RFCHS:** select RFC oscillator channel
00: RFC0R (PA2)
01: RFC1R (PA0)
10: RFC2R (PA1)
11: RFC3R (PB7)

F11	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCNTH	RFCNTH							
R/W	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

F11.7~0 **RFCNTH:** RFC counter high byte, RFCNT[15:8]

F12	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCNTL	RFCNTL							
R/W	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

F12.7~0 **RFCNTL:** RFC counter low byte, RFCNT[7:0]

F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.5 **RFCIE:** RFC interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.5 **RFCIF:** RFC counter overflow interrupt event pending flag
Set by H/W while RFC counter overflow, clear by S/W writing 0xDF to INTIF

12. LCD Driver

When LCDON = 1, LCD driver enable. If set LCD Bias=1/3, typical LCD Bias voltage is $1/3V_{LCD}$, $2/3\ V_{LCD}$ and V_{LCD}. If set LCD Bias=1/2, typical LCD Bias voltage = $1/2V_{LCD}$ and V_{LCD}.

VBAT 3V application (M5620/40):

User can only set 1/3Bias.

VBAT 1.5V application (M5625/45):

User can set 1/3Bias or 1/2Bias.

When LCDON = 1, the LCD pump is work and VLCD is pump up to 2*VBAT. User can set different pump frequency by PUMPCKS.

LCD Duty setting:

P/N	LCDUTY	LCD (SEG x COM) Max.
TM57M5620	1	28 x 4
TM57M5625	1	26 x 4
TM57M5640	1	44 x 4
TM57M5645	1	42 x 4
TM57M5620	0	29 x 3
TM57M5625	0	27 x 3
TM57M5640	0	45 x 3
TM57M5645	0	43 x 3

LCD Frame rate setting:

User can choose different LCD frame rate by LCDFRM. The LCD frame rate is related to Slow clock frequency and is not related to CPUCLK pre-scalar (CPUPSC). The table below is an example which assume user set Slow clock as SXT32768Hz.

LCDUTY	LCDFRM	LCD 帧率 @SXT32768Hz
1/4 DUTY	0	47Hz
1/4 DUTY	1	57Hz
1/4 DUTY	2	73Hz
1/4 DUTY	3	85Hz
1/3 DUTY	0	49Hz
1/3 DUTY	1	57Hz
1/3 DUTY	2	68Hz
1/3 DUTY	3	85Hz

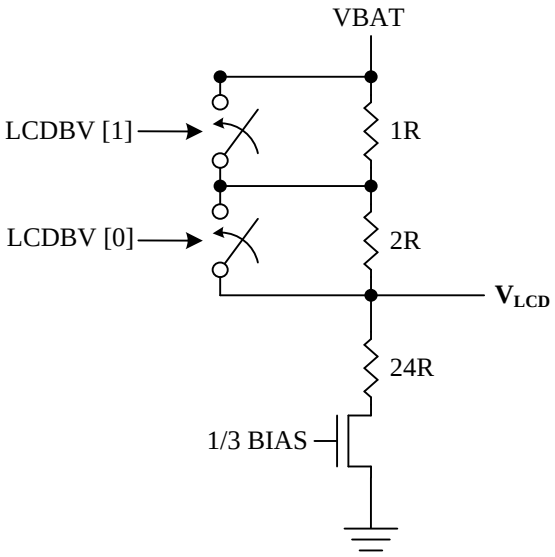
LCD frame rate @SXT32768Hz

LCD Brightness setting：(only for 1/3 bias)

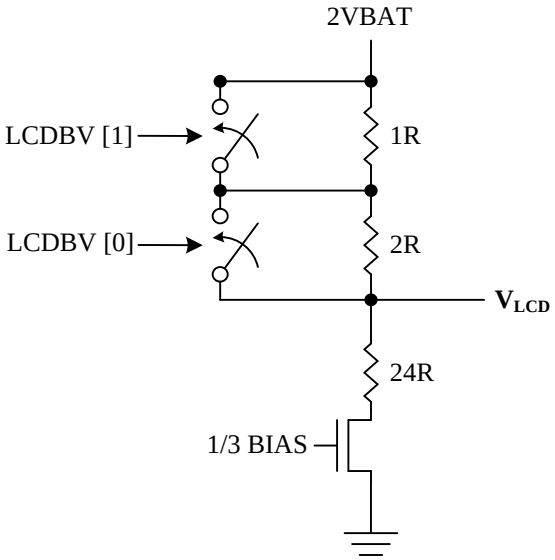
LCDBV[1:0]	LCDBIAS	M5620/40	M5625/45 (LCDON=1)
00	1/3 BIAS	V_{LCD}=0.89*VBAT	V_{LCD}=0.89*2VBAT
01	1/3 BIAS	V_{LCD}=0.92*VBAT	V_{LCD}=0.92*2VBAT
10	1/3 BIAS	V_{LCD}=0.96*VBAT	V_{LCD}=0.96*2VBAT
11	1/3 BIAS	V_{LCD}=VBAT	V_{LCD}=2VBAT
Don’t care	1/2 BIAS	N/A	V_{LCD}=2VBAT

V_{LCD} 与 LCD 亮度调节

M5620/40:



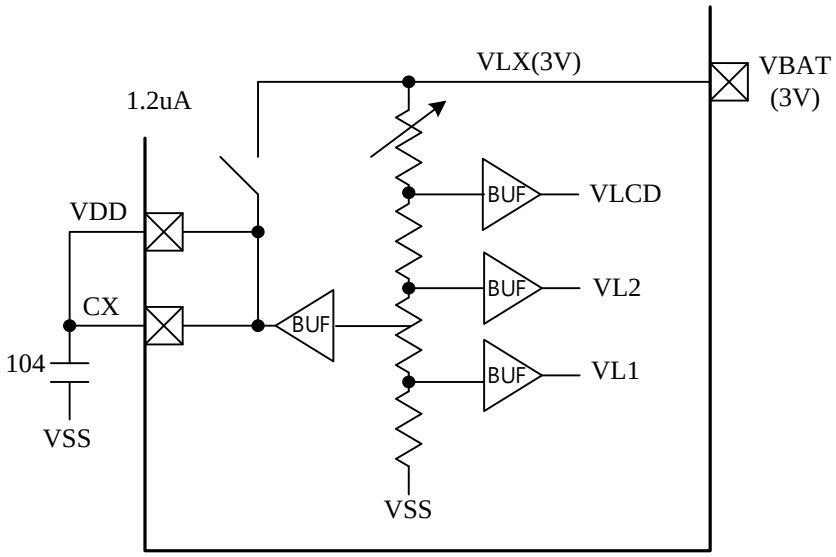
M5625/45: (LCDON=1)



LCD IOPAD setting:

M5620/40：

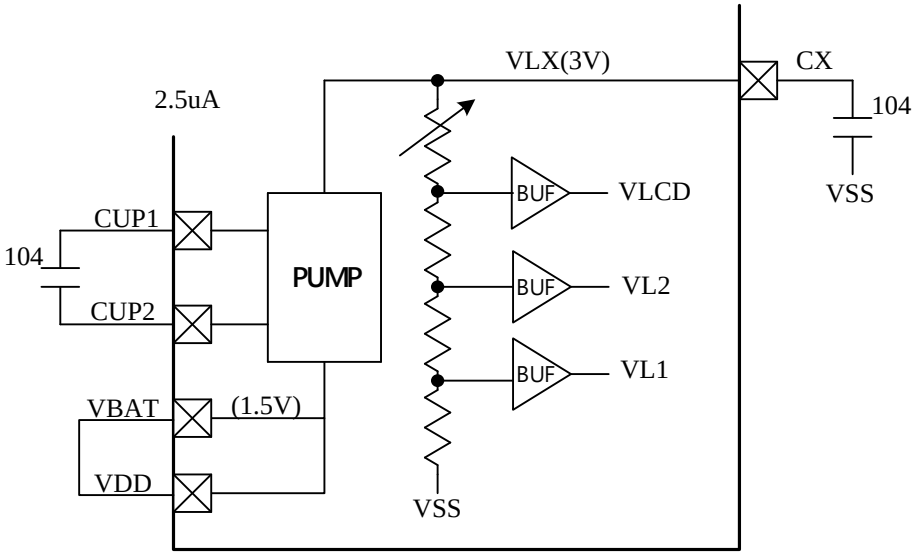
CXPAD connected to a capacitor and both CUP1 PAD and CUP1 PAD as LCD SEG.



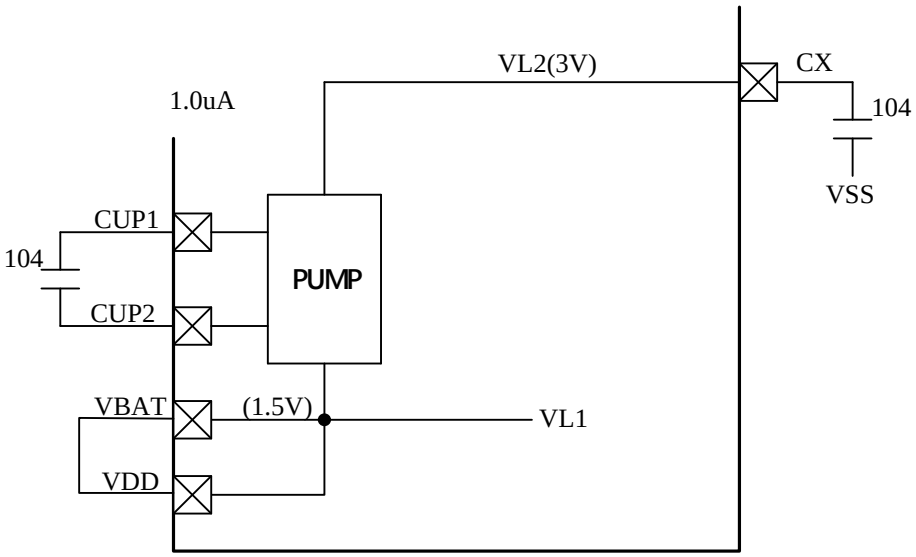
M5620/40, 1/3 Bias

M5625/45：

CXPAD connected to a capacitor and CUP1 PAD and CUP1 PAD connected together by a capacitor for LCD pump.

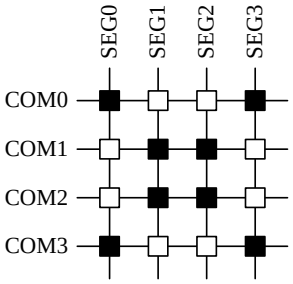


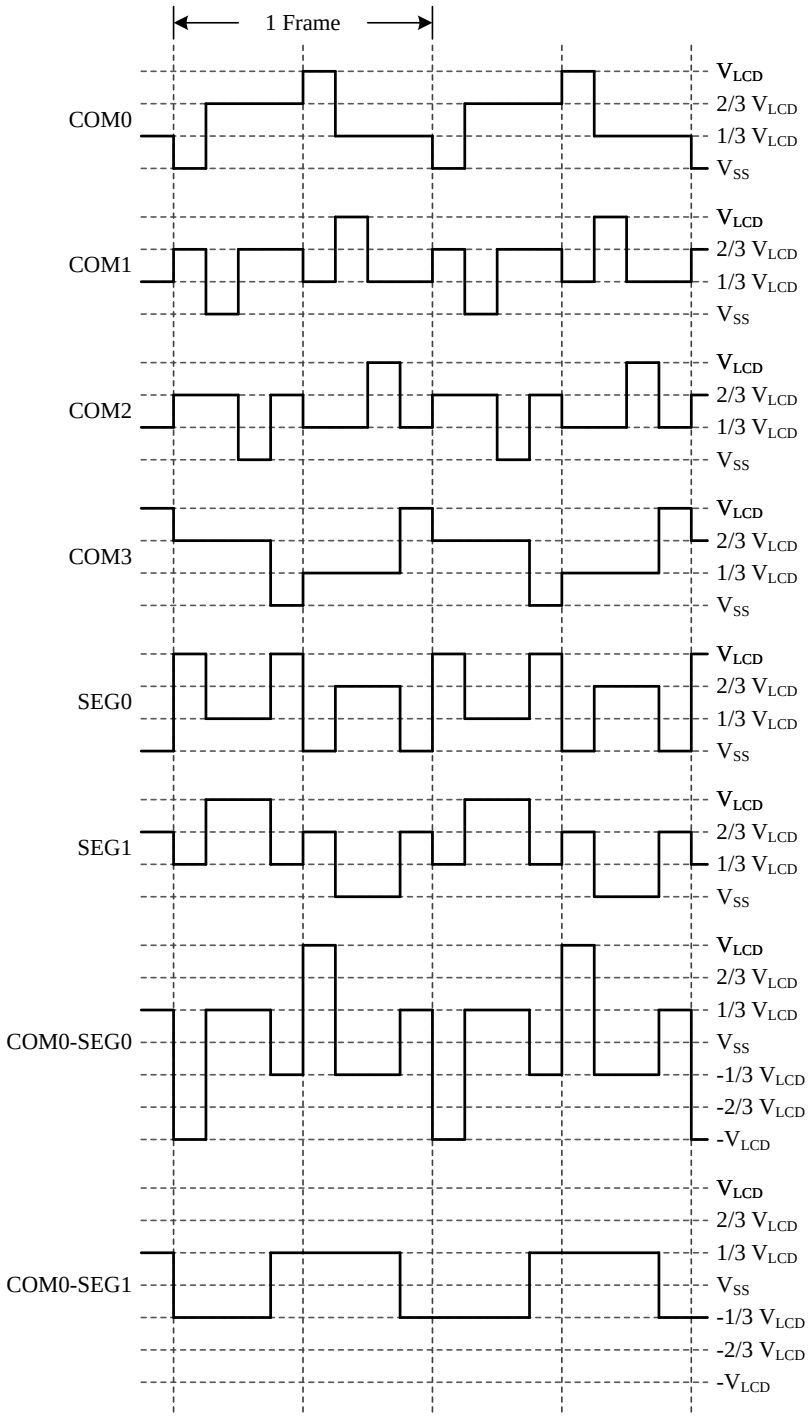
M5625/45, 1/3 Bias



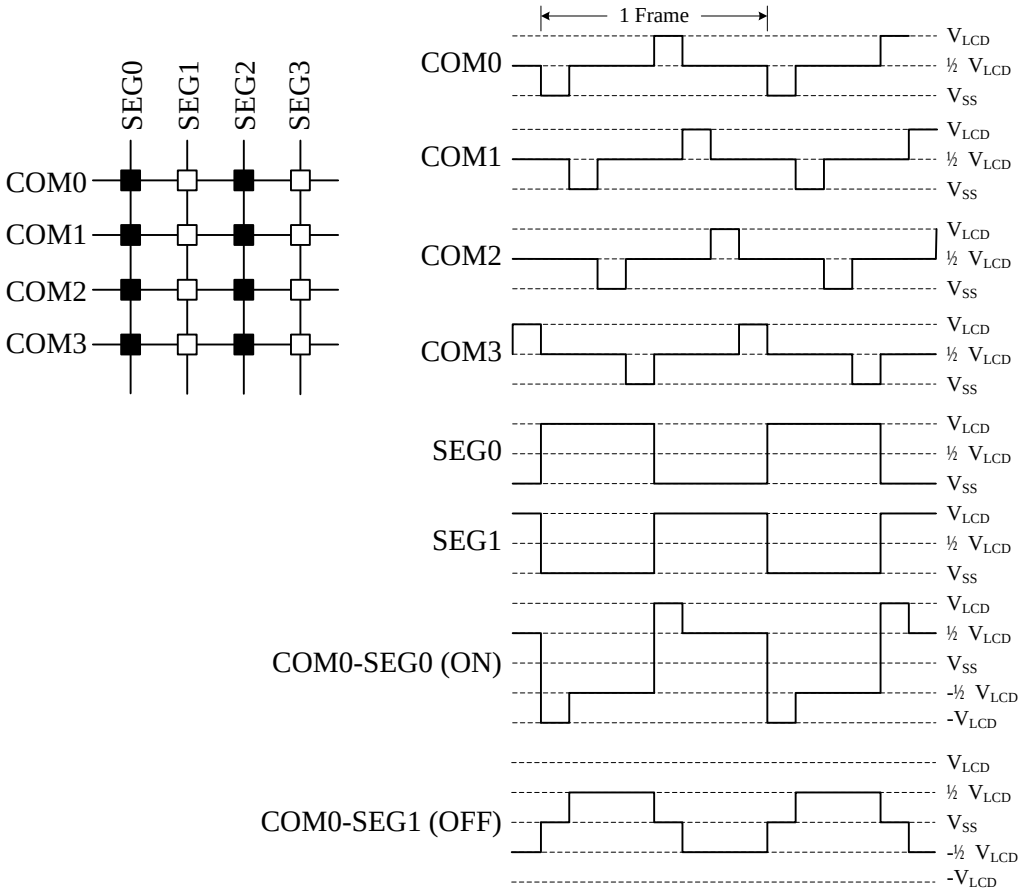
M5625/45, 1/2 Bias

1/4 Duty, 1/3 Bias Output Waveform





1/4 Duty, 1/2 Bias Output Waveform



F10	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDCTL	LCDON	LCDFRM		LCDUTY	LCDBIAS	–	LCDBV	
R/W	R/W	R/W	R/W	R/W	R/W	–	R/W	R/W
Reset	0	1	0	1	0	–	0	0

F10.7 **LCDON:** LCD driver enable
0: disable
1: enable

F10.6~5 **LCDFRM:** LCD frame rate, calculated by Slow-clock=32768Hz
00: 47Hz for 1/4 duty, 49Hz for 1/3 duty
01: 57Hz for 1/4 duty, 57Hz for 1/3 duty
10: 73Hz for 1/4 duty, 68Hz for 1/3 duty
11: 85Hz for 1/4 duty, 85Hz for 1/3 duty

F10.4 **LCDUTY:** LCD duty
0: 1/3 duty
1: 1/4 duty

F10.3 **LCDBIAS:** LCD Bias (M5620/40 must set 1/3 bias)
0: 1/2 Bias
1: 1/3 Bias

F10.1~0 **LCDBV:** LCD Brightness (only for 1/3 bias)
LCDON=1, V_{LCD}=
00: V_{BAT}*0.89 for M5620/40, V_{BAT}*2*0.89 for M5625/45
01: V_{BAT}*0.92 for M5620/40, V_{BAT}*2*0.92 for M5625/45
10: V_{BAT}*0.96 for M5620/40, V_{BAT}*2*0.96 for M5625/45
11: V_{BAT} for M5620/40, V_{BAT}*2 for M5625/45

R08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBMODL	PB3MOD		PB2MOD		PB1MOD		PB0MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

R08.7~6 **PB3MOD:** PB3 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG25 output

R08.5~4 **PB2MOD:** PB2 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG26 output

R08.3~2 **PB1MOD:** PB1 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG27 output

R08.1~0 **PB0MOD:** PB0 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG28 output

R09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDMODL	PD3MOD		PD2MOD		PD1MOD		PD0MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

R09.7~6 **PD3MOD:** PD3 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG42 output

R09.5~4 **PD2MOD:** PD2 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG43 output

R09.3~2 **PD1MOD:** PD1 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG44 output

R09.1~0 **PD0MOD:** PD0 pin mode
0x: Mode1, input without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG45 output

F0E	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LBDCTL	CMPO	CMPVS			PWRSAV	VDDS	PUMPCKS	LVRPDF
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset	–	0	0	0	0	0	0	–

F0E.1 **PUMPCKS:** LCD pump clock select (only for M5625/45)
0: Slow-clock / 4
1: Slow-clock / 8

	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
R-Plane	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
R40	SEG1	SEG1	SEG1	SEG1	SEG0	SEG0	SEG0	SEG0
R41	SEG3	SEG3	SEG3	SEG3				
R42	SEG5	SEG5	SEG5	SEG5	SEG4	SEG4	SEG4	SEG4
R43	SEG7	SEG7	SEG7	SEG7	SEG6	SEG6	SEG6	SEG6
R44	SEG9	SEG9	SEG9	SEG9	SEG8	SEG8	SEG8	SEG8
R45	SEG11	SEG11	SEG11	SEG11	SEG10	SEG10	SEG10	SEG10
R46	SEG13	SEG13	SEG13	SEG13	SEG12	SEG12	SEG12	SEG12
R47	SEG15	SEG15	SEG15	SEG15	SEG14	SEG14	SEG14	SEG14
R48	SEG17	SEG17	SEG17	SEG17	SEG16	SEG16	SEG16	SEG16
R49	SEG19	SEG19	SEG19	SEG19	SEG18	SEG18	SEG18	SEG18
R4A	SEG21	SEG21	SEG21	SEG21	SEG20	SEG20	SEG20	SEG20
R4B	SEG23	SEG23	SEG23	SEG23	SEG22	SEG22	SEG22	SEG22
R4C	SEG25	SEG25	SEG25	SEG25	SEG24	SEG24	SEG24	SEG24
R4D	SEG27	SEG27	SEG27	SEG27	SEG26	SEG26	SEG26	SEG26
R4E	SEG29	SEG29	SEG29	SEG29	SEG28	SEG28	SEG28	SEG28
R4F	SEG31	SEG31	SEG31	SEG31	SEG30	SEG30	SEG30	SEG30
R50	SEG33	SEG33	SEG33	SEG33	SEG32	SEG32	SEG32	SEG32
R51	SEG35	SEG35	SEG35	SEG35	SEG34	SEG34	SEG34	SEG34
R52	SEG37	SEG37	SEG37	SEG37	SEG36	SEG36	SEG36	SEG36
R53	SEG39	SEG39	SEG39	SEG39	SEG38	SEG38	SEG38	SEG38
R54	SEG41	SEG41	SEG41	SEG41	SEG40	SEG40	SEG40	SEG40
R55	SEG43	SEG43	SEG43	SEG43	SEG42	SEG42	SEG42	SEG42
R56	SEG45	SEG45	SEG45	SEG45	SEG44	SEG44	SEG44	SEG44

LCDRAM mapping (Do not use SEG2)

MEMORY MAP

F-Plane

Name	Address	R/W	Rst	Description
(F00) INDF				**Function related to: F-Plane R/W**
INDF	00.7~0	R/W	–	Not a physical register, addressing INDF actually point to the F-Plane register whose address is contained in the FSR register
(F01) TM0				**Function related to: Timer0**
TM0	01.7~0	R/W	0	Timer0 data
(F02) PCL				**Function related to: Program Counter**
PCL	02.7~0	R/W	0	Low-byte of Program Counter (PC[7~0])
(F03) STATUS				**Function related to: STATUS**
GB2	03.7	R/W	0	General purpose bit 2
GB1	03.6	R/W	0	General purpose bit 1
RAMBK	03.5	R/W	0	RAM Bank Selection
TO	03.4	R	0	WDT timeout flag, set by WDT timeout; cleared by POR, LVR, ‘SLEEP’ or ‘CLRWDT’ instruction
PD	03.3	R	0	Power down flag, set by ‘SLEEP’ instruction; cleared by POR, LVR or ‘CLRWDT’ instruction
Z	03.2	R/W	0	Zero flag
DC	03.1	R/W	0	Decimal Carry flag
C	03.0	R/W	0	Carry flag
(F04) FSR				**Function related to: F-Plane R/W**
GB3	04.7	R/W	0	General purpose bit 3
FSR	04.6~0	R/W	0	F-Plane File Select Register, indirect address mode pointer
(F05) PAD				**Function related to: Port A**
PAD	05.7~0	R	FF	Port A pin or “data register” state
		W		Port A output data register
(F06) PBD				**Function related to: Port B**
PBD	06.7~0	R	FF	Port B pin or “data register” state
		W		Port B output data register
(F07) PDD				**Function related to: Port D**
PDD	07.3~0	R	F	Port D pin or “data register” state
		W		Port D output data register
(F08) INTIE				**Function related to: Interrupt Enable**
PWM0IE	08.7	R/W	0	PWM0 interrupt enable 0: disable 1: enable
TM1IE	08.6	R/W	0	Timer1 interrupt enable 0: disable 1: enable
RFCIE	08.5	R/W	0	RFC interrupt enable 0: disable 1: enable
TM0IE	08.4	R/W	0	Timer0 interrupt enable 0: disable 1: enable
T2IE	08.3	R/W	0	Timer2 interrupt enable 0: disable 1: enable
INT2IE	08.2	R/W	0	INT2 pin (PA7) interrupt enable 0: disable 1: enable

INT1IE	08.1	R/W	0	INT1 pin (PB4) interrupt enable 1: enable 0: disable
INT0IE	08.0	R/W	0	INT0 pin (PA0) interrupt enable 0: disable 1: enable

Name	Address	R/W	Rst	Description
(F09) INTIF				**Function related to: Interrupt Flag**
PWM0IF	09.7	R	0	PWM0 interrupt event pending flag, Set by H/W while PWM0 period completes
		W		writing 0x7F to INTIF to clear this flag
TM1IF	09.6	R	0	Tmer1 interrupt event pending flag, Set by H/W while Timer1 overflows
		W		writing 0xBF to INTIF to clear this flag
RFCIF	09.5	R	0	RFC counter overflow interrupt event pending flag, Set by H/W while RFC counter overflows
		W		writing 0xDF to INTIF to clear this flag
TM0IF	09.4	R	0	Timer0 interrupt event pending flag, set by H/W while Timer0 overflows
		W		writing 0xEF to INTIF to clear this flag
T2IF	09.3	R	0	Timer2 interrupt event pending flag, set by H/W while WKT time out
		W		writing 0xF7 to INTIF to clear this flag
INT2IF	09.2	R	0	INT2 (PA7) interrupt event pending flag, set by H/W at INT2 pin's rising/falling edge
		W		writing 0xFB to INTIF to clear this flag
INT1IF	09.1	R	0	INT1 (PB4) interrupt event pending flag, set by H/W at INT1 pin's rising/falling edge
		W		writing 0xFD to INTIF to clear this flag
INT0IF	09.0	R	0	INT0 (PA0) interrupt event pending flag, set by H/W at INT0 pin's rising/falling edge
		W		writing 0xFE to INTIF to clear this flag
(F0A) PCH				**Function related to: PROGRAM COUNT**
PCH	0A.3~0	R	0	4 MSBs of Program Counter (PC[11:8])
(F0B) CLKCTL				**Function related to: System Clock (Fsys)**
SCKTYPE	0B.7	R/W	0	Slow-clock Type 0: SIRC 1: SXT
SXTGAIN	0B.6~5	R/W	11	32768 SXT oscillator gain 0: lowest gain ... 3: highest gain
SLOWSTP	0B.4	R/W	0	Slow-clock Stop control 0: Slow-clock run 1: Slow-clock stop
FASTSTP	0B.3	R/W	1	Fast-clock Stop control 0: Fast-clock run 1: Fast-clock stop
CPUCKS	0B.2	R/W	0	System clock (Fsys) source selection 0: Slow-clock 1: Fast-clock
CPUPSC	0B.1~0	R/W	11	System clock source prescaler. Clock source is divided by 00: /8 01: /4 10: /2 11: /1
(F0C) MF0C				**Function related to: TM0/TM1/T2/Interrupt**
T2CLR	0C.7	R/W	0	T2 counter clear 0: T2 is counting 1: T2 is cleared, this bit is auto cleared by H/W
T2CKS	0C.6	R/W	0	T2 clock source selection 0: Slow-clock 1: Fsys/128

TM0STP	0C.5	R/W	0	Timer0 counter stop 0: Timer0 running 1: Timer0 stop
TM1STP	0C.4	R/W	0	Timer1 counter stop 0: Timer1 running 1: Timer1 stop
TM1CLR	0C.3	R/W	0	Timer1 clear and stop 0: Timer1 run 1: Timer1 clear and stop
INT2EDG	0C.2	R/W	0	INT2 pin (PA7) interrupt trigger edge select 0: falling edge 1: rising edge
INT1EDG	0C.1	R/W	0	INT1 pin (PB4) interrupt trigger edge select 0: falling edge 1: rising edge
INT0EDG	0C.0	R/W	0	INT0 pin (PA0) interrupt trigger edge select 0: falling edge 1: rising edge

Name	Address	R/W	Rst	Description
(F0D) PWM0D				**Function related to: PWM0**
PWM0D	0D.7~0	R/W	80h	PWM0 duty, 0=0 PWM0CLK, 80h=128 PWM0CLK, FFh=255 PWM0CLK
(F0E) LBDCTL				**Function related to: LBD/LCD**
CMPO	0E.7	R	–	LBD (low battery detect) result Compare result of bandgap voltage and VBAT voltage divider. CMPO=0 means the VBAT divided voltage is lower than bandgap voltage.
CMPVS	0E.6~4	R/W	0	Select V_{BAT}/V_{LCD} resistor divider for Comparator input to compare with the 1.2V Bandgap reference voltage. M5620/40: 000: Comparator and Bandgap Disable 001: detect if V_{BAT}>2.4V 010: detect if V_{BAT}>2.5V; 011: detect if V_{BAT}>2.6V; 100: detect if V_{BAT}>2.7V; 101: detect if V_{BAT}>2.8V; 110: detect if V_{BAT}>2.9V; 111: detect if V_{BAT}>3.0V; M5625/45: 000: Comparator and Bandgap Disable 001: detect if V_{BAT}>1.20V 010:; detect if V_{BAT}>1.25V 011: detect if V_{BAT}>1.30V 100: detect if V_{BAT}>1.35V 101: detect if V_{BAT}>1.40V 110: detect if V_{BAT}>1.45V 111: detect if V_{BAT}>1.50V
PWRSAV	0E.3	R/W	0	Power saving control. (only for M5620/40) 0: Disable, $V_{DD}=V_{BAT}$ 1: Enable, $V_{DD}=V_{LCD}$*0.54 or V_{LCD}*0.625
VDDVS	0E.2	R/W	0	V_{DD} voltage selection (only for M5620/40) 0: V_{LCD}*0.54 1: V_{LCD}*0.625
PUMPCKS	0E.1	R/W	0	LCD pump clock select (only for M5625/45) 0: Slow-clock / 4 1: Slow-clock / 8
LVRPDF	0E.0	R	–	LVR Power Down Flag

(F0F) RFCTL				Function related to: RFC
RFCLR	0F.7	R/W	1	Clear RFC counter 0: RFC run 1: RFC clear
T1STPRFC	0F.6	R/W	0	Timer1 overflow toggle signal (TM1TGL) to stop RFC counter 0: disable 1: enable
T0STPRFC	0F.5	R/W	0	Timer0 overflow toggle signal (TM0TGL) to stop RFC counter 0: disable 1: enable
RFCSTP	0F.4	R/W	1	S/W stop RFC counter and oscillator 0: RFC run 1: RFC stop
SLOWPSC	0F.3~2	R/W	11	Slow clock divider for Timer0 00: /64 01: /16 10: /4 11: /1
RFCHS	0F.1~0	R/W	0	Select RFC oscillator channel 00: RFC0R (PA2) 01: RFC1R (PA0) 10: RFC2R (PA1) 11: RFC3R (PB7)
(F10) LCDCTL				**Function related to: LCD**
LCDON	10.7	R/W	0	LCD driver enable 0: disable 1: enable
LCDFRM	10.6~5	R/W	10	LCD frame rate, calculated by Slow-clock=32768Hz 00: 47Hz for 1/4 duty, 49Hz for 1/3 duty 01: 57Hz for 1/4 duty, 57Hz for 1/3 duty 10: 73Hz for 1/4 duty, 68Hz for 1/3 duty 11: 85Hz for 1/4 duty, 85Hz for 1/3 duty
LCDUTY	10.4	R/W	1	LCD duty 0: 1/3 duty 1: 1/4 duty
LCDBIAS	10.3	R/W	0	LCD bias (M5620/40 must set 1/3 bias) 0: 1/2 bias 1: 1/3 bias
LCDBV	10.1~0	R/W	0	LCD Brightness, V_{LCD} voltage level control. (only for 1/3 bias) LCDON=1, V_{LCD}= 00: V_{BAT}*0.89 for M5620/40, V_{BAT}*2*0.89 for M5625/45 01: V_{BAT}*0.92 for M5620/40, V_{BAT}*2*0.92 for M5625/45 10: V_{BAT}*0.96 for M5620/40, V_{BAT}*2*0.96 for M5625/45 11: V_{BAT} for M5620/40, V_{BAT}*2 for M5625/45
(F11) RFCNTH				**Function related to: RFC**
RFCNTH	11.7~0	R	0	RFC counter high byte, RFCNT[15:8]
(F12) RFCNTL				**Function related to: RFC**
RFCNTL	12.7~0	R	0	RFC counter low byte, RFCNT[7:0]
(F13) PWM1D				**Function related to: PWM1**
PWM1D	13.7~0	R/W	80	PWM1 duty
(F14) TM1				**Function related to: Timer1**
TM1	14.7~0	R/W	0	Timer1 data
(F15) PWMCLR				**Function related to: PWM0/PWM1**
PWM1CLR	15.1	R/W	0	PWM1 clear and hold 0: PWM1 running 1: PWM1 clear and hold
PWM0CLR	15.0	R/W	0	PWM0 clear and hold 0: PWM0 running 1: PWM0 clear and hold
(F1C) RSR				**Function related to: R-Plane R/W**
RSR	1C.7~0	R/W	0	R-Plane file select register, indirect address mode pointer
(F1D) DPL				**Function related to: Table Read**
DPL	1D.7~0	R/W	0	Table read low address, data ROM pointer (DPTR[7:0])
(F1E) DPH				**Function related to: Table Read**
DPH	1E.3~0	R/W	0	Table read high address, data ROM pointer (DPTR[11:8])

User Data RAM				
FRAM	20~2F	R/W	–	F-Plane RAM Common area (16 Bytes)
	30~7F	R/W	–	F-Plane RAM Bank0 area (RAMBK=0, 80 Bytes)
	30~7F	R/W	–	F-Plane RAM Bank1 area (RAMBK=1, 80 Bytes)

R-Plane

Name	Address	R/W	Rst	Description
(R00) INDR				**Function related to: R-Plane R/W**
INDR	00.7~0	R/W	–	Not a physical register, addressing INDR actually point to the R-Plane register whose address is contained in the RSR register
(R01) TM0RLD				**Function related to: TM0**
TM0RLD	01.7~0	R/W	0	Timer0 reload Data
(R02) TM0CTL				**Function related to: TM0**
TM0CM	02.7	R/W	0	Timer0 Capture mode 0: Timer mode or Counter mode 1: Capture mode
T0ISRC	02.6	R/W	1	Timer0 Counter mode source 0: TM0CKI pin (PB4) 1: Slow-clock div 1/4/16/64 sets by SLOWPSC(F0F.3~2)
TM0EDGE	02.5	R/W	0	if TM0EDG=1, TM0CKI/CAPT input data will be reversed Timer0 prescaler counting edge for Counter mode 0: Rising edge 1: Falling edge Timer0 capture level for Capture mode 0: High level capture 1: Low level capture Timer1 capture edge for Capture mode 0: Falling edge capture 1: Rising edge capture
TM0CKS	02.4	R/W	0	Timer0 mode select 0 : Timer mode (Fsys/2) 1 : Counter mode (SCLK divided 1/4/16/64 or T0CKI(PB4))
TM0PSC	02.3~0	R/W	0	Timer0 clock source prescaler. Clock source is divided by 0000: Fsys/2 0101: Fsys/64 0001: Fsys/4 0110: Fsys/128 0010: Fsys/8 0111: Fsys/256 0011: Fsys/16 1xxx: Fsys/512 0100: Fsys/32
(R03) PWRDN				**Function related to: Power Down**
PWRDN	03	W	–	Write this register (=SLEEP instruction) to enter IDLE or STOP Mode
(R04) WDTCLR				**Function related to: WDT**
WDTCLR	04	W	–	Write this register to clear WDT (=CLRWDT instruction)
(R05) PAMODH				**Function related to: Port A**
PA7MOD	05.6	R/W	0	0: Mode0, PA7 is open-drain I/O with internal pull-up 1: Mode1, PA7 is open-drain I/O without internal pull-up
PA6MOD	05.5~4	R/W	01	00: Mode0, PA6 is open-drain I/O with internal pull-up 01: Mode1, PA6 is open-drain I/O without internal pull-up 10: Mode2, PA6 is CMOS push-pull output 11: Mode3, PA6 is PWM0P CMOS push pull output
PA5MOD	05.3~2	R/W	01	00: Mode0, PA5 is open-drain I/O with internal pull-up 01: Mode1, PA5 is open-drain I/O without internal pull-up 10: Mode2, PA5 is CMOS push-pull output 11: Mode3, PA5 is RFCX input
PA4MOD	05.1~0	R/W	01	00: Mode0, PA4 is open-drain I/O with internal pull-up 01: Mode1, PA4 is open-drain I/O without internal pull-up 10: Mode2, PA4 is CMOS push-pull output

(R06) PAMODL				Function related to: Port A
PA3MOD	06.7~6	R/W	01	00: Mode0, PA3 is open-drain I/O with internal pull-up 01: Mode1, PA3 is open-drain I/O without internal pull-up 10: Mode2, PA3 is CMOS push-pull output
PA2MOD	06.5~4	R/W	01	00: Mode0, PA2 is open-drain I/O with internal pull-up 01: Mode1, PA2 is open-drain I/O without internal pull-up 10: Mode2, PA2 is CMOS push-pull output 11: Mode3, PA2 is RFC0R output
PA1MOD	06.3~2	R/W	01	00: Mode0, PA1 is open-drain I/O with internal pull-up 01: Mode1, PA1 is open-drain I/O without internal pull-up 10: Mode2, PA1 is CMOS push-pull output 11: Mode3, PA1 is RFC2R output
PA0MOD	06.1~0	R/W	01	00: Mode0, PA0 is open-drain I/O with internal pull-up 01: Mode1, PA0 is open-drain I/O without internal pull-up 10: Mode2, PA0 is CMOS push-pull output 11: Mode3, PA0 is RFC1R output

Name	Address	R/W	Rst	Description
(R07) PBMODH				Function related to: Port B
PB7MOD	07.7~6	R/W	01	00: Mode0, PB7 is open-drain I/O with internal pull-up 01: Mode1, PB7 is open-drain I/O without internal pull-up 10: Mode2, PB7 is CMOS push-pull output 11: Mode3, PB7 is RFC3R output
PB6MOD	07.5~4	R/W	01	00: Mode0, PB6 is open-drain I/O with internal pull-up 01: Mode1, PB6 is open-drain I/O without internal pull-up 10: Mode2, PB6 is CMOS push-pull output 11: Mode3, PB6 is TCOUT output
PB5MOD	07.3~2	R/W	01	00: Mode0, PB5 is open-drain I/O with internal pull-up 01: Mode1, PB5 is open-drain I/O without internal pull-up 10: Mode2, PB5 is CMOS push-pull output 11: Mode3, PB5 is PWM1O output
PB4MOD	07.1~0	R/W	01	00: Mode0, PB4 is open-drain I/O with internal pull-up 01: Mode1, PB4 is open-drain I/O without internal pull-up 10: Mode2, PB4 is CMOS push-pull output
(R08) PBMODL				Function related to: Port B
PB3MOD	08.7~6	R/W	01	0x: Mode1, PB3 is input without internal pull-up 10: Mode2, PB3 is CMOS push-pull output 11: Mode3, PB3 is LCD SEG25 output
PB2MOD	08.5~4	R/W	01	0x: Mode1, PB2 is input without internal pull-up 10: Mode2, PB2 is CMOS push-pull output 11: Mode3, PB2 is LCD SEG26 output
PB1MOD	08.3~2	R/W	01	0x: Mode1, PB1 is input without internal pull-up 10: Mode2, PB1 is CMOS push-pull output 11: Mode3, PB1 is LCD SEG27 output
PB0MOD	08.1~0	R/W	01	0x: Mode1, PB0 is input without internal pull-up 10: Mode2, PB0 is CMOS push-pull output 11: Mode3, PB0 is LCD SEG28 output
(R09) PDMODL				Function related to: Port D
PD3MOD	09.7~6	R/W	01	0x: Mode1, PD3 is input without internal pull-up 10: Mode2, PD3 is CMOS push-pull output 11: Mode3, PD3 is LCD SEG42 output
PD2MOD	09.5~4	R/W	01	0x: Mode1, PD2 is input without internal pull-up 10: Mode2, PD2 is CMOS push-pull output 11: Mode3, PD2 is LCD SEG43 output
PD1MOD	09.3~2	R/W	01	0x: Mode1, PD1 is input without internal pull-up

				10: Mode2, PD1 is CMOS push-pull output 11: Mode3, PD1 is LCD SEG44 output
PD0MOD	09.1~0	R/W	01	0x: Mode1, PD0 is input without internal pull-up 10: Mode2, PD0 is CMOS push-pull output 11: Mode3, PD0 is LCD SEG45 output
(R0A) PWM0CTL				**Function related to: PWM0/T2/WDT**
PWM0CKS	0A.7	R/W	1	PWM0 clock source select 0: Slow-clock 1: Fast-clock
T2PSC	0A.6~5	R/W	0	T2 prescaler. T2 interrupt is T2 clock divided by 00: (32768*60) 01: 32768 10: 16384 11: 4096
PWM0PSC	0A.4~2	R/W	0	PWM0 clock prescaler 000: PWM0 clock is Slow/Fast clock divided by 128 001: PWM0 clock is Slow/Fast clock divided by 64 010: PWM0 clock is Slow/Fast clock divided by 32 011: PWM0 clock is Slow/Fast clock divided by 16 100: PWM0 clock is Slow/Fast clock divided by 8 101: PWM0 clock is Slow/Fast clock divided by 4 110: PWM0 clock is Slow/Fast clock divided by 2 111: PWM0 clock is Slow/Fast clock divided by 1
PWM0NOE	0A.1	R/W	0	PWM0N output to PA1 pin 0: disable 1: enable
WDTPSC	0A.0	R/W	0	WDT Prescaler, 0: fsys/65536 1:fsys/32768 1.4sec/0.7sec @VDD=3V (Fsys = SIRC) 2.0sec/1.0sec @VDD=1.5V (Fsys = SIRC)
(R0B) PWM0PRD				**Function related to: PWM0**
PWM0PRD	0B.7~0	R/W	FF	PWM0 period, FFh=256 PWM0CLK, 7Fh=128 PWM0CLK
(R0C) PWM1CTL				**Function related to: PWM1**
PWM1CKS	0C.7	R/W	1	PWM1 clock source select 0: Slow-clock 1: Fast-clock
PWM1PSC	0C.4~2	R/W	0	PWM1 clock prescaler 000: PWM1 clock is Slow/Fast clock divided by 128 001: PWM1 clock is Slow/Fast clock divided by 64 010: PWM1 clock is Slow/Fast clock divided by 32 011: PWM1 clock is Slow/Fast clock divided by 16 100: PWM1 clock is Slow/Fast clock divided by 8 101: PWM1 clock is Slow/Fast clock divided by 4 110: PWM1 clock is Slow/Fast clock divided by 2 111: PWM1 clock is Slow/Fast clock divided by 1
(R0D) PWM1PRD				**Function related to: PWM1**
PWM1PRD	0D.7~0	R/W	FF	PWM1 period, FFh=256 PWM1CLK, 7Fh=128 PWM1CLK
(R10) TM1RLD				**Function related to: TM1**
TM1RLD	10.7~0	R/W	0	Timer1 reload Data
(R11) TM1CTL				**Function related to: TM1**
TM1CM	11.4	R/W	0	Timer1 Capture mode 0: Timer mode 1: Capture mode
TM1PSC	11.3~0	R/W	0	Timer1 clock source prescaler. Clock source is divided by

				0000: Fsys/2 0101: Fsys/64 0001: Fsys/4 0110: Fsys/128 0010: Fsys/8 0111: Fsys/256 0011: Fsys/16 1xxx: Fsys/512 0100: Fsys/32
(R12) PBWKEN				**Function related to: Port B/Wake Up**
PBWKEN	12.7~0	R/W	0	PB7~PB0 low level wakeup 0: disable 1: enable
(R1F) LVROFF				**Function related to: LVR**
LVROFF	1F.7~0	W	–	Write this register with 0x37 to force LVR disable
	1F.0	R	0	Flag indicates LVR is forced to disable or not 1: LVR is forced to disable
User Data RAM				
LCDRAM	40~4E	R/W	–	LCD RAM area (15 Bytes)
LCDRAM	4F~56	R/W	–	LCD RAM area (8 Bytes) (only for M5640/45)
RRAM	60~FF	R/W	–	R-Plane RAM (160 Bytes) (only for M5640/45)

INSTRUCTION SET

Each instruction is a 14-bit word divided into an Op Code, which specifies the instruction type, and one or more operands, which further specify the operation of the instruction. The instructions can be categorized as byte-oriented, bit-oriented and literal operations list in the following table.

For byte-oriented instructions, “f” or “r” represents the address designator and “d” represents the destination designator. The address designator is used to specify which address in Program memory is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If “d” is “0”, the result is placed in the W register. If “d” is “1”, the result is placed in the address specified in the instruction.

For bit-oriented instructions, “b” represents a bit field designator, which selects the number of the bit affected by the operation, while “f” represents the address designator. For literal operations, “k” represents the literal or constant value.

Field/Legend	Description
f	F-Plane Register File Address
r	R-Plane Register File Address
b	Bit address
k	Literal. Constant data or label
d	Destination selection field, 0: Working register, 1: Register file
W	Working Register
Z	Zero Flag
C	Carry Flag or/Borrow Flag
DC	Decimal Carry Flag or Decimal/Borrow Flag
PC	Program Counter
TOS	Top Of Stack
GIE	Global Interrupt Enable Flag (i-Flag)
[]	Option Field
( )	Contents
.	Bit Field
B	Before
A	After
←	Assign direction

Mnemonic		Op Code	Cycle	Flag Affect	Description
Byte-Oriented File Register Instruction					
ADDWF	f, d	00 0111 dfff ffff	1	C, DC, Z	Add W and "f"
ANDWF	f, d	00 0101 dfff ffff	1	Z	AND W with "f"
CLRF	F	00 0001 1fff ffff	1	Z	Clear "f"
CLRW		00 0001 0100 0000	1	Z	Clear W
COMF	f, d	00 1001 dfff ffff	1	Z	Complement "f"
DECF	f, d	00 0011 dfff ffff	1	Z	Decrement "f"
DECFSZ	f, d	00 1011 dfff ffff	1 or 2	-	Decrement "f", skip if zero
INCF	f, d	00 1010 dfff ffff	1	Z	Increment "f"
INCFSZ	f, d	00 1111 dfff ffff	1 or 2	-	Increment "f", skip if zero
IORWF	f, d	00 0100 dfff ffff	1	Z	OR W with "f"
MOVFW	f	00 1000 0fff ffff	1	-	Move "f" to W
MOVWF	f	00 0000 1fff ffff	1	-	Move W to "f"
MOVWR	r	01 1110 00rr rrrr	1	-	Move W to "r"
MOVRW	r	01 1111 00rr rrrr	1	-	Move "r" to W
RLF	f, d	00 1101 dfff ffff	1	C	Rotate left "f" through carry
RRF	f, d	00 1100 dfff ffff	1	C	Rotate right "f" through carry
SUBWF	f, d	00 0010 dfff ffff	1	C, DC, Z	Subtract W from "f"
SWAPF	f, d	00 1110 dfff ffff	1	-	Swap nibbles in "f"
TESTZ	f	00 1000 1fff ffff	1	Z	Test if "f" is zero
XORWF	f, d	00 0110 dfff ffff	1	Z	XOR W with "f"
Bit-Oriented File Register Instruction					
BCF	f, b	01 000b bbff ffff	1	-	Clear "b" bit of "f"
BSF	f, b	01 001b bbff ffff	1	-	Set "b" bit of "f"
BTFSC	f, b	01 010b bbff ffff	1 or 2	-	Test "b" bit of "f", skip if clear
BTFSS	f, b	01 011b bbff ffff	1 or 2	-	Test "b" bit of "f", skip if set
Literal and Control Instruction					
ADDLW	k	01 1100 kkkk kkkk	1	C, DC, Z	Add Literal "k" and W
ANDLW	k	01 1011 kkkk kkkk	1	Z	AND Literal "k" with W
CALL	k	10 kkkk kkkk kkkk	2	-	Call subroutine "k"
CLRWDT		01 1110 0000 0100	1	TO, PD	Clear Watch Dog Timer
GOTO	k	11 kkkk kkkk kkkk	2	-	Jump to branch "k"
IORLW	k	01 1010 kkkk kkkk	1	Z	OR Literal "k" with W
MOVLW	k	01 1001 kkkk kkkK	1	-	Move Literal "k" to W
NOP		00 0000 0000 0000	1	-	No operation
RET		00 0000 0100 0000	2	-	Return from subroutine
RETI		00 0000 0110 0000	2	-	Return from interrupt
RETLW	k	01 1000 kkkk kkkK	2	-	Return with Literal in W
SLEEP		01 1110 0000 0011	1	TO, PD	Go into Power-down mode, Clock oscillation stops
TABRH		00 0000 0101 1000	2	-	Lookup ROM high data to W
TABRL		00 0000 0101 0000	2	-	Lookup ROM low data to W
XORLW	k	01 1101 kkkk kkkk	1	Z	XOR Literal "k" with W

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (T_A =25℃)

Parameter	Rating	Unit
Supply voltage	Vss-0.3 ~ Vss+3.6	V
Operating voltage (M5620/40)	LVR ~ Vss+3.6	
Operating voltage (M5625/45)	LVRC ~ Vss+1.8	
Input voltage	V_{SS} -0.3 ~ V_{BAT} +0.3	
Output voltage	V_{SS} -0.3 ~ V_{BAT} +0.3	
Output current high per 1 pin / all pins	–20 / –50	mA
Output current low per 1 pin / all pins	+30 / +100	
Operating temperature	-40 ~ +85	℃
Storage temperature	-65 ~ +150	

2. DC Characteristics (T_A =25℃)

Parameter	Sym	Conditions		Min	Typ	Max	Unit
Input High Voltage	V_{IH}	M5620/40: V_{BAT}=3V M5625/45: V_{BAT}=1.5V		0.7V_{BAT}	–	–	V
Input Low Voltage	V_{IL}			–	–	0.2V_{BAT}	
I/O Source/Sink Current (except PA7)	I_{OH}	V_{OH}=2.7V	M5620/40 V_{BAT}=3V	–	5	–	mA
	I_{OL}	V_{OL}=0.3V		–	15	–	
I/O Source/Sink Current (except PA7)	I_{OH}	V_{OH}=1.35V	M5625/45 V_{BAT}=1.5V	–	1.2	–	
	I_{OL}	V_{OL}=0.15V		–	4.5	–	
I/O Source/Sink Current (PA7)	I_{OH}	V_{OH}=2.7V	M5620/40 V_{BAT}=3V	–	N/A	–	
	I_{OL}	V_{OL}=0.3V		–	9.6	–	
I/O Source/Sink Current (PA7)	I_{OH}	V_{OH}=1.35V	M5625/45 V_{BAT}=1.5V	–	N/A	–	
	I_{OL}	V_{OL}=0.15V		–	2.7	–	
Input leakage current (pin high)	I_{ILH}	all Input	V_{IN}=V_{BAT}	–	–	1	uA
Input leakage current (pin low)	I_{ILL}		Vin=0V	–	–	–1	
Power Supply Current	I_{BAT}	FRC, 3.8MHz	M5620/40 V_{BAT}=3V V_{DD}=3V	–	523	–	uA
		SRC, 45KHz		–	10	–	
		SXT, 32KHz			10		
		FRC, 1.3MHz	M5620/40 V_{BAT}=3V V_{DD}=1.5V	–	90	–	
		SRC, 32KHz		–	5	–	
		SXT, 32KHz		–	5	–	
		FRC, 1.3MHz	M5625/45 V_{BAT}=1.5V	–	97	–	
		SRC, 32KHz		–	5	–	
		SXT, 32KHz		–	5	–	
Timepiece Current CPU Off, LCD On, 32K Crystal oscillating	I_{BAT}	M5620/40, V_{BAT}=3V, V_{DD}=3V			5		uA
		M5620/40, V_{BAT}=3V, V_{DD}=1.5V		–	3	–	
		M5625/45, V_{BAT}=1.5V, 1/3 LCD bias		–	4	–	

		M5625/45, V_{BAT}=1.5V, 1/2 LCD bias	–	2	–	
Stop Mode Current	I_{BAT}	M5620/40, V_{BAT}=3V	–	0.5	–	uA
		M5625/45, V_{BAT}=1.5V, 1/3 LCD bias	–	0.2	–	
		M5625/45, V_{BAT}=1.5V, 1/2 LCD bias	–	0.1	–	
Pull-Up Resistor	PA0~PA6, PB4~PB7	M5620/40, V_{BAT}=3V	–	50	–	KΩ
		M5625/45, V_{BAT}=1.5V	–	400	–	
	PB0~PB3, PD0~PD3	–	–	N/A	–	
	PA7	M5620/40, V_{BAT}=3V	–	50	–	
		M5625/45, V_{BAT}=1.5V	–	400	–	

3. Clock Timing (T_A = -40°C to +85°C)

Parameter	Sym	Conditions	Min	Typ	Max	Unit
FRC Clock Frequency	F_{FRC}	V_{DD}=3V	–	3.9	–	MHz
		V_{DD}=1.5V	–	1.3	–	
SRC Clock Frequency	F_{SRC}	V_{DD}=3V	–	45	–	KHz
		V_{DD}=1.5V	–	30	–	
		V_{DD}=1.3V	–	20	–	

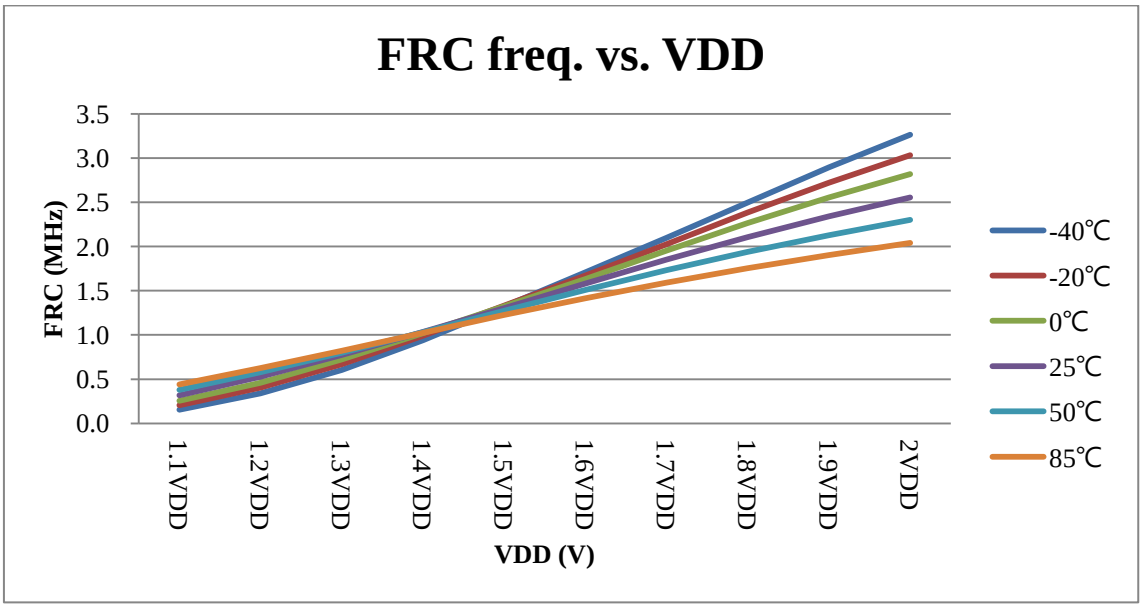
4. BandGap Reference Voltage

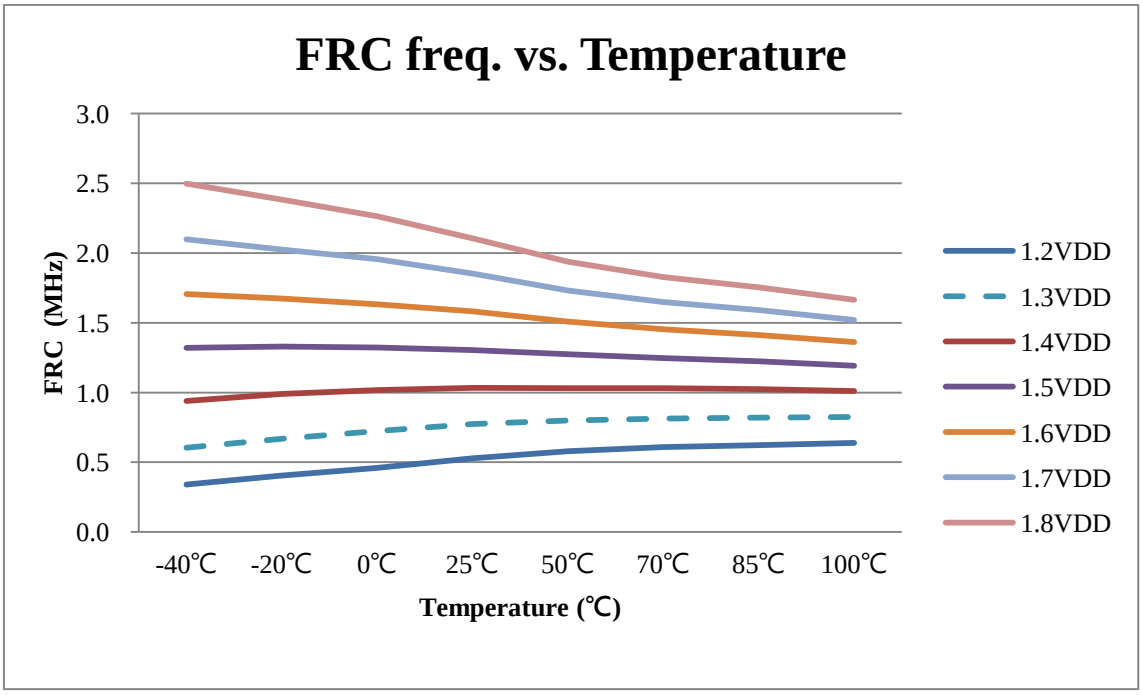
Parameter	Sym	Conditions	Min	Typ	Max	Unit
BandGap Voltage	V_{BG}	V_{BAT}=3V, 25℃	1.14	1.2	1.26	V
		V_{BAT}=3V, –40℃~85℃	1.12	1.2	1.28	

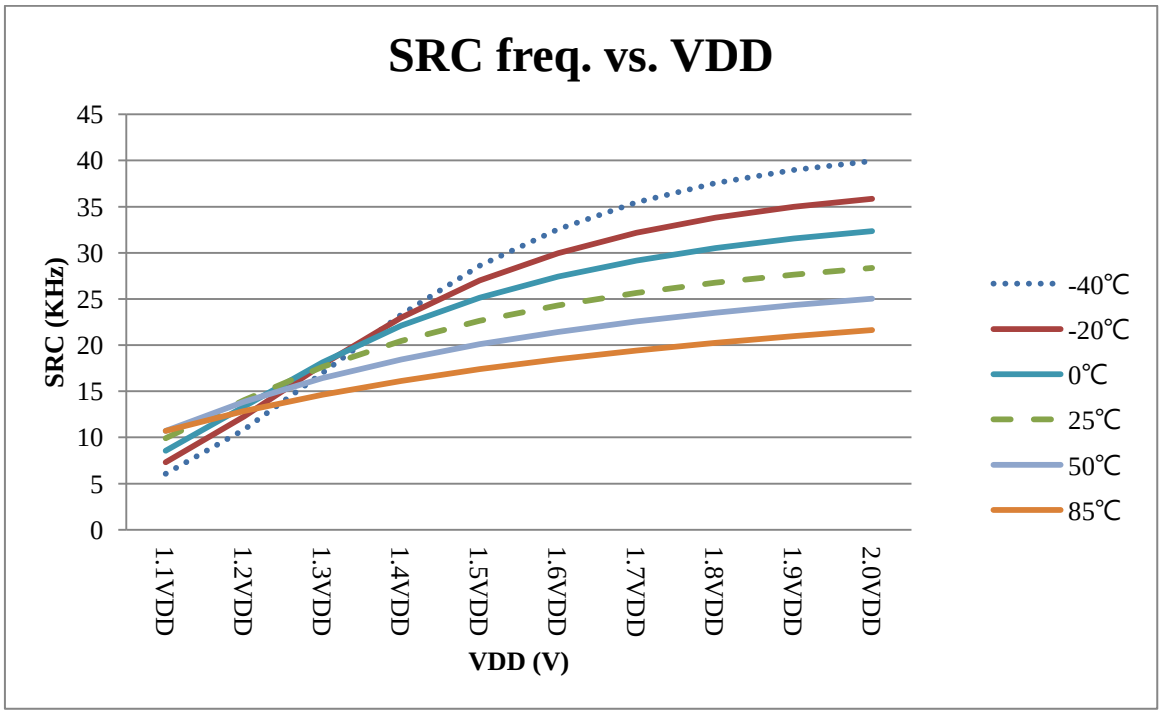
5. Low Battery Detector(LBD) Delay Time

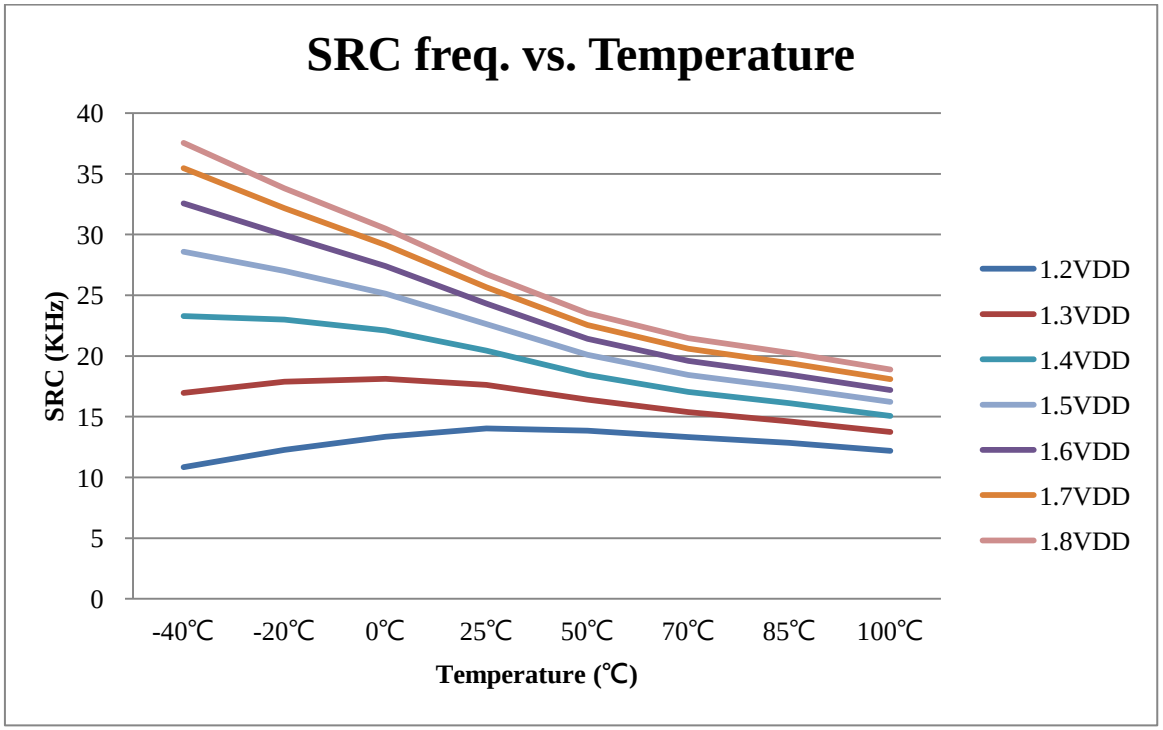
Parameter	Sym	Conditions	Min	Typ	Max	Unit
LBD delay time	T_{LBD}	-	-	20	-	us

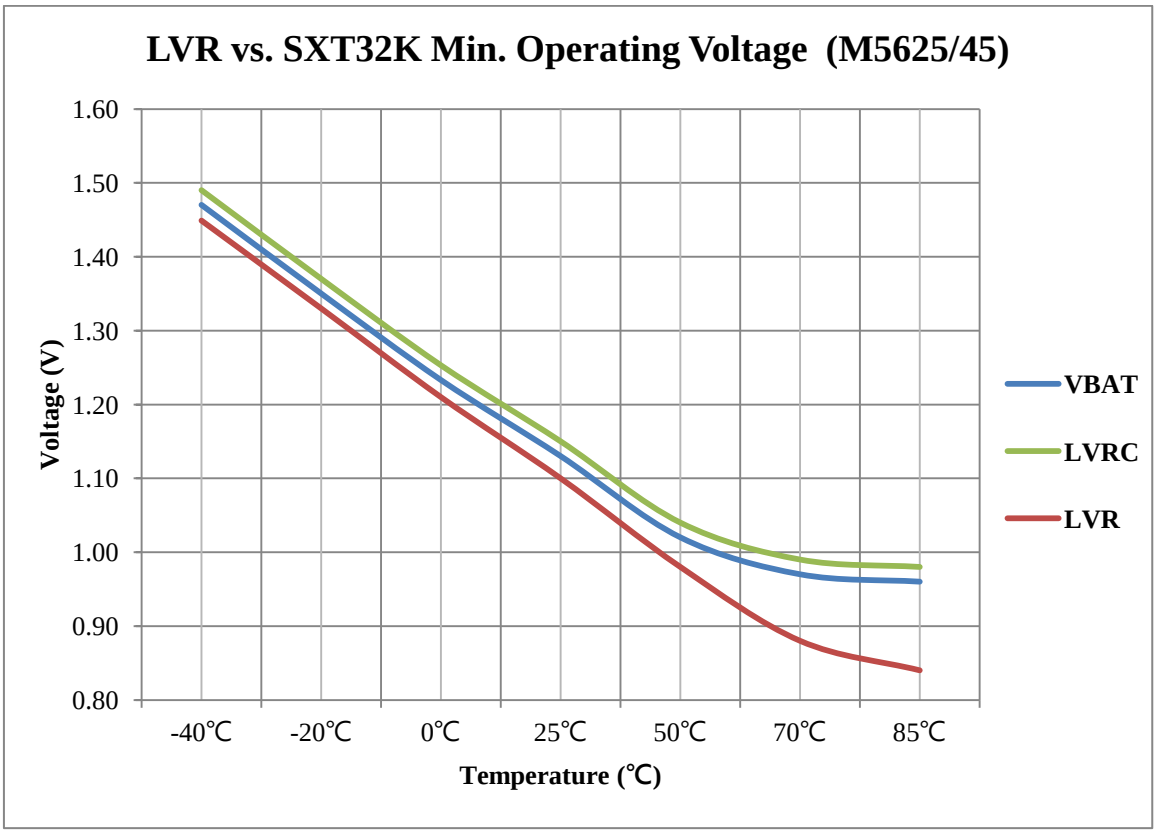
Characteristic Graphs





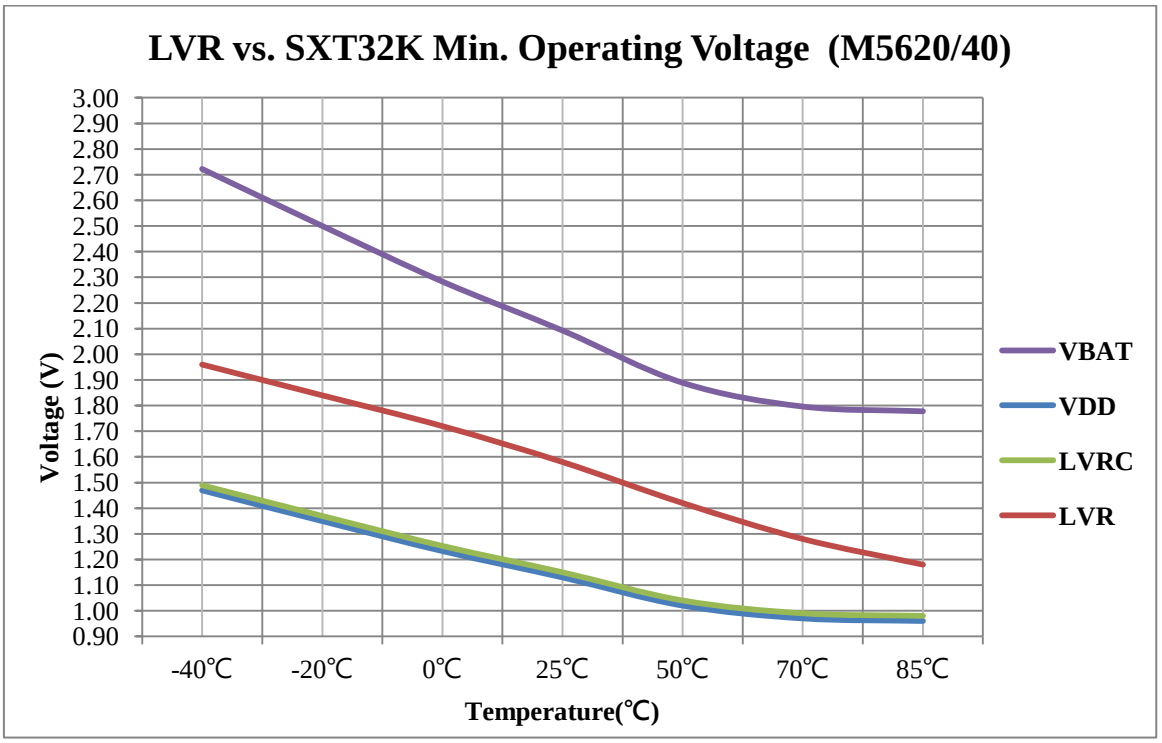

SRC freq. vs. VDD
SRC (KHz)
45
40
35
30
25
20
15
10
5
0
1.1VDD
1.2VDD
1.3VDD
1.4VDD
1.5VDD
1.6VDD
1.7VDD
1.8VDD
1.9VDD
2.0VDD
VDD (V)
-40℃
-20℃
0℃
25℃
50℃
85℃


SRC freq. vs. Temperature
SRC (KHz)
40
35
30
25
20
15
10
5
0
-40℃
-20℃
0℃
25℃
50℃
70℃
85℃
100℃
Temperature (℃)
1.2VDD
1.3VDD
1.4VDD
1.5VDD
1.6VDD
1.7VDD
1.8VDD



LVR vs. SXT32K Min. Operating Voltage (M5625/45)

Note:
1. LVRC (ROM Error Reset, follow minimum operating voltage) always enable
2. LVR (Power-on Reset or Low Voltage Reset) can disable by LVROFF register.
3. Power up VBAT must exceed the LVR (**1.1**V@25C) and then set LVROFF=0x37 (disable LVR) to obtain lowest VBAT operating.



LVR vs. SXT32K Min. Operating Voltage (M5620/40)

Note:

1. LVRC (ROM Error Reset, follow minimum operating voltage) always enable
2. LVR (Power-on Reset or Low Voltage Reset) can disable by LVROFF register.
3. Power up VBAT must exceed the LVR (**1.6V**@25C) and then set LVROFF=0x37 (disable LVR) to obtain lowest VBAT operating.
4. VDD (Internal voltage of the chip) =V_{LCD}*0.54 (if VDDVS=0 & PWRSAV=1)

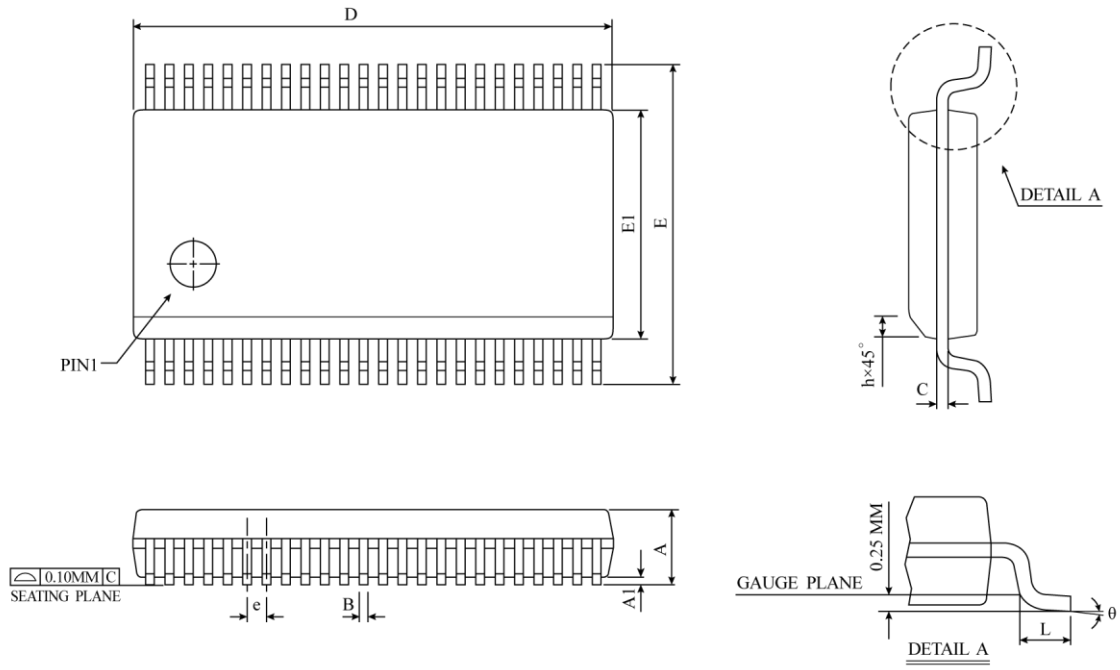
PACKAGING INFORMATION

Please note that the package information provided is for reference only. Since this information is frequently updated, users can contact Sales to consult the latest package information and stocks.

The ordering information:

Ordering number	Package
TM57M5620-MTP	Wafer / Dice blank chip
TM57M5620-COD	Wafer / Dice with code
TM57M5620-MTP-37	SSOP 48 pin (300mil)
TM57M5625-MTP	Wafer / Dice blank chip
TM57M5625-COD	Wafer / Dice with code
TM57M5625-MTP-37	SSOP 48 pin (300mil)
TM57M5640-MTP	Wafer / Dice blank chip
TM57M5640-COD	Wafer / Dice with code
TM57M5640-MTP-72	LQFP 48-pin (7mm x 7mm)
TM57M5640-MTP-73	LQFP 64-pin (7mm x 7mm)
TM57M5645-MTP	Wafer / Dice blank chip
TM57M5645-COD	Wafer / Dice with code
TM57M5645-MTP-72	LQFP 48-pin (7mm x 7mm)
TM57M5645-MTP-73	LQFP 64-pin (7mm x 7mm)

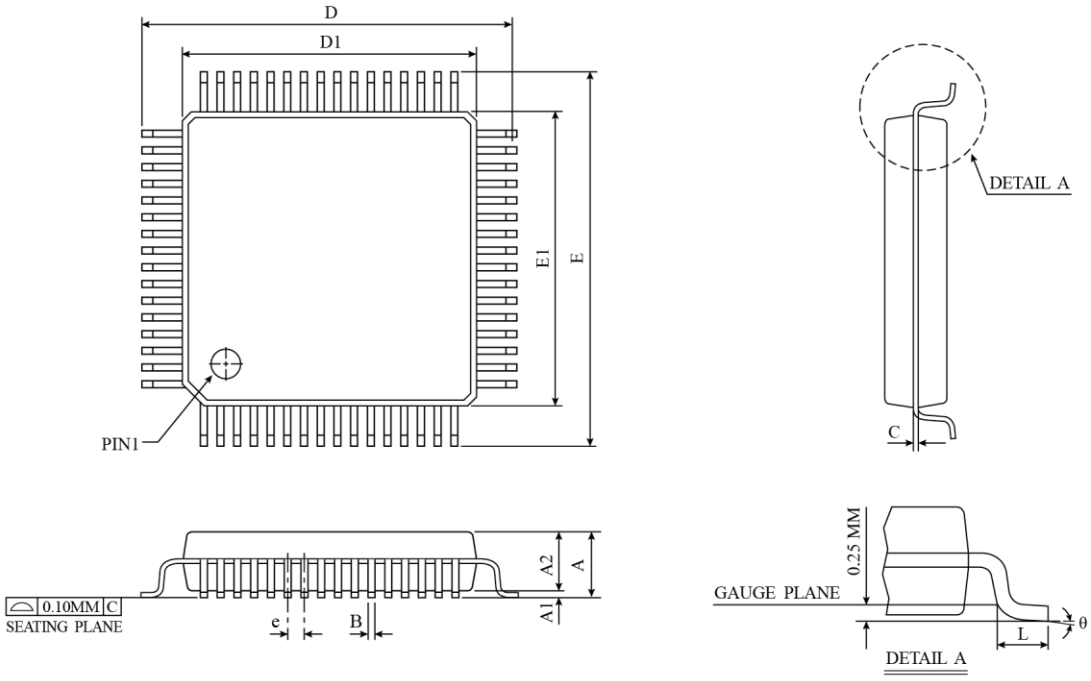
SSOP-48 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.413	2.604	2.794	0.095	0.103	0.110
A1	0.203	0.305	0.406	0.008	0.012	0.016
B	0.203	0.273	0.343	0.008	0.011	0.014
C	0.127	0.191	0.254	0.005	0.008	0.010
D	15.748	15.875	16.002	0.620	0.625	0.630
E	10.033	10.351	10.668	0.395	0.408	0.420
E1	7.391	7.493	7.595	0.291	0.295	0.299
e	0.635 BSC			0.025 BSC		
L	0.508	0.762	1.016	0.020	0.030	0.040
θ	0°	4°	8°	0°	4°	8°
JEDEC	M0-118 (AA)					

⚠ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.1524 MM (0.006 INCH) PER SIDE.

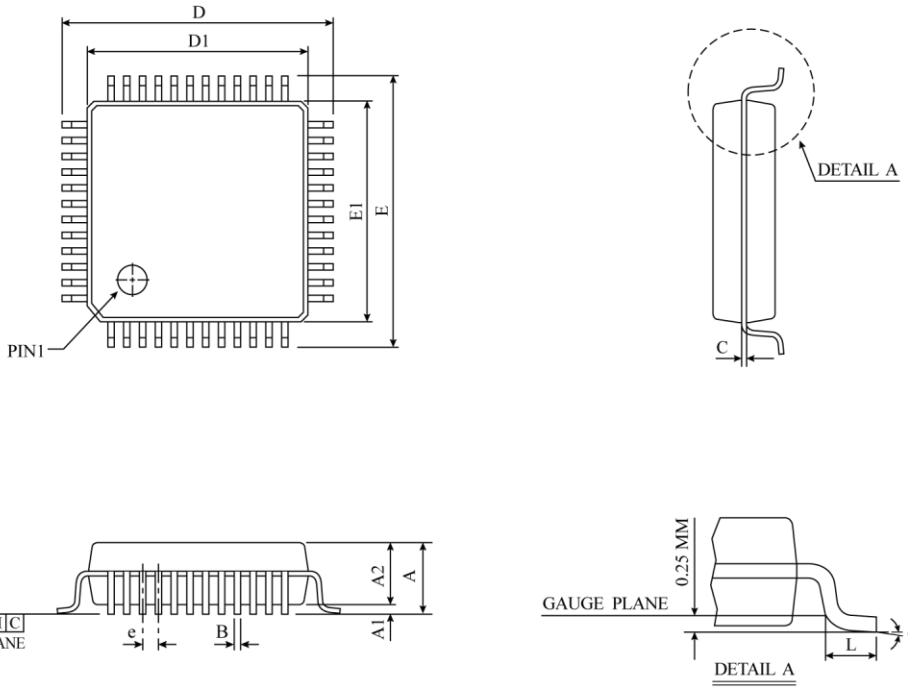
LQFP-64 Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.13	0.18	0.23	0.005	0.007	0.009
C	0.09	-	0.20	0.004	-	0.008
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
e	0.40 BASIC			0.016 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°	3.5°	7°	0°	3.5°	7°
JEDEC	MS-026 (BBD)					

△ * NOTES : DIMENSION "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSIONS IS 0.25mm PER SIDE. "D1" AND "E1" ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMACH.

LQFP-48 Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	0.10	0.15	0.001	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09	0.15	0.20	0.004	0.006	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°	3.5°	7°	0°	3.5°	7°
JEDEC	MS-026 (BBC)					

△ * NOTES : DIMENSION " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSIONS IS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMACH.